Control of Grid Connected Modular Multilevel Converter

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***Abstract*—This paper describes the control of multilevel voltage source active rectifier connected directly to ac grid. The proposed topology of multilevel converter is composed of three cascaded H-bridge converters (CHB), thus in this case seven level converter. Designed control algorithm provides direct current control in each phase even under unbalanced load. The main attention is paid to voltage balancing of the individual power cells (H-bridge). The voltage balancing algorithm is designed separately for each power cell. The paper presents simulation and experimental results of designed low-voltage laboratory prototype with rated power of 10 kW.**

***Index Terms*—AC-DC power converters, three-phase electric power, current control, linear feedback control systems.**

I. INTRODUCTION

The objective of this research has been analysis and design of control algorithm for three-phase multilevel voltage-source active rectifier (ac/dc converter), connected directly to ac grid without transformer. The multilevel converter topology is based on cascaded H-bridge converters. Presented grid connected modular converter consist of 3 CHB per phase resulting in 7 voltage level converter. The basic converter scheme is shown in Fig.1. This type of converter topology is well known e.g. [1]–[9]. The converter topology and designed control were tested on low-voltage single-phase laboratory prototype based on standard semiconductor parts. The final application of this multilevel converter is 6 MW/6 kV three-phase active rectifier connected to ac grid directly without transformer.

Proposed multilevel converter with developed control algorithm has these challenging requirements (i) the distribution of dc-link voltage on each H-bridge cell must be near to required value (U_{c_mXw} = 150 V) and (ii) harmonic ac currents should has very low THDi. These requirements are difficult to achieve especially for non-symmetrical condition like two phase operation for single-phase ac grid ground short-circuit. In addition we want to ensure a very low current ripple therefore PS-PWM (phase shifted pulse-width modulation) is used with zero vector alternating, which is well described in [10]–[11].

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II. PROPOSED CONTROL

Our designed control of ac/dc converter based on cascaded H-bridge uses three separate control loops (these control loops are the same for each converter phase – a, b, c). The presented control algorithm can operates under non-symmetric operation or with fully autonomous phase control. It allows proper converter function in single-phase short circuit grid-ground condition or under other single-phase grid faults. Each one of these independent control loops is composed of three parts as a shown in Fig. 2: (i) feed-forward (mathematical model) branch is located in the top of the figure, (ii) voltage and current control branch which is located in the middle part of the figure and (iii) voltage balancing branch is located in the bottom of the figure. Very important part of control algorithm is synchronization with ac grid. The designed control is composed of standard linear PI (proportional-integral) and PR (proportional-resonant) controllers. The narrow frequency response of the PR controllers provides high robustness on external disturbances and high quality sinusoidal response without permanent control error. Modulation for each phase is solved separately by PS-PWM (firing pulses phase_a, b, c in Fig. 2) and implemented in FPGA.

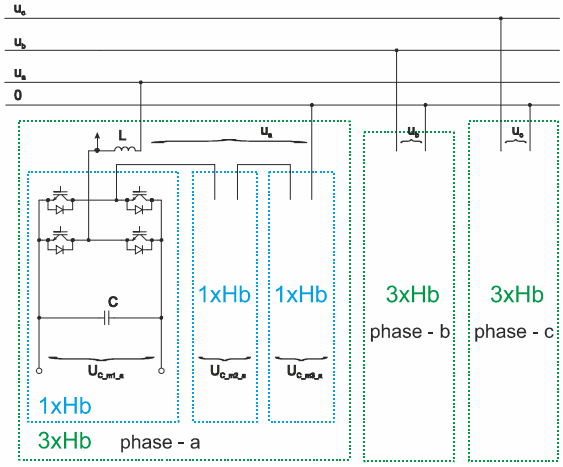

Fig. 1. Configuration of designed three-phase multilevel ac/dc converter based cascaded H- bridge cells.

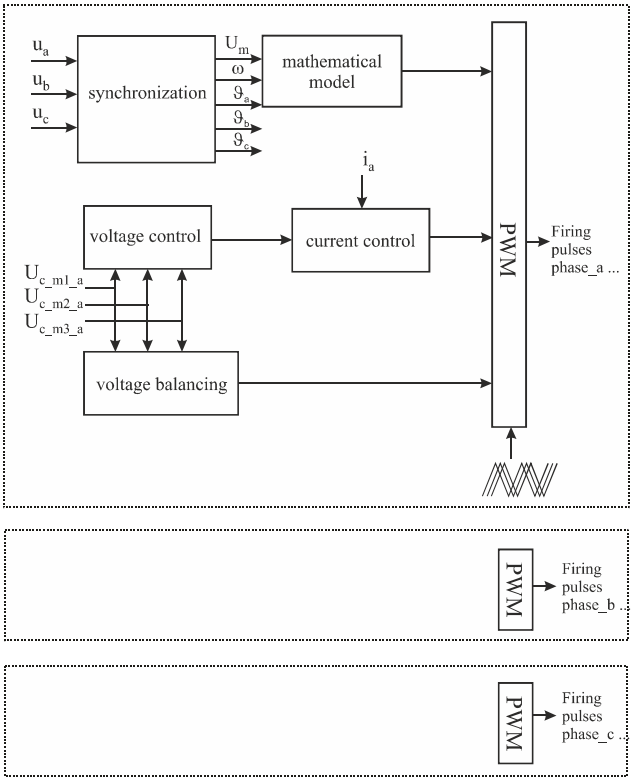

Fig. 2. Proposed control for three-phase multilevel ac/dc converter based cascaded H- bridge cells.

The control algorithm of each phase (it means single-phase control) of converter is shown more detail in Fig. 3. These control loops for phase_a are composed of synchronization block, with output signals U_m (v oltage magnitude), ω (voltage angular velocity), ϑ_a (position of voltage vector). These signals are important for mathematical model and also for direct current control loop. Mathematical model (feed-forward compensation) part allows faster transient response. The mathematical model use (1) for calculation signal u_{v_estim}. The values R (parasitic resistance) and L (induction) are constants and represents input inductor parameters, signal I_m is amplitude of required value of ac current (output signal from voltage controller R_{Uc_a}). The PI controller (R_{Uc_a}) is used for control sum of dc-link voltage (ΣU_{c_a}) to required value U_{cw}, with output signal I_m. The value ΣU_{c_a} is sum of voltage on dc-links cell of phase_a, as seen from (2). The direct current control is provided by PR controller R_{ia} and Resonant controller R_{3rd}. This resonant controller (R_{3rd}) is in this case use as third harmonic compensator (for dead-time effect minimization). This method is well described in [10] or it is also possible to use filtration method described in [12] and [13]. The resulting value $u_{v\_m1\_a}$ enters into PWM modulator and firing pulses switch the first cell (H-bridge) of phase_a. The second and the third cells are switched according to signals $u_{v\_m2\_a}$ and $u_{v\_m3\_a}$. The value of these modulation signals $u_{v\_m2\_a}$, $u_{v\_m3\_a}$ are slightly modified to ensure balancing of dc links of each cell in the phase_a by PI controllers $R_{\Delta Uc\_m2}$ and $R_{\Delta Uc\_m3}$. These controllers only modify the value of modulation signals size $u_{v\_m2\_a}$, $u_{v\_m3\_a}$ from the signal $u_{v\_m1\_a}$. The signals modification depends on sign of requirement current magnitude (sign(I_m)).

Controller settings were found empirically by using extensive simulations as compromise between stability and response behaviour. The controllers were tuned separately for the current control loop (R_i, R_{3rd}), the voltage control loop (R_{Uc}) and finally for the voltage balancing controllers ($R_{\Delta Uc\_m2}$, $R_{\Delta Uc\_m3}$). The final controllers' adjustment were held at the low-voltage laboratory prototype and resulting settings were: R_i (K_p = 1.1, K_r = 50), R_{3rd} (K_r = 20), R_{Uc} (K_p = 0.3, T_i = 0.05 s), $R_{\Delta Uc}$ (K_p = 0.005, T_i = 0.1 s).

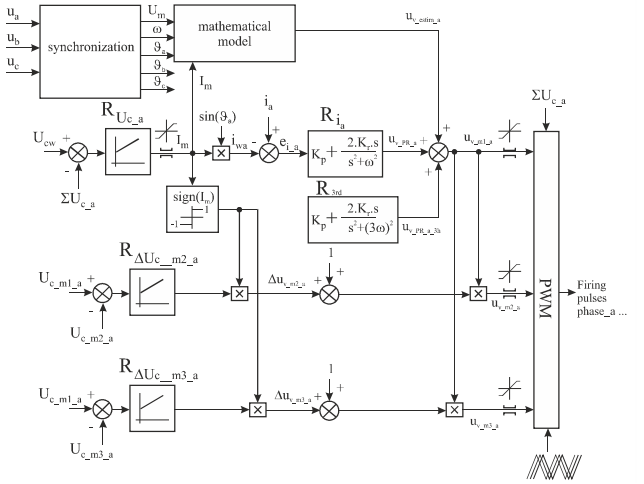

Fig. 3. Detail of single-phase part of control of multilevel converter, including voltage balancing controllers.

$$u_{v\_estim} = \left(U_m - R.I_m\right).\sin\left(\vartheta_a - \arctan\frac{\mu.L.I_m}{U_m - R.I_m}\right), \quad (1)$$

$$\sum U_{c\_a} = U_{c\_m1\_a} + U_{c\_m2\_a} + U_{c\_m3\_a}. \quad (2)$$

III. SIMULATIONS AND EXPERIMENTAL RESULTS

The converter behaviour with designed control was at the first time tested on the simulation model of active rectifier (Fig. 1). The simulation model consists of three-phase voltage source (ua, ub, uc), input inductance L, three H-bridge for each phase connected in series, their dc-link capacitors (C) and nine separate equivalent current sources (iz_a_M1 - iz_c_M3) representing the load of active converter. The switching frequency of IGBTs is fixed to 800 Hz. The PWM frequency was chosen in relation to the final application 6 MW/6 kV to achieve low switching losses on semiconductors.

The active rectifier was simulated for non-symmetrical load ($i_{z\_a\_M1}$ = 7 A, $i_{z\_a\_M2}$ = 7.3 A, $i_{z\_a\_M3}$ = 7.6 A, $i_{z\_b\_M1}$ = 5.6 A, $i_{z\_b\_M2}$ = 5 A, $i_{z\_b\_M3}$ = 5.3 A, $i_{z\_c\_M1}$ = 5 A, $i_{z\_c\_M2}$ = 6 A, $i_{z\_c\_M3}$ =7 A) as a shown in Fig. 4 and Fig. 5. Figure 4 represents current waveforms i_a, i_b, i_c. Currents have a sinusoidal shape and zero phase shift with ac grid voltage u_a, u_b, u_c. In this case the non-symmetrical load leads to different ac current amplitudes and current ripples. Different current ripples are based on different load impedances, resulting in different power and final size of phase modulation signals. The output dc-link voltage at individual power cells for step change of load is shown in Fig. 5.

Experimental tests of ac/dc converter were tested for the single-phase variant of converter. The converter load was represented by controlled inverter. The power circuit is shown in Fig. 6 and the converter power was limited to 1.1 kW. The complete experimental test values and parameters are given in Table I.

The control of multilevel converter has been implemented in the floating-point digital signal microcontroller Texas Instruments TMS320F28335 and PS-PWM modulator was realized on FPGA Altera EP3C40. Both devices are located on development board specially designed to control multi-level converters (described in 0). Utilization of FPGA allows to have perfectly synchronous PWM outputs, which are needed for proper function of PS-PWM. The FPGA design consists of basic system part as described in 0 and modulators part itself. Each full H-bridge has its own modulator (Fig. 7). The input signals ($u_{v\_mX\_a}$, Period, Dead-time and Sawtooth phase shift) are type of int_16t and accessible by memory space of microcontroller. The control signals (dashed lines) are reachable through single configuration register. It is very easy to expand design to support more H-bridges, thus creates more levels of output voltage.

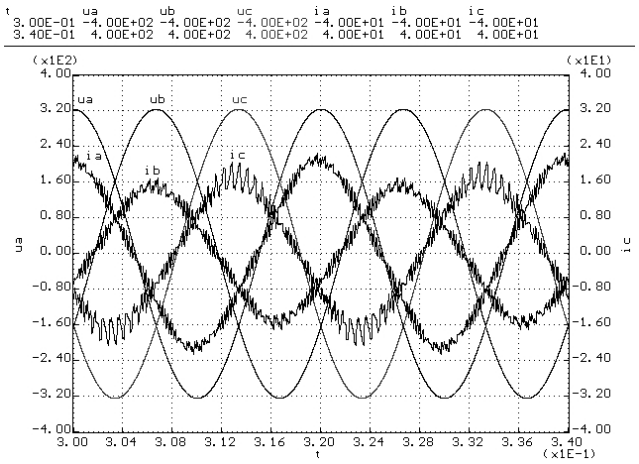

Fig. 4. Simulation – phase-voltages and currents of three-phase multilevel ac/dc converter under steady-state conditions in rectifier mode for non-symmetrical loadphase-voltages u_a, u_b, u_c [80 V/div]phase-currents i_a, i_b, i_c [8 A/div].

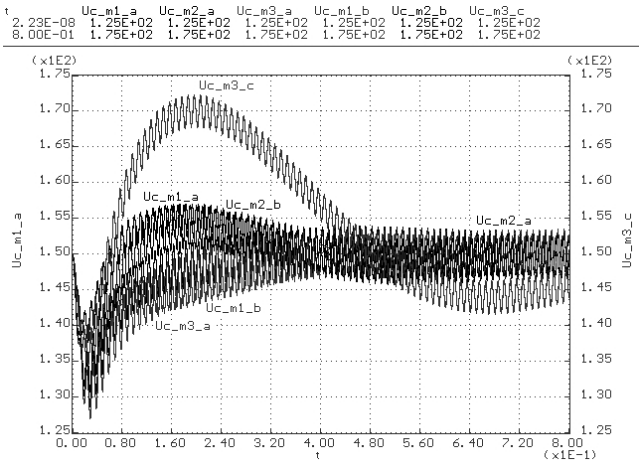

Fig. 5. Simulation – Voltage on selected dc links of three-phase multilevel ac/dc converter under step change of non-symmetrical load $i_{z\_a\_M1}$=7 A, $i_{z\_a\_M2}$=7.3 A, $i_{z\_a\_M3}$=7.6 A, $i_{z\_b\_M1}$=5.6 A, $i_{z\_b\_M2}$=5 A, $i_{z\_b\_M3}$=5.3 A, $i_{z\_c\_M1}$=5 A, $i_{z\_c\_M2}$=6 A, $i_{z\_c\_M3}$=7 A DC-links voltages U_{c_m} [5V/div].

Figure 8–Fig. 11 present single-phase seven-level CHB active rectifier experimental results. Figure 8 illustrates the converter start-up under non-load conditions. Very fast rise of the current (violet signal) is caused by requirement to maximal current. At the first moment operates mainly model part of control. The voltage at dc-links (dark blue, light blue, green signals) rise from value 108 V (charged via diode rectifier) to required value 150 V.

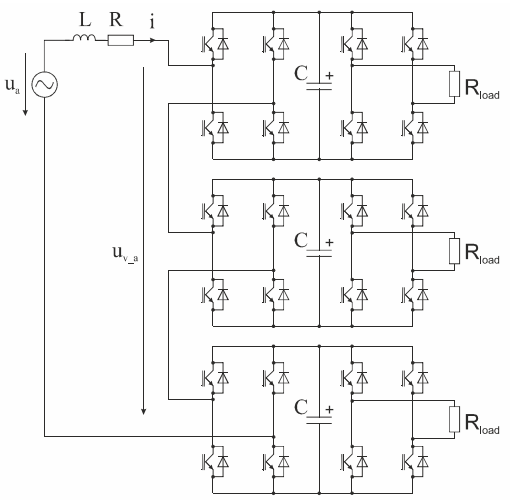

Fig. 6. Experimental low-voltage setup of single-phase seven-level CHB active rectifier.

TABLE I. PARAMETERS OF EXPERIMENTAL TEST.

Converter power for experiments	P = 1.1 kW
ac grid voltage	u_a = 230 V_{rms} / 50 Hz
Input inductor	L = 6 mH R = 0.2 Ω
Value of dc-link capacitors	C = 6 mF
Required dc-link voltage	U_{DCw} = 150 V
Switching frequency of IGBTs	f_{swit} = 800 Hz

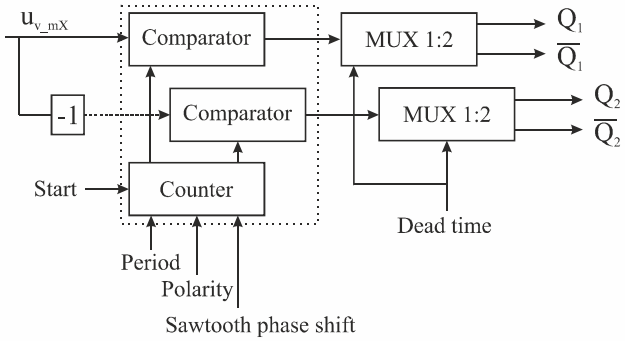

Fig. 7. Scheme of modulator for one H-bridge cell.

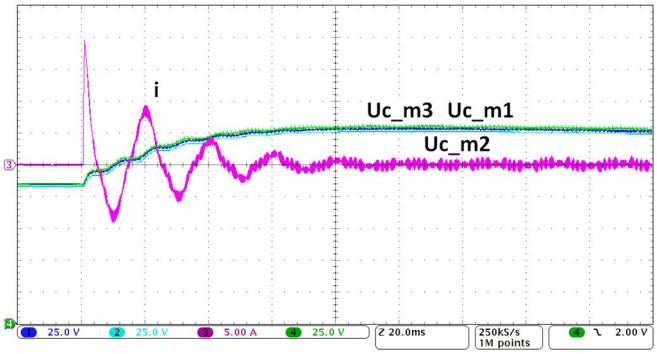

Fig. 8. Experiment – laboratory setup of single-phase multilevel converter under start-up sequence (converter load P = 0 kW) U_{c_m1} – dc-link voltage on first cell [25 V/div], U_{c_m2} – dc-link voltage on second cell [25 V/div], i– ac current (5A/div), U_{c_m3} – dc-link voltage [25V/div].

Figure 9 shows converter behaviour in rectifier mode under steady-state condition with load 1.1 kW. The green signal represents ac grid voltage with zero phase shift with ac current (violet signal). The dark blue signal represents voltage on ac converter terminals u_{v_a} seven voltage levels for this case (it is due the correct functions of PS-PWM for

three H-bridge cells). The frequency of current ripple is 4800 Hz. That is result of PS-PWM and zero vectors alternating modulation technique.

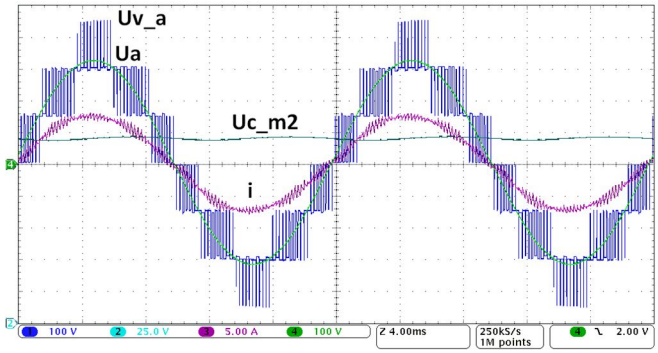

Fig. 9. Experiment – laboratory stand of single-phase multilevel converter under steady-state (symmetrical converter load P = 1.1 kW) u_{v_a} – Voltage at converter ac terminals [100 V/div], U_{c_m2} – dc-link voltage on second cell [25 V/div], i – ac current (5 A/div), u_a – Voltage of ac source [100 V/div].

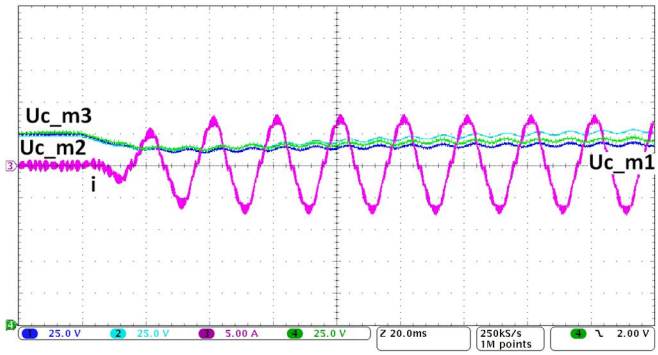

Fig. 10. Experiment – laboratory setup of single-phase multilevel converter under step change of non-symmetrical load (converter load 0 kW→1 kW, second cell load 90 %) U_{c_m1} – dc-link voltage on first cell [25 V/div], U_{c_m2} – dc-link voltage on second cell [25 V/div], i – ac current (5 A/div), U_{c_m3} – dc-link voltage [25 V/div].

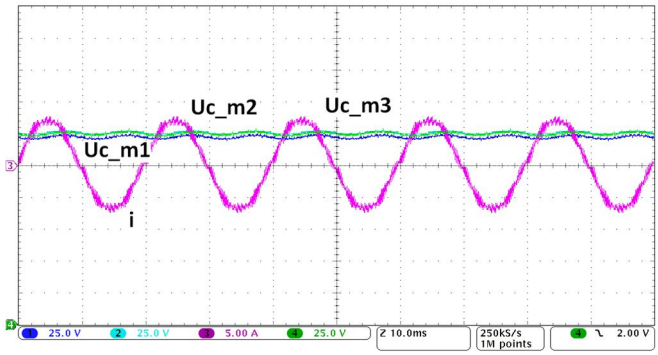

Fig. 11. Experiment – steady after transient with non-symmetrical load from Fig. 8 (converter with non-symmetrical load P=1kW, second cell load 90 %) U_{c_m1} – dc-link voltage on first cell [25 V/div], U_{c_m2} – dc-link voltage on second cell [25 V/div], i – ac current (5 A/div), U_{c_m3} – dc-link voltage [25 V/div].

Figure 10 shows converter response on step change of load (with 10 % asymmetry for second cell). The light blue signal representing the voltage on dc-link of second cell rises faster because the load of this cell is lower than in other cells. Due to gradual control, PI controllers stabilize of all voltages at dc-links to required value 150 V (shown in Fig. 11).

IV. CONCLUSIONS

This paper presents prospective topology of ac/dc multilevel converter connected directly to ac grid. The main attention is paid in the control and active power cell dc-link voltage balancing strategy of input active rectifier. Designed control of cascaded H-bridge voltage-source active rectifier provides sinusoidal current waveform shape (even for non-symmetrical converter load). The algorithm provides voltage balancing on individual power cells directly at the control structure level. This simple and powerful approach can be easily achieved by using conventional PR and PI controllers. These types of controllers are industry-standard components and can be easily implemented in common processors. The paper consists of simulation results supported by experimental test on the laboratory prototypes.

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