A Novel Low Voltage Low Power OTA Based on Level Shifter Current Mirror

Okkes Gokalp Sokmen[1], Hamdi Ercan[2], Sezai Alper Tekin[3], Mustafa Alci[1]
[1]*Department of Electrical and Electronics Engineering, Erciyes University, 38039, Kayseri, Turkey*
[2]*Department of Avionics, Erciyes University, 38039, Kayseri, Turkey*
[3]*Department of Industrial Design Engineering, Erciyes University, 38039, Kayseri, Turkey*
hamdiercan@erciyes.edu.tr

***Abstract*—In this paper, a low voltage low power operational transconductance amplifier (OTA) structure is proposed. To achieve the low voltage low power operation, level shifter current mirrors are employed in the circuit structure. The proposed structure operates at ±0.5 V as supply voltages and dissipates power as 83 µW. Positive and negative slew rate of the circuit is 223 V/µs and 162 V/µs, respectively. Furthermore, the bandwidth of the circuit is about 80 MHz. The designed OTA is simulated with 0.18 µm TSMC CMOS technology parameters using SPICE. Simulation results have been justified the theoretical approach.**

***Index Terms*—Analog integrated circuits, CMOS integrated circuits, current mode circuits, operational amplifiers.**

I. INTRODUCTION

In recent years, usage of the battery-powered devices such as smart phones and portable medical equipments have became really widespread. In addition, IC technology tends to minimize the device dimensions. Therefore, channel dimensions of the MOS transistors have been reached to the range of nanometers. The recent MOS structures with smaller channel dimensions are able to operate with low supply voltages. Thus, low voltage low power (LVLP) circuit design becomes the major topic of the analog IC technology [1], [2].

For analog signal processing, a wide range of the active devices are easily available in the literature. The analog signal processing devices can be classified into two groups such as voltage mode and current mode devices. Formerly, voltage mode active blocks such as op-amps were widely used. In terms of bandwidth, slew rate, power dissipation and circuit complexity, the voltage mode devices exhibit the worse performance. Therefore, the current mode devices such as current conveyors and operational transconductance amplifiers (OTA) have became more popular in recent years. The OTAs are promising active element used in analog circuit design [3]–[8]. Furthermore, the OTAs produce output current proportional to the differential input voltage and their gain can be controlled by the bias current. Thus, the OTAs are useful devices for current controlled applications. There are a lot of circuit structures designed with OTA such as filters, instrumentation amplifiers, oscillators and analog multiplier in the previous studies [9]–[13]. Although any number of the OTA structures has been in literature, to meet demands of the day, the researchers are studying to design new OTA structures which have more linearity, wider dynamic range, lower power consumption and lower supply voltages [14]–[20].

The OTA proposed in this paper employed level shifter current mirrors as an active load to operate with lower supply voltages and cross-coupled quad transconductance structure is used to improve the linearity [21]–[24]. Also, a current controlled low pass filter is designed to indicate the applicability of the proposed circuit. The proposed OTA and the low pass filter are simulated with 0.18 µm CMOS technology parameters using SPICE. Simulation results have been justified the theoretical approach. The proposed circuit can operate with ±0.5 V and consume low power. Also, the circuit not only exhibits good slew rate performance but also has an acceptable frequency behaviour.

II. PROPOSED OTA STRUCTURE

The proposed LVLP OTA is shown in Fig. 1. Bulk terminals of the all NMOS transistors are connected to the negative supply voltage, and bulk terminals of the all PMOS transistors are connected to the positive power supply. To achieve the low voltage operation, a PMOS level shifter current mirror has been designed with using M1, M2 and M5 transistors, and also the another PMOS level shifter current mirror has been designed with using M3, M4 and M6 transistors [21]. Moreover, a NMOS level shifter current mirror has been formed with using M9, M10 and M11 transistors [22]. Because the current mirrors need the bias current, I_{D12}, I_{D13} and I_{D14} are used as bias current. For the current mirror composed of M1, M2 and M5 transistors, the biasing current I_{D12} can be obtained as

$$I_{D12} = I_{D0}\frac{W_{12}}{L_{12}}\exp\left(\frac{-V_{THN}}{nU_T}\right), \quad (1)$$

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where I_{D12} is the drain current of the M12, U_T is the thermal voltage, W_{12}/L_{12} is the aspect ratio of the M12 and V_{THN} is the threshold voltage. Also, I_{D0} and n are the process-dependent constants. The biasing current of the other level shifter current mirrors I_{D13} and I_{D14} can be defined as similar to I_{D12}. Hence, M12, M13 and M14 transistors provide very small bounded bias currents to level shifter current mirrors. Thus, M5, M6 and M9 transistors operate in subthreshold region. Additionally, C1, C2 and C3 capacitors are used to improve the frequency performances of current mirrors.

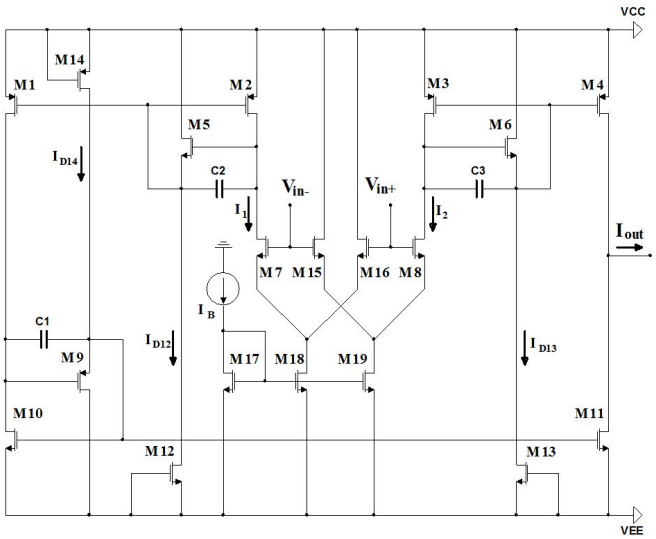


Fig. 1. Proposed level shifter current mirror based low voltage low power OTA.

M7, M8, M15 and M16 transistors are employed as cross coupled transconductance cell. M17, M18 and M19 have copied the I_B to the cross coupled transconductance cell as the biasing current [23], [24].

In Fig. 1 it is assumed that the aspect ratio of the M7 and M8 transistors is equal to W/L and the aspect ratio of the M15 and M16 transistors is equal to $a(W/L)$. I_1 and I_2 currents are determined as:

$$I_1 = k\left[\frac{-aV_{in}}{a+1} + \sqrt{\frac{1}{k}}\sqrt{1-\frac{kaV_{in}^2}{(a+1)I_B}}\right]^2, \quad (2)$$

$$I_2 = k\left[\frac{aV_{in}}{a+1} + \sqrt{\frac{1}{k}}\sqrt{1-\frac{kaV_{in}^2}{(a+1)I_B}}\right]^2. \quad (3)$$

where V_{in} is the differential input voltage and equal to $V_{in+} - V_{in-}$ and k is equal to $(1/2)\cdot\mu_n\cdot C_{ox}\cdot(W/L)$.

The current I_1 is copied to the drains of the M1 and M11 transistors. Also, the current I_2 is copied to the drain of the M4 transistor by the level shifter current mirrors. Hence, it is obviously seen that the output current I_{out} can be obtained as

$$I_{out} = I_2 - I_1. \quad (4)$$

If the aspect ratio of the M15 and M16 transistors are chosen as much greater than the aspect ratio of the M7 and M8 transistors, in other words if a is much greater than 1, the output current I_{out} can be written as below using (2), (3) and (4)

$$I_{out} = 4\sqrt{\frac{kI_B}{a}} \times V_{in}. \quad (5)$$

Here, the transconductance (g_m) of the circuit can be obtained as

$$g_m = 4\sqrt{\frac{kI_B}{a}}. \quad (6)$$

It is obviously seen from (6) that the g_m of the proposed circuit can be controlled by the biasing current I_B.

III. Simulation Results

The designed OTA is simulated with 0.18 µm TSMC CMOS technology parameters using SPICE. The supply voltage is chosen as ±0.5 V. Transistor dimensions of the proposed OTA are given in Table I. The all capacitors shown in Fig. 1 are chosen as equal to 0.1 nf.

TABLE I. TRANSISTOR DIMENSIONS OF THE PROPOSED OTA.

Transistor	L(µm)	W(µm)
M1 - M4	0.5	3
M5, M6	0.5	10
M7, M8	1	0.5
M9	0.5	25
M10, M11	0.5	1
M12 - M14	3	30
M15, M16	0.35	15
M17 - M19	1	3

Figure 2 shows the transfer curve of the proposed OTA. As seen in Fig. 2, the linear operation range of the proposed circuit can be defined as ±0.3 V. Furthermore, the transconductance can be controlled by the biasing current.

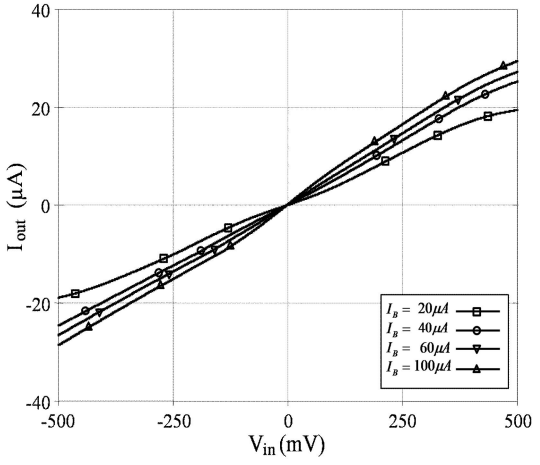


Fig. 2. The transfer curve of the proposed OTA.

Figure 3 indicates the g_m versus I_B. As shown in Fig. 3, the transconductance of the circuit can be controlled between 21 µS and 73 µS while I_B varies from 10 µA to 100 µA.

Figure 4 and Fig. 5 show the g_m – frequency curve and the unity voltage gain – frequency curve, respectively. It is clearly seen from Fig. 4 and Fig. 5 that the bandwidth of the proposed circuit is about 80 MHz. This value is highly

reasonable when compared to LVLP circuits.

The pulse response of the proposed OTA is shown in Fig. 6. Positive and negative slew rates of the circuit are obtained as 223 V/μs and 162 V/μs, respectively. It is obvious that the OTA exhibits acceptable performance with these values of the slew rate. The performance of the proposed OTA for different temperature values is depicted in Fig. 7. It is obviously seen that the temperature compensation can provide benefit for the circuit.

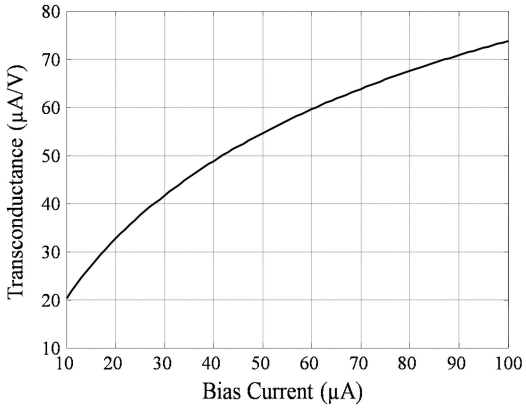


Fig. 3. The Variation of the g_m with the biasing current I_B.

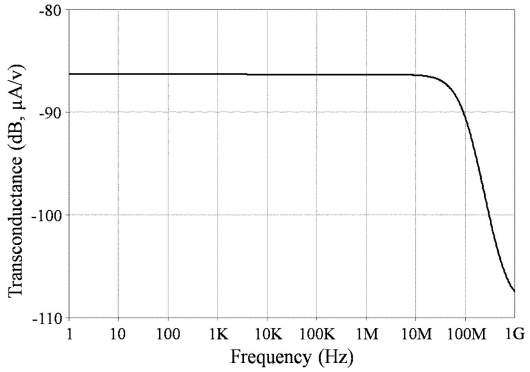


Fig. 4. The g_m – frequency curve.

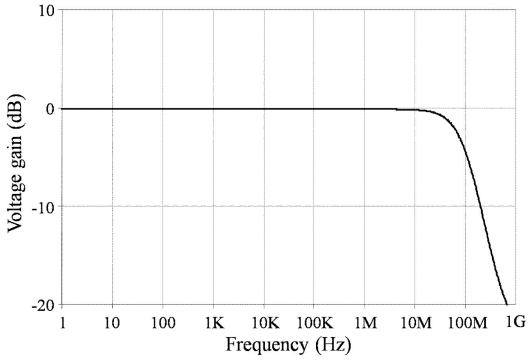


Fig. 5. The unity voltage gain – frequency curve.

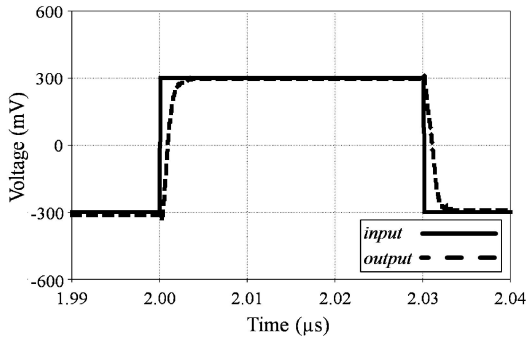


Fig. 6. The pulse response of the proposed OTA.

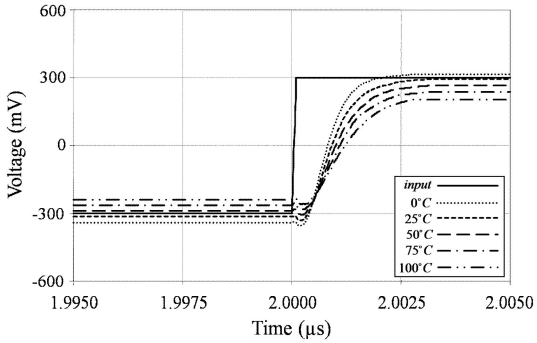
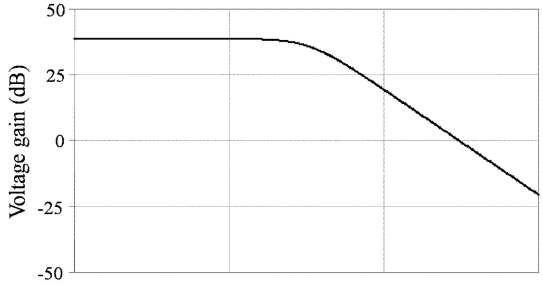
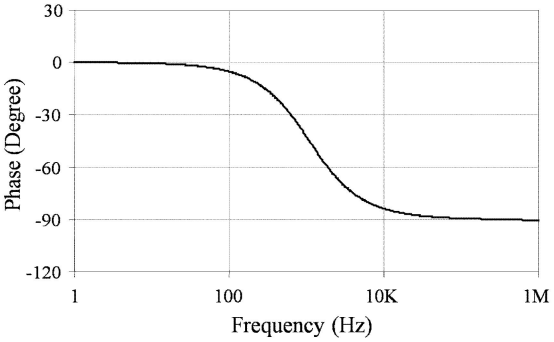


Fig. 7. The pulse response of the proposed OTA versus different temperature.



(a)

Figure 8 indicates the frequency response of the proposed circuit for 80 pF capacitive load. Phase margin of the circuit is 89.44˚. Considering that this value is quite close to 90˚, the proposed OTA can highly be operated at stable state [25].



(b)

Fig. 8. Frequency response of the proposed circuit for 80pF load.

The frequency response of the CMRR is indicated in Fig. 9. The CMRR of the circuit is about 64 dB up to 1 MHz. Also, the CMRR is about 60 dB at 10 MHz. However, the CMRR values of the other structures exhibit dramatically decreasing over the 10 KHz [18], [19]. The CMRR value of the proposed circuit is admirable at 10 MHz.

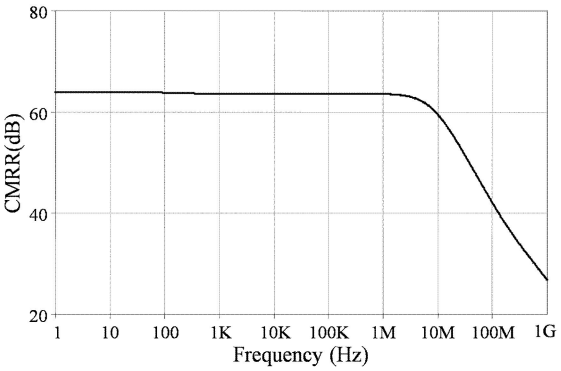


Fig. 9. CMRR versus frequency.

Figure 10 shows CMRR, MonteCarlo analysis, which is repeated for 35 times. Figure 10 justifies that CMRR value has still high under 5 % random variations in threshold voltages of the transistors. Figure 10 indicates the good performance of the proposed circuit versus mismatches.

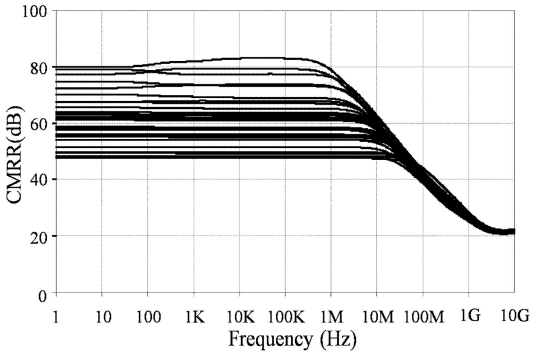


Fig. 10. Monte Carlo analysis for CMRR.

Figure 11 indicates the total harmonic distortion (THD) of the proposed circuit. The THD is 1.42 % when input is equal to 600 mV_{P-P}. Also, simulation results show that the proposed OTA consumes 83 µW power. Hence, the proposed OTA is highly suitable for low power applications.

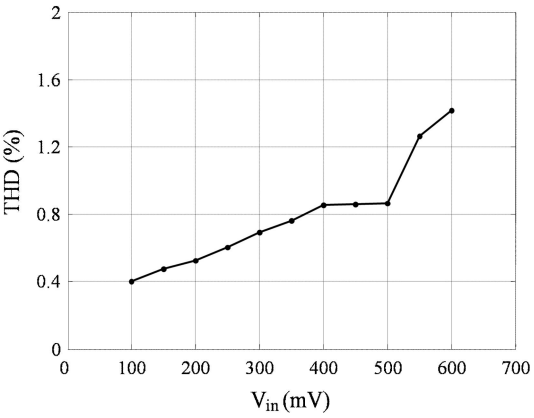


Fig. 11. Total harmonic distortion for input voltage at 100 KHz.

Performance parameters of the proposed circuit and the other OTA's are given in Table II. When the proposed OTA is compared to others as shown in Table II, the proposed OTA can operate with lower supply voltages and consumes lower power. Furthermore, slew rate values of the proposed circuit are higher than the previous circuits. As seen in Table II, although the proposed OTA has reasonable performance in terms of the bandwidth and the THD, some of the other OTA circuits have better performance. Also, CMRR value of the proposed circuit is larger than 60 dB up to 10 MHz. Although the CMRR value of the circuit is shown lower than the others in Table II, the proposed circuit exhibits a better performance above 10 KHz than the others. Consequently, it is figured out that the proposed OTA is suitable for analog integrated circuits and LVLP applications.

IV. OTA BASED LOW PASS FILTER APPLICATION

To show the applicability of the proposed circuit, a basic OTA based low pass filter is formed. The low pass filter is shown in Fig. 12.

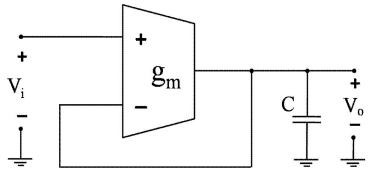


Fig. 12. OTA based low pass filter.

The transfer function and the cut-off frequency of the filter are given below:

$$T(s) = \frac{(g_m/C)}{s+(g_m/C)}, \tag{7}$$

$$\mu_C = \frac{g_m}{C}. \tag{8}$$

The filter is simulated for different biasing currents. The capacitor is chosen as equal to 0.5 nF. The voltage gain-frequency curve of the low pass filter is shown in Fig. 13. It is obviously seen in Fig. 13 that the g_m of the proposed OTA can be controlled by the biasing current. Therefore, the cut-off frequency of the low pass filter can be controlled by the biasing current. Actually, the simulation results confirm the theoretical approach of the low pass filter.

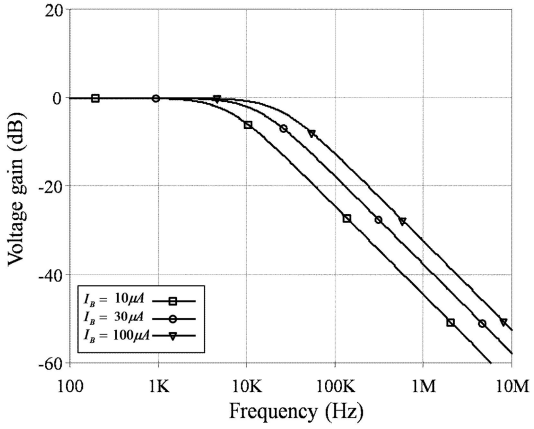


Fig. 13. Voltage gain – frequency curve of the low pass filter.

TABLE II. THE COMPARISON OF PERFORMANCE PAMARAMETERS FOR OTAS.

	This work	**[14]**	**[15]**	**[16]**	**[17]**	**[18]**
CMOS tech. (µm)	0.18	0.5	0.5	0.35	0.13	0.18
Supply voltage (V)	±0.5	±1	±1	3.3	±0.65	±0.75
Power dissipation (µW)	83	140	220	4800	1200	397.5
Bandwidth (MHz)	80	470	3.27	90	NA	3.72
Slew rate$^{(+)}$ (V/µs)	223	42	10	200	24.3	5.6
Slew rate$^{(-)}$ (V/µs)	-162	- 80	-15	NA	NA	-4
CMRR (dB)	64	69	85	NA	NA	259
THD (dB)	-37 (0.4 V_{pp}, 100 KHz)	-41 (0.9 V_{pp}, 100 KHz)	-37 (0.9 V_{pp}, 100 KHz)	-59 (0.4 V_{pp}, 700 KHz)	-84	NA
Capacitive Load (pF)	80	80	80	13	1	17
Phase Margin ($^{\circ}$)	89.44	90	56	61	45	70

V. CONCLUSIONS

In this paper, a novel level shifter current mirror based low voltage low power OTA is proposed. Furthermore, to demonstrate the operation of the OTA, a basic low pass filter is employed. The proposed OTA and the low pass filter are simulated with 0.18 µm CMOS technology parameters using SPICE. The simulation results confirm the theoretical approach. Moreover, the proposed circuit is compared to the other OTA structures in the literature. Hence, the advantages and disadvantages of the proposed circuit are determined. The major advantages of the considered OTA are the operating with ±0.5 V supply voltage capability and having lower power dissipation as 83 µW. Also, the positive and negative slew rates of the proposed circuit are high values as 223 V/µs and 162 V/µs, respectively. In addition, the bandwidth is about 80 MHz. Also, the THD and CMRR values of the circuit are reasonable. Consequently, it is figured out that the proposed OTA is quite convenient for analog integrated circuits and LVLP applications.

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