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Modeling of Manufacturing Processes in EPIC Technology

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Introduction

EPIC (engl. *Epitaxial Pasivated Integrated Circuit*) is an integrated circuit (IC) manufacturing technology where combined (epitaxial and dielectric layers) insulation is used. This type of insulation allows to avoid parasitic connections between elements and to improve IC characteristics, to increase the number of integration of elements (transistors etc.) [1]. This technology is used for formatting specialized IC on the base of bipolar transistor structures. The characteristics of IC elements depend on technological IC treatment, design, and operating conditions. One of the most complex objectives is to identify and evaluate the changes of designed IC structures through the whole cycle of manufacturing. Most of the time it is done experimentally by examination IC already produced, and then setting technological treatment required. It is expensive and time consuming. The structure changes in IC manufacturing cycle are mostly determined by high temperature technological process (HTTP) modes, which influence dopant reallocating in diffusive layers, and by this form the characteristics and manufacturing faults of elements formed. Main modes of HTTP are time for structure forming and technological process temperature. The mathematical model of the sequence of HTTP in EPIC is created on the grounds of Fick‘s law and MathCAD, Excel, AutoCAD programs. Each mode of HTTP through all cycle and their influence for structures formed are evaluated in mathematical model. The reliance between current gains α and β and HTTP modes is determined.

Creating a mathematical model of HTTP

Enlarging the process of EPIC manufacturing, we get 19 TP. The actual number of small TP depends on IC type and can be about few dozens. From a created technological cycle the HTTP sequence can be extracted. This sequence consists of 9 HTTP. The main problems of integrated circuit manufacturing are:

- Direct problem – find the distribution of dopants in diffusive layers according to TP regimens given [5];

- Indirect problem – find TP regimens: time, temperature, according to distribution of the diffusion layer already formed or *pn* junction [5].

To solve these problems it is essential to create a mathematical model based on Fick's laws mathematic expressions. The incoming parameters in this model will be time and temperature of each HTTP. Main out coming parameters will be current gain α and β of n^+pn transistor and their reliance with technological regiments of their manufacturing. Of course, analyzing HTTP, it is important to know the distribution and redistribution of dopants after each HTTP, for this reason the influence of HTTP to layers of diffusion is evaluated. Based on equation (1), connection coefficients are estimated [2]:

$$(Dt)_{tot} = \sum_i D_i t_i \; ; \qquad (1)$$

All 9 HTTP influence the distribution of dopants in “hidden” n^+ layer in EPIC technology. All HTTP technological regiments must be evaluated to receive desirable deviation and thickness of this layer. The influence of each HTTP (according to technological cycle) is transferred through connection coefficients ξ_i (2) (i – number of HTTP), diffusion coefficient D_i, which directly depends on temperature, and performance time t_i of HTTP. The change of depth x_i of this layer is important because it causes breakdown voltage of collector and base junction and collector body resistance. Diffusion coefficients D depend not only on HTTP temperature, but also on the type of diffusing material. According to the technological cycle of IC, two diffundands *B* and *As* are used, so other connection coefficients ξ_{ib} (2) (i – HTTP number) must be foreseen.

$$\begin{cases} \xi_1 = D_1 t_1; \\ \xi_2 = \xi_1 + D_2 t_2; \\ \xi_3 = \xi_2 + D_3 t_3; \\ .....; \\ \xi_i = \xi_{i-1} + D_i t_i; \end{cases} \qquad \begin{cases} \xi_{6b} = D_{6b} t_{6b}; \\ \xi'_{6b} = D'_{6b} t'_{6b}; \\ \xi_{7b} = \xi_{6b} + D_{7b} t_7; \\ .....; \\ \xi_{ib} = \xi_{(i-1)b} + D_{ib} t_i; \end{cases} \qquad (2)$$

here D_i, t_i – coefficient and time, respectively, of HTTP diffusion using arsenic; D_{ib} – coefficient and time, respectively, of HTTP diffusion using boron. D'_{6b}, t'_{6b} - coefficient and time, respectively, of sixth HTTP in first stage of diffusion.

Modeling dopant deviation in EPIC integrated circuit

Accepting HTTP regiments noted in Table 1, the distribution and redistribution of formed diffusion layers after each HTTP will be set according to mathematical model created.

Table 1. HTTP of EPIC technology

No	Process	T*, °C	t*, min	Dopant	E_a, eV	D_0, cm^2/s
1	Diffusion	~1220	~20	As	4,08	24
2	Oxidation	~1000	~40	-	-	-
3	Oxidation	~1200	~80	-	-	-
4	Epitaxy	~1150	~120	-	-	-
5	Oxidation	~1000	~40	-	-	-
6	Diffusion	~1100	~10	B	3,46	0,76
7	Oxidation	~1000	~40	-	-	-
8	Diffusion	~1000	~170	As	4,08	24
9	Oxidation	~1000	~330	-	-	-

Basic layers of EPIC are formed in diffusion. The temperature of these HTTP is over 1000°C. [3] Fig. 1. shows modeled distribution of dopants in bipolar transistor structure, evaluating the influence of HTTP to all layers. Final distribution of base p and emitter n^+ diffusion layers are important parameters evaluating gain coefficients α and β of bipolar transistor. Final base thickness can be estimated only after all HTTP evaluating. Base thickness ω is important parameter evaluating dependence of α and β on EPIC manufacturing regiments.

Change of diffusion layer depth

"Hidden", base, emitter and undercollector layers, formed in diffusion, and their dopant distribution, as well as depth change in relation with HTTP regiments. The change of diffusion layers according to the model created by the sequence of EPIC technology IC manufacturing is showed in Fig. 2.

Increasing of hidden n^+ layer depth is mostly noticeable performing 3rd, 4th and 6th HTTP, is caused by high temperature and long duration. The biggest increase of base layer depth is noticed in performing oxidation process (8th HTTP), because it is the longest HTTP of base. In modeling, the depths of diffusion layers are calculated from solutions of dopant distribution (Fick's) equations, in this case, the point of intersection is found, i.e. the point where the concentration of inserted dopants is the same as concentration of dopants already in the pad. In such case more accurate model of HTTP calculation is found. From the depth of "hidden" n^+ layer(evaluating all cycle of IC manufacturing), etching of needed depth of channels can be set, so that the capacity of "hidden" and collector layers junction would be the smallest and body resistance the biggest. In this case the optimization of the distance between base – collector junction x_{BK} and "hidden" layer – collector junction x_{KP} is needed. Optimum distance is supposed to be 0,3 - 3μm, so this condition can be set, to improve the model. This also helps to avoid manufacturing errors, because the thickness of "hidden" n^+ layer after all HTTP of IC can be 2,5 - 10μm, and choosing the depth of channel etching too small can cause base layer and "hidden" layer over cover (Fig. 3.), and because of this, collector area can disappear completely.

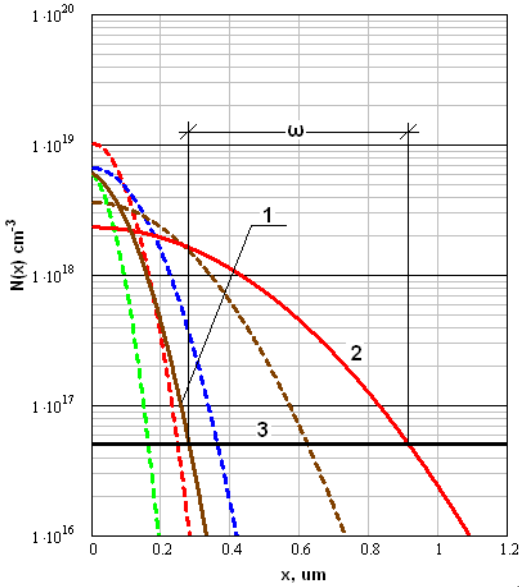

Fig. 1. Distribution of dopants concentration in emitter n^+ layer and base p layer after 6th – 9th - HTTP. 1 – distribution of dopants concentration in emitter n^+ layer after 9-th HTTP; 2 – distribution of dopants concentration in base p layer after 9-th HTTP; 3 – distribution of dopants concentration in collector n layer.; ω – depth of base

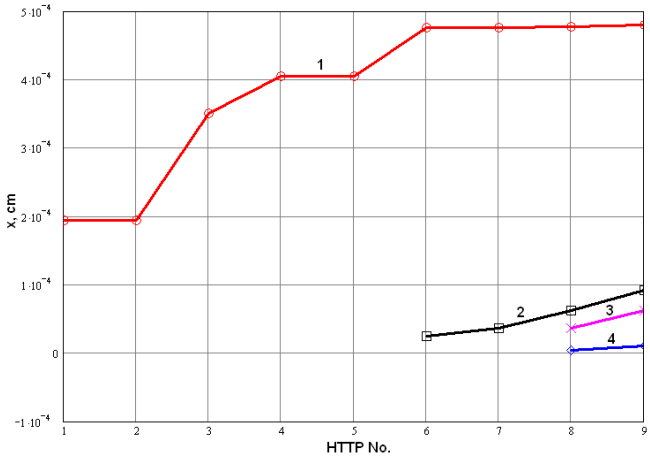

Fig. 2. Depth of diffusive layer after every HTTP and EPIC technology manufacturing cycle. 1- n^+ "hidden" layer; 2 – p base layer; 3 - n^+ collector layer; 4 - n^+ emitter layer

n^+pn transistor current gain dependance on HTTP in technology

Transistor current gains α (3) and β (5) are directly dependant on base thickness ω (4), and this depends on high temperature process producing EPIC.

As seen in Fig. 2. EPIC the depth of integrated circuit base, and by this thickness ω is influences only by last four HTTP. In this case, to evaluate the influence of these four HTTP to transistor current gain, regular method will be used. This method will not evaluate disturbances while manufacturing. Each of HTTP is described by two parameters – time and temperature, so we will change temperature by given step ΔT, and for each of these temperatures we will measure the dependence of current gain from time with step Δt.

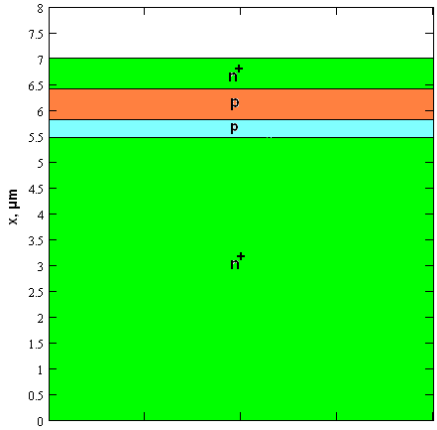

Fig. 3. Depth x of diffusive layers. Modeling of technology fault

As this method of analysis is regular we will change HTTP time with stable temperature, and other parameters, in this case, other HTTP regiments, will be stabled and not changing. The results will be from the created model, which evaluates all sequence of EPIC integrated circuit technological cycle as well as all HTTP influence to each other

$$\alpha = \frac{1-\frac{\omega^2}{2D_B\tau}}{1+\frac{\omega D_E N_B}{L_E D_B N_E}}; \qquad (3)$$

here α – current gain in common base junction; ω - base thickness, cm; L_E – length of unleading charge-carrying particles in diffusion emitter, cm; D_E and D_B – coefficients of charge-carrying particles diffusion in emitter and base, cm^2/s; N_E and N_B – concentration in base and emitter; τ - life cycle of unleading charge-carrying particles in base.

$$\omega = x_{bk} - x_{eb}; \qquad (4)$$

here x_{BK} – base depth (*pn* junction with collector area); x_{EB} – emitter depth (emitter area *pn* junction with base area)

$$\beta = \frac{\alpha}{1-\alpha}; \qquad (5)$$

here β – current gain in common emitter junction.

Modeling in these HTTP we choose 5 regiments of temperature 800°C, 900°C, 1000°C, 1100°C, 1200°C. As TP depends on time also, we choose time changing boundaries up to 2000 min. with step Δt=10 min. in the last HTTP we expand boundaries up to 400 min., because this oxidation is dry and long. In this case, the step is Δt=20 min.

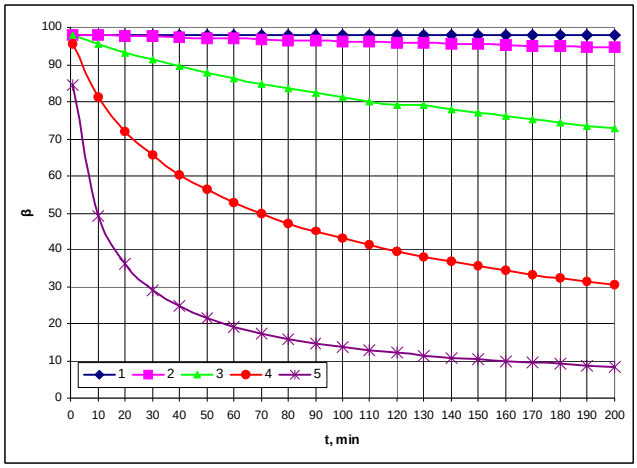

Fig. 4. The dependence of n^+pn transistor in EPIC integrated circuit current gain on 6th HTTP (base diffusion) regiments. 1 - 800°C, 2 - 900°C, 3 - 1000°C, 4 - 1100°C, 5 - 1200°C

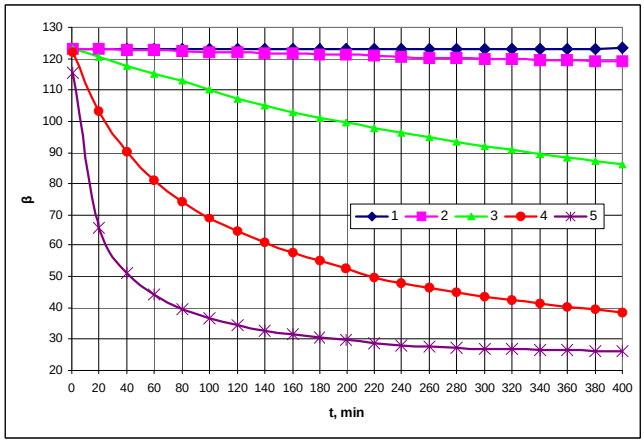

Fig. 5. The dependence of n^+pn transistor in EPIC integrated circuit current gain on 9th HTTP (emitter diffusion) regiments. 1 - 800°C, 2 - 900°C, 3 - 1000°C, 4 - 1100°C, 5 - 1200°C

After analyzing the influence of EPIC integrated circuits HTTP to α and β we can say, that first base diffusion stage is enough to form base layer, and other distribution of dopants can be performed by HTTP after that, so thinner ω can be gained, and by this – higher α and β. In common case from Fig. 4. and Fig. 5. we can tell that high temperature strongly influences transistor structures, formed in IC, so modeling is essential before beginning the manufacturing of such IC, to detect TP interconnections, influence, to decrease manufacturing and exploitation errors. Of course, active experiment is needed to evaluate the influence of each HTTP to formed or needed out coming parameters. Such experiment would be time and money consuming, because IC manufacturing cycle and its HTTP has a few incoming parameters, also such model would be of high volume. To add, such model (as well as the one, created in this paper) would be selective, i.e. suitable only for selected integrated circuit technology.

Conclusions

1. Areas formed in diffusion of EPIC technology integrated circuit redistribute after each high temperature technological process and by this change the depths of layers formed. The structures formed mostly change after HTTP with temperature T>1100°C.

2. The hidden n^+ layer formed in EPIC technology, as HTTP regiments are stable, mostly change 80,7% in forming isolating oxide (third HTTP), 15,3% - forming epitaxy layer (fourth HTTP), 14,8% - forming base layer (6-th HTTP).

3. The depth of base layer p formed in EPIC technology, as HTTP regiments are stable, mostly change 72,3% forming emitter layer with diffusion (8-th HTTP) and 46,9% forming oxide (9-th HTTP).

4. Performing modeling of diffusing layers redistribution in EPIC technology integrated circuit, deduced that "hidden" n^+ layer redistribution in manufacturing cycle can cover base p area, causing irreparable manufacturing error.

5. After analyzing n^+pn transistor current gains α and β dependence on HTTP regiments, deducted that α and β decreases as TP time and temperature increases.

6. After analyzing n^+pn transistor current gains α and β dependence on high temperature technological processes, deducted that performing technological processes in temperature range from 800°C to 1000°C current gains α and β change little, maximum β variation can reach 18,6%, bigger variation is noticed in temperature range 1000°C – 1200°C, where β variation can reach 83,3%.

7. To reach as big as possible α and β, time and temperature of 6^{th} – 9^{th} HTTP must be decreased. But these parameters of technological processes depend on other layers formed, such as oxide and epitaxy layer.

8. To ensure as small as possible redistribution of diffusion layers, and by this better values of α and β, high temperature processes must be accelerated or changed with low temperature processes – performed oxidation in wet oxygen or perform pyrolisis, the growth of epitaxy layer perform in the way of molecular epitaxy, perform ion implantation for emitter diffusion.

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EPIC technology is used for specialized IC formatting on the ground of transistor structures. The change of structure in IC manufacturing cycle is mostly determined by high temperature technological processes (HTTP) regiments, which influence diffuse layer dopant redistribution, and by this determine characteristics and manufacturing errors of elements formed. Main regiments of HTTP are considered time for structure formatting and technological process (TP) temperature. The main goal is to analyze and model the cycle of HTTP used in EPIC technology and their influence to ach other and current gain α and β. Ill. 5, bibl. 8 (in English; summaries in English, Russian, Lithuanian).

В. Кашаускас, Р. Анилёнис, Д. Эйдукас. Моделирование производственных процессов в EPIC технологии // Электроника и электротехника. – Каунас: Технология, 2008. – № 7(87). – С. 49–52.

Технология ЭПИК применяется для формирования специализированных биполярных интегральных микросхем (ИМ). В технологическом процессе изготовления ИМ на транзисторные структуры наиболее влияние оказывют высокотемпературные процессы (ВТП), влияющие на перераспределение диффузионных слоев. Основные параметры ВПТ – время и температура технологического процесса. Цель работы исследовать и смоделировать влияние ВПТ друг на друга, а также определить изменения коэффициентов усиления по току α и β. Ил. 5, библ. 8 (на английском языке; рефераты на английском, русском и литовском яз.).

V. Kašauskas, R. Anilionis, D. Eidukas. Gamybinių EPIC technologijos procesų modeliavimas // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2008. –Nr. 7(87). – P. 49–52.

EPIC technologija taikoma specializuotiems MG formuoti bipolių tranzistorinių struktūrų pagrindu. MG gamybos maršrute struktūrų pokyčius labiausiai lemia aukštos temperatūros technologinių procesų (ATTP) režimai, kurie turi įtakos difuzinių sluoksnių priemaišų persiskirstymams, o kartu ir formuojamų elementų charakteristikoms bei gamybos defektams. Pagrindiniais ATTP režimais laikomi struktūros formavimo trukmė ir technologinio proceso (TP) temperatūra. Pagrindinis darbo tikslas – ištirti ir sumodeliuoti EPIC gamyboje naudojamų aukštos temperatūros technologinių procesų (ATTP) seką ir įtaką vienas kitam bei α ir β stiprinimo koeficientams. Il. 5, bibl. 8 (anglų kalba; santraukos anglų rusų ir lietuvių k.).