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Investigation of Etching Process in Nano Structures

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Introduction

Integral circuit (IC) and their elements must be released with high precision.

The IC made modern day information processing and communications systems possible. It's basic functional element is the transistor, most commonly a silicon metal oxide semiconductor field-effect transistor (MOSFET). In MOS/CMOS structures regions between the active elements must be isolated [1].

After a photo mask has been created a layer under the resist is etching. A large etch rate is like advantage in technological process [2]. Too high an etch rate is treat like lack, because it is difficult to control etching process. Etch process rate can reach hundreds nanometers per minute by common way.

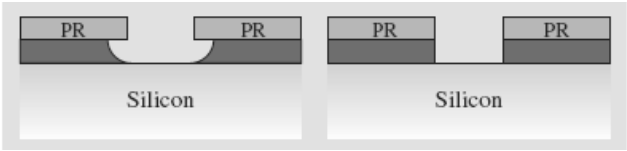
Every technological process related with past one (for example: diffusion depends on wafer (crystal lattice) quality, which depends on technological process temperature) [3]. That's why etching process is important to IC formation. Choosing correct type of etch is possible to avoid disasters like: undesirable dislocations, bird's beak (in thermal oxidation).

Very-large-scale integration (VLSI)

VLSI is the process of creating integrated circuits by combining thousands of transistor-based circuits into a single chip [4]. The microprocessor is a VLSI device. The term is no longer as common as it once was, as chips have increased in complexity into the hundreds of millions of transistors. The first semiconductor chips held one transistor each. Subsequent advances added more and more transistors, and as a consequence more individual functions or systems were integrated over time. The first integrated circuits held only a few devices, perhaps as many as ten diodes, transistors, resistors and capacitors, making it possible to fabricate one or more logic gates on a single device. Now known retrospectively as "small-scale integration" (SSI), improvements in technique led to devices with hundreds of logic gates, known as large-scale integration (LSI), i.e. systems with at least a thousand logic gates. Current technology has moved far past this mark and today's microprocessors have many millions of gates and hundreds of millions of individual transistors.

Billion-transistor processors are commercially available.

Thin film and bulk substrate etching is fabricationstep that is of fundamental importance to both VLSI processes and micro/nanofabrication. In the VLSI area, various conducting and dielectric thin films deposited for passivation or masking purposes must be removed at some point or another. In micro/nanofabrication, in addition to thin film etching, very often the substrate also needs to be removed in order to create various mechanical micro-/nanostructures. Two important figures of merit for any etching process are selectivity and directionality. Selectivity is the degree to which the etchant can differentiate between the masking layer and the layer to be etched. Directionality has to do with the etch profile under the mask. In an isotropic etch, the etchant attacks the material in all directions at the same rate, creating a semicircular profile under the mask, Fig. 1a. In an anisotropic etch, the dissolution rate depends on specific directions, and one can obtain straight sidewalls or other noncircular profiles, Fig. 1b.



a) b)

Fig. 1. Etch through a photoresist (PR) mask: a – isotropic etching is independent of the plan the crystal; b – anisotropic etching is dependent on the plane of orientation [4]

Also it is possible divide the various etching techniques into wet and dry categories.

Wet Etching

Wet etchants are by and large isotropic and show superior selectivity to the masking layer compared to various dry techniques. In addition, due to the lateral undercut, the minimum feature achievable with wet etchants is limited. Silicon dioxide is commonly etched in a dilute. Photoresist and silicon nitride are the two most common masking materials for the wet oxide etch. Nitride wet etch is not very common, due to the masking difficulty and unrepeatable etch rates.

Anisotropic and isotropic wet etching of crystalline and non-crystalline substrates are important topics in micro/nanofabrication.

For short etch times, silicon dioxide can be used as the masking material. However, one needs to use silicon nitride if a longer etch time is desired.

Dry Etching

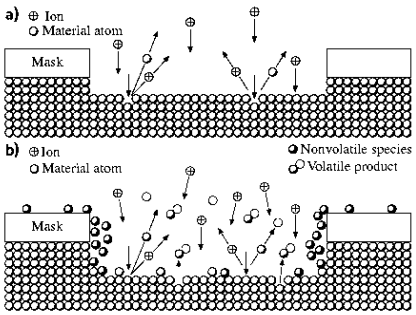
Most dry etching techniques are plasma-based. They have several advantages compared with wet etching. These include smaller undercut (allowing smaller lines to be patterned) and higher anisotropicity (allowing high-aspect-ratio vertical structures). However, the selectivity of dry etching techniques is lower than the wet etchants, and one must take into account the finite etch rate of the masking materials.

The three basic dry etching techniques, namely, high-pressure plasma etching, reactive ion etching (RIE), and ion milling utilize different mechanisms to obtain directionality.

Ion milling is a purely physical process that utilizes accelerated inert ions striking perpendicular to the surface to remove the material Fig. 2a. The main characteristics of this technique are very low etch rates (on the order of a few nanometers per minute) and poor selectivity (close to 1:1 for most materials); hence it is generally used to etch very thin layers.

High-pressure plasma. In high-pressure plasma etchers, highly reactive species are created that react with the material to be etched. The products of the reaction are volatile, so that they diffuse away and new material is exposed to the reactive species. Directionality can be achieved, if desired, with the sidewall passivation technique (Fig. 2b). In this technique, nonvolatile species produced in the chamber deposit and passivate the surfaces. The deposit can only be removed by physical collision with incident ions. Because the movement of the ions has a vertical directionality, the deposit is removed mainly at the horizontal surfaces, while the vertical walls remain passivated. In this fashion, the vertical etch rate becomes much higher than the lateral one.

The RIE etching, also called ion-assisted etching, is a combination of physical and chemical processes. In this technique, the reactive species react with the material only when the surfaces are "activated" by the collision of incident ions from the plasma (e.g., by breaking bonds at the surface). As in the previous technique, the directionality of the ion's velocity produces many more collisions in the horizontal surfaces than in the walls, thus generating faster etching rates in the vertical direction (Fig. 2c).



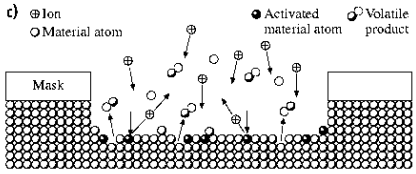


Fig. 2. Simplified representation of etching mechanisms for: a – ion milling; b – high-pressure plasma etching; c – RIE

MOS technological process

To improve MOS structure parameters parasitic capacities: gate-source, gate-drain has to be returned to minimum [3]. In order to reduce parasitic capacities we must avoid lateral diffusion, the size of gate electrode must be the same during all technological processes in order to avoid source-drain channel shortening. The area of element formation must be the same during all technological processes. Separation of MOS elements can be produced using local oxidation [5] and silicon on sapphire technologies.

Thermical grown silicon oxide separates semiconductor elements. It is necessary to get hole with less lateral etched side wall. The lateral oxidation can be formed during local oxidation. Therefore length of the source-drain channel decreases, because source and drain regions can be moved under the gate. A large attention must be paid to this process.

Silicon on Sapphire (SOS) technology have recently attracted more and more interest in the development of next-generation high-performance VLSI circuits and systems. The absence of latch-up, the reduced parasitic capacitance, the transparency of the substrate, the isolation and multi-threshold devices are just a few of the advantages of this technology.

Silicon on sapphire is an integrated circuit manufacturing technology. It is a hetero-epitaxial process that consists of a thin layer of silicon grown on a sapphire (Al_2O_3) wafer and this epitaxial layer etching (Fig. 3) [3].

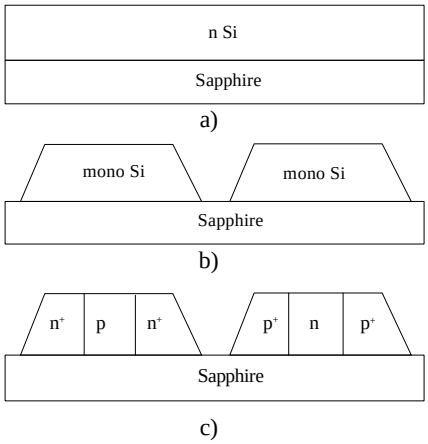


Fig. 3. SOS technology: a – epitaxial of silicon; b – separated regions of silicon creation; c – formation of NMOP and PMOP transistors

Created silicon regions are isolated by wafer from bottom and from the side by air space. It is necessary to avoid lateral encroachment during region formation,

because “active” length of region can be reduced, where transistors are formed.

MOS transistor characterized by the output characteristic ($I_D(U_{DS})$). It is connected by common-source scheme. The inversion layer charge density varies in the channel between the source and the drain from 0 to L, channel voltage varies from 0 to U_{DS}:

$$\int_0^L I_D dy = -\mu C_{ox} B \int_0^{V_{SI}} (U_{GS} - U_S - U_C - U_T) dU_C, \quad (1)$$

$$I_D = -\mu C_{ox} \frac{B}{L}((U_{GS} - U_T)U_{DS} - \frac{U_{DS}^2}{2}), \text{ when } U_{DS} < U_{GS} - U_T, \quad (2)$$

where μ – the mobility, cm^2/V; C_{ox} – capacitance per unit area, μF; B – gate width , nm; L – gate length , nm; U_{GS} – gate-source voltage, V; U_S – drain-source voltage, V; U_C – inversion channel voltage, V; U_T – threshold voltage, V. Output current direct proportional channel length (2nd formula). In this we got, that decreases channel length increases escarpment of transistor output characteristics, threshold voltage and drain current.

Process simulation

Etch process is simulated with ATHENA. ATHENA is a simulator that provides general capabilities for numerical, physically – based, two – dimensional simulation of semiconductor processing.

The ELITE module of ATHENA allows the use of sophisticated models for etch process. This process is modeled by defining a machine and invoking the machine to perform etch [6].

For all models except Monte Carlo Etching, ELITE uses a string algorithm to describe topographical changes that occur during etching process.

As micro/nanofabrication technology becomes more complex, modeling each step of the manufacturing process is increasingly important for predicting the performance of the technology.

Etching is a step that is universal in micro/nanofabrication. It may take place as the dissolution of a photoresist by an organic solvent, the etching of an oxide by an alkali, or the plasma etching of an electron resist. Whatever its physical details, the etching process can in many cases be modeled as a surface etching phenomenon. Etching simulation starts from an initial profile that moves through a medium in which the speed of etching propagation can be a function of position and other variables that determine the final profile.

Main task of etching process simulation is avoid lateral encroachment during region formation. Ideal structure is shown in Fig. 4.

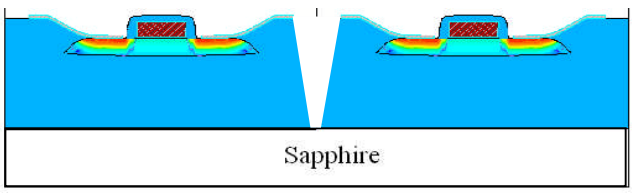
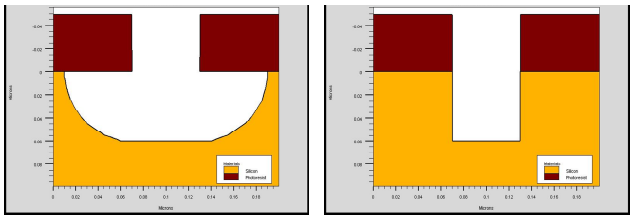


Fig. 4. Silicon on sapphire technology

Wet Etching can provide a higher degree of selectivity than dry etching techniques. In isotropic etching (Fig. 5a) materials are removed uniformly from all directions and it is independent of the plane of orientation of the silicon (crystal lattice). Anisotropic etching presents the opposite behavior of isotropic etching. Anisotropic etchants remove materials based on the crystal plane and do not etch uniformly in all directions (Fig. 5b)



a) b)

Fig. 5. Wet etching types: a – isotropic etch; b – anisotropic etch

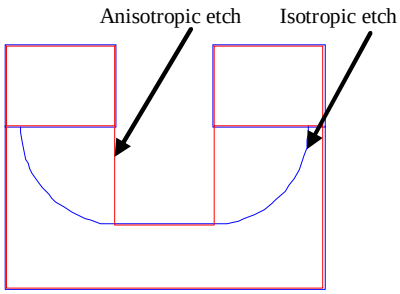
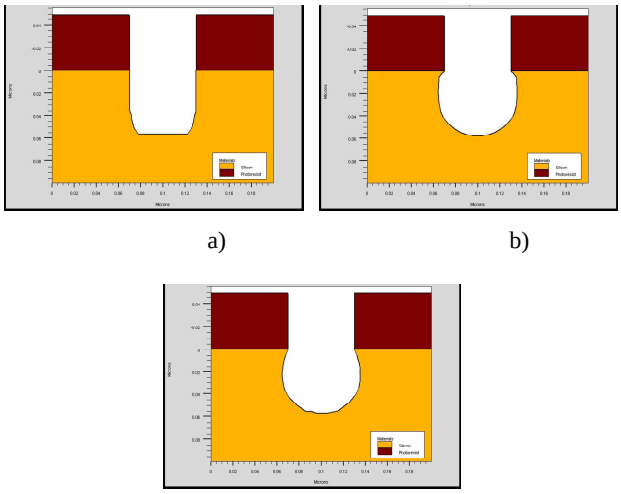


Fig. 6. Comparison wet etching types: blue line – isotropic; red line – anisotropic

Anisotropic etching solves the problem of lateral control. The laterally masked geometry of the planar surface can be etched and a vertical profile can be easily made. Although it solves the problem of lateral etching, the process is not problem-free. The process is slow even in the fast etching direction of the plane (100) and consumes more time.

Despite its simplicity in controlling the etching, wet etching is not flexible and reliable process. A dry etching process is an alternative choise (Fig. 7)



a) b)

c)

Fig. 7. Dry etching types: a – ion milling etch, b – high-pressure plasma etch, c – RIE etch

Dry Etching has several significant advantages compared with wet etching: it is much easier to start and stop than simple immersion wet etching; less undercutting; better process control. Ion milling (Fig. 7) has two significant advantages compared to high–pressure plasmas: directionality and applicability. With RIE can be achieved much higher selectivity compared with with ion milling.

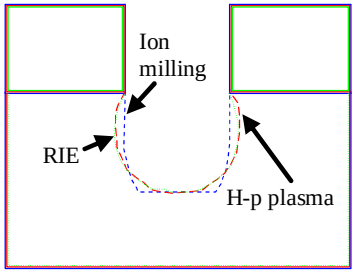


Fig. 8. Comparison dry etching types: blue line – ion milling; red line – plasma, green line – RIE

According to wet and dry etching process simulation results less lateral encroachment during region formation could be achieved using dry etching technology – ion milling. It has better directionality.

Conclusion

1. Unavoidable problems associated with wet etching process are: difficulties in etching at convex corners; difficult in preparing the mask with high precision; etch rate is very sensitive, it difficult to control both lateral and vertical geometries of the structure.

2. Using Dry Etching: it is possible to get less undercutting; better process control, directionality (Ion milling).

3. Less lateral encroachment could be achieved using dry etching technology – ion milling during region formation in MOS/CMOS technology.

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Problems of etching process, related with MOS transistors separation in SOS technologys was researched. Wet Etching provide a higher degree of selectivity than dry etching techniques. In isotropic etching materials are removed uniformly from all directions. A vertical profile can be easily made using anisotropic etching and it solves the problem of lateral etching. Using dry etching it is much easier to start and stop than simple immersion wet etching and less lateral encroachment is achieved. The main avantage of ion milling is directionality. That's why less lateral encroachment during region formation could be achieved using ion milling according to wet and dry etching process simulation results. Ill. 8, bibl. 6 (in English; summaries in English, Russian and Lithuanian).

Д. Андрюкайтис, Р. Анилёнис. Исследование травления в наноструктурах // Электроника и электротехника. – Каунас: Технология, 2008. – № 6(86). – С. 77–80.

Исследованы проблемы, связанные с отделением транзисторов в технологии КНС. "Мокрое" травление обеспечивает более высокую селективность по сравнению с сухим травлением. Изотропное травление обеспечивает равномерное удаление материала во всех направлениях. Вертикальное травление с минимальным боковым подтравливанием технологией анизотропного травления применяя "сухое" травление. Моделированием процесса ионного травленния онределено минимальное боковое подтравление. Ил. 8, библ. 6 (на английском языке; рефераты на английском, русском и литовском,).

D. Andriukaitis, R. Anilionis. Ėsdinimo proceso nanostruktūrose tyrimas // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2008. – Nr. 6(86). – P. 77–80.

Išnagrinėtos ėsdinimo problemos, susijusios su MOP tranzistorių atskyrimu SAS technologijoje. "Šlapiasis" ėsdinimas užtikrina didesnį selektyvumą nei „sausojo" ėsdinimo technologija. Taikant izotropinę ėsdinimo technologiją, ėsdinamoji medžiaga visomis kryptimis pašalinama vienodai. Vertikalusis ėsdinimas gali būti pasiektas taikant anizotropinę ėsdinimo technologiją. Tai išsprendžia šoninio paėsdinimo problemą. Tačiau lengviau kontroliuoti patį ėsdinimo procesą ir mažesnis šoninis paėsdinimas gali būti pasiektas ėsdinant „sausai". Mažiausias šoninis paėsdinimas pasiektas joniniu ėsdinimu, remiantis modeliavimo metu gautais rezultatais. Il. 8, bibl. 6 (anglų kalba; santraukos anglų, rusų ir lietuvių k.).