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Investigation of Digital Signal Processing for Measurement of Dynamic Parameters of High-Speed DAC's

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Introduction

Development and modern IC industry is improving resolution and speed of modern DACs and ADC [1-4]. Specialized test equipment is necessary to perform quality acceptance of such DACs [5-8]. Measurement of dynamic parameters and especially measurement of DAC settling time parameter becomes rather complex task with increasing resolution and speed of modern DACs [7].

Settling time of high-speed DAC is measured as a difference between time moment when value of test pulse sent to all information inputs of DAC under test reaches 0.5 level of its magnitude and the moment when difference of the signal level of DAC output and settled value of DAC output signal (U^1 and U^0) is not exceeding defined value (usually ± 0.5; 1; 2; … of Least Significant Bit – LSB).Start moment of the settling time measurement is the same as in any measurement of dynamic parameters and is easily obtained. End point moment of the settling time measurement is set when the level of the DAC output signal is higher (or lower) than the level of the settled signal by

$$U_{\mathrm{A}} = \frac{U_{\mathrm{DAC}} \cdot k}{2^{\mathrm{n}}}, \qquad (1)$$

where $U_{\mathrm{DAC}} = U_1 - U_0$ – magnitude of DAC output signal, k – readout level factor in LSB units (e.g., 0.5; 1;…), n – number of bits of DAC (resolution).

In case of 12-bit resolution DAC and standard output signal magnitude of 1 V, readout levels (at 0.5 LSB) according to (1) are U_{A} = 122 μV. It is obvious that in nanosecond range measurement of end point moment of settling time in such low voltage range is complicated.

Device of settling time measurement that converts measurement signal to a digital array and send it to PC for further processing has been developed and investigated by authors [7]. Together with the device the algorithm of digital signal processing has been developed and described. Nevertheless efficiency and limit cases of the digital processing algorithm have not been investigated by that time due to lack of the working digital model of input signal and digital signal processing algorithm.

With the improved resolution and speed of modern DACs it became necessary to perform more thorough investigation of the device.

Plan of the digital signal processing efficiency investigation

It has been shown that major problems of settling time measurement of high-speed DACs occurs because of very small readout levels when it becomes very difficult to distinguish signal under investigation from background noise [7]. Therefore the objective of the investigation of efficiency is to establish how much is it possible to increase reliability of the settling time measurement by using the developed digital signal processing algorithm on the digital array of the investigation signal.

Plan of the investigation is set as following:

- Develop model of DAC output signal without noise for definition of settling time reference value;
- Develop digital model of noises instabilities and drifts of sampling converter;
- Develop possibilities to change parameters of noise instabilities and drifts in order to evaluate different measurement situations and conditions;
- Implement digital signal processing algorithm into software program. Ensure possibilities to change parameters of the algorithm for the investigation of how these parameters are influencing result of settling time measurement;
- Investigate different situations with various parameters of sampling converter noises and instabilities by changing digital signal processing algorithm parameters the way that the inaccuracies are not exceeding target values;
- Determine limit cases of the digital signal processing algorithm and highest possible resolution of DACs that can be investigated for settling times using hardware developed.

LabView® software package is selected for implementation of the plan because of its agility, simplicity and possibility to provide results in convenient and visual manner.

Digital model of the DAC output signal

Digital model of DAC output signal must have possibility to change parameters of the signal. It is constructed in order to have reference value of settling time measured under conditions with no external influence of sampling converter. Having this value it is possible to evaluate efficiency of the digital signal processing algorithm by comparing sampling time measurement results.

Digital model is developed using mathematic model of the DAC output signal [9]:

$$S(t) = S_{st}(t) + Ae^{-\beta t}\sin(\omega t + \varphi), \quad (2)$$

where $S_{st}(t)$ – square test pulse, A – magnitude of settling signal drop-outs, β – fade factor of settling oscillation, ω – angular frequency of settling oscillation; φ – initial phase.

Signal after sampling converter is usually reversed in time axis [7]. Therefore it is more convenient to reverse signal model as well to use the same settling time measurement algorithm.

Output signal model is developed as LabView Virtual Instrument (VI). Result of this model is a digital array of DAC output signal without influence of noises and drifts of sampling converter.

Model developed allows changing of signal parameters and enables possibility to model output signals of various DACs. After that required readout levels are set according to the DAC modelled and reference settling time is calculated.

Model parameters are chosen to represent the most problematic case for investigation – settling oscillations of the modelled DAC output signal is fading relatively slowly and the oscillation signal after settling time capturing moment is near to readout levels. In this case even small noises or drifts of signal value cause significant errors of settling time measurement. Most of modern high-speed and high resolutions DACs have very short settling oscillation fading time. Usually not more than 2 periods of settling oscillation are observed and therefore settling time measurement with real modern DACs would be more accurate than case modelled.

Model of Sampling Converter (SC) internal noises drifts and instabilities

In order to model signal received from sampling converter to a PC it is necessary to develop a model of sampling converter internal noises instabilities and drifts. Model of sampling converter influence should include [7]: a) instability of the start moment of the converted signal; b) instability of the settled value of the signal and c) noises of the SC.

Because of real time scale transformation processes in SC, such as instability of the formation of sampling signal, start times of output signal realizations are different. Therefore it becomes difficult to calculate average values of the different realizations and calculate start moment of the settling time measurement. This results in errors of settling time measurement. Such instabilities are modelled by using random shift of samples in digital array of the signal (shift of start time). Possibility to change maximum shift value (amplitude) is implemented into VI front panel for easy control during investigations.

Because of drifts and errors of levelling circuits in the SC instabilities of signal settled value level occur. Such instabilities are modelled by random shift of signal zero value (shift of value of all momentary values in the digital array). Initial and maximum values of the amplitude shift can be set on the VI panel for easy control during investigations.

Internal noises of the SC are modelled by Gaussian white noise. Amplitude of the noise is controlled from the VI panel. Sample values of white noise are added to DAC output signal model array.

Digital signal processing algorithm is based on processing of several (up to hundreds) of signal realizations; digital model of SC output signal is developed to generate different realizations of the output signal. All the realizations are stored in two-dimension digital array.

Gaussian white noise, settled value and time instabilities are observed in the graphic representation of the two-dimension array of the SC output signal.

Graphic representation of single realization of the SC output signal model is represented in Fig. 1.

It is obvious from Fig. 1 that with the defined readout levels it is not possible to measure settling time of DAC. Therefore digital signal processing should be applied to realizations of the SC output signal.

Digital signal processing

Realizations of the SC output signal are processed by the developed LabView VI which is applying procedures set in [7]: a) initial filtering of the signal; b) synchronization of the signal realizations in time axis; c) levelling of the signal zero values to coincidence settled values of the signal; d) calculation of the averaged signal realization; e) calculation of the settled value; f) set up of readout levels; g) calculation of the settling time measurement start moment; h) calculation of the settling time measurement end moment; i) calculation of the settling time and comparison with the settling time measurement value of the signal without SC noises and instabilities applied. The above-mentioned procedures are implemented as following:

a) Initial filtering of signal after SC is not implemented in this phase of the investigations.

b) Starting moments of signal realizations are different and therefore it would cause averaging errors and as a consequence errors in settling time measurement. In order to avoid such errors starting moments of the realizations are synchronized by determining edge of the pulse in each realization. Then each edge is analyzed for the fastest rise moment and the number of sample of this particular moment is captured. Difference of number of sample and standard number of sample of fastest rise of the input signal is a correction factor. After that time axis of each realization is shifted to the defined correction factor synchronizing each realization in time axis.

c) In order to avoid settling time measurement errors because of instability of the settled value of each realization it is necessary to equalize settled values of all realizations to a standard value. For this purpose time frame (100 samples) of the signal in the area of the settled

signal is extracted and the average of the frame values is calculated. Obtained average is compared to the standard value and correction factor is calculated and signal values are shifted by correction factor. After this procedure settled signal value of all the realizations are at the same standard level.

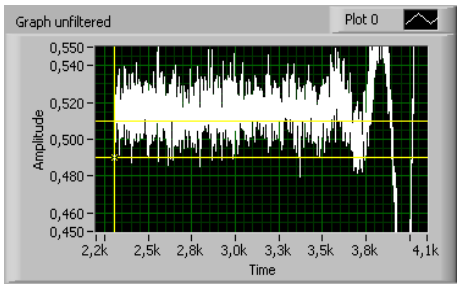

Fig. 1. Graphic representation of the single realization of the SC output signal with noises and instabilities model

d) Average of each sample out of all realizations is then calculated and single dimension of processed SC signal array is obtained.

Averaging of samples of the signal realizations ensure decrease of the influence of random errors (internal noise) to the measurement result. Mean square deviation of the noise voltage code value after averaging is

$$n_{trv}^2 = \frac{n_{tr}^2}{\sqrt{v}}, \tag{3}$$

where n_{tr}^2 – mean square instability of the output signal code caused by random noise, v – number of signal realizations averaged;

Therefore by averaging samples of signal realizations it is possible to reduce influence of the random errors.

After averaging of 50 realizations of the SC signal resulting single dimension array is represented graphically in Fig. 2. It is obvious that the noise level is significantly lower than one observed in Fig. 1 and it does not exceed readout levels. Measurement of settling time can be performed with necessary accuracy level.

e) Settled value of the averaged signal $n^{1(0)}$ is obtained the same way as in step c as after averaging it can be slightly shifted.

f) Codes of readout levels' values are calculated

$$n_{\text{A}} = \pm 2^{(\text{n}-\text{m})} k \frac{U_{\text{DAC}} K_{\text{SC}}}{U_{\text{ADC}}} + n^{1(0)}, \tag{4}$$

where m – number of ADC bits, U_{DAC} – magnitude of ADC input signal; K_{SC} – transfer ratio of the SC.

g) Values of the samples of averaged signals are compared to the readout level codes (4). At the time moment with sample number d_{p} when code of particular sample is exceeding upper or lower readout level start of settling time measurement is set.

h) Number of last signal sample d_{g} is obtained. Because of time shift in step b number of last sample can slightly differ between realizations. Therefore average value is obtained.

i) Number of samples between settling time measurement start and end samples $d_{\text{NT}} = d_{\text{g}} - d_{\text{p}}$, is

j) Obtained and DAC settling time is calculated

$$t_{\text{NT}} = d_{\text{NT}} \frac{(f_1 - f_2)}{f_{\text{ADC}} f_1}, \tag{5}$$

where t_{NT} – DAC settling time; f_1 and f_2 – frequencies of the sample step formation oscillators, f_{ADC} –ADC sampling frequency.

Calculated value is indicated on the screen and compared to the reference settling time value.

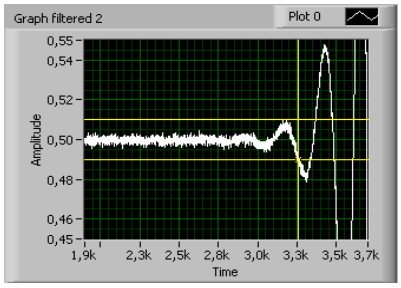

Fig. 2. Graphic representation of the SC signal after digital signal processing

Results of the investigations

LabView® Virtual Instruments is developed to unify all the investigation plan steps to a single investigation management system. It is possible to change any necessary parameter including parameters of noise and instabilities and the number of realizations to be averaged easily in this system during the investigation. It is possible to perform huge number of measurements simulations and perform statistical analysis of the results obtaining reliable results about the efficiency of the digital signal processing algorithm.

It was established that even without initial filtration of the SC signal (step a) digital signal processing algorithm is removes time and settled value instabilities and reduces influence of the internal noises of SC effectively. It has been established that increasing the influence of the SC internal noises it is necessary to increase the number of realizations processed to keep accuracy level on the required value. Dependence of the accuracy to the number of realizations processed and amplitude of Sc internal noise is presented on Fig. 3.

It is established that with setting particular amplitude of the SC noise by adding additional signal realizations at some point a rapid decrease of maximum error is observed because of chosen DAC signal model which is the most problematic for settling time measurement. It is established that for real conditions of 12 bit resolution DAC ($U_{\text{tr}} \leq 0.8$ U_{A}) 15 – 20 realisations of the SC signal is enough to obtain inaccuracy level as low as 3 %. It has been established that even in case SC noise level is exceeding readout levels by 4 times it is still possible to achieve the same level of maximum errors 3 %. For this case it is necessary to process at least 500 realizations of SC output signal. Therefore the tester developed equipped with the developed digital signal processing algorithm is capable of measuring settling time 14 bit resolution DACs with readout levels set to ± 0.5 LSB.

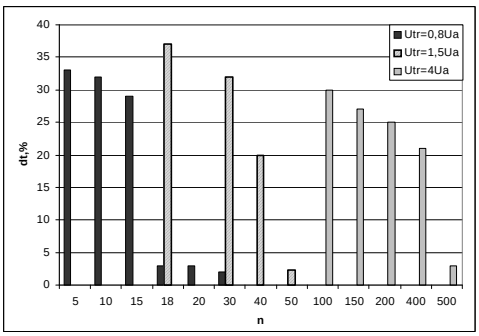

Fig. 3. Dependence of the maximum measurement errors to realizations processed and amplitude of SC noise

Conclusions

1. LabView® Virtual Instruments has been developed for the investigation of the DAC settling time measurement digital processing algorithm.

2. The VI created is capable of working in DAC settling time measurement system measuring settling times of 12 – 14 bit resolution DACs with slight changes, using real SC output signal instead of the signal models created for investigations.

3. It is established that with the hardware developed [3] and taking into account obtained noise levels and instabilities it is possible to achieve maximum measurement inaccuracy at 3 % level for 12 – 14 bit resolution DACs while setting readout levels to 0.5 LSB. Only 10 bit resolution DACs could be measured by using this hardware until now.

4. It has been established that in case the noise levels are high it is necessary to process huge number of signal realizations. Implementation using LabView package does not allow efficient usage of CPU power and therefore it takes comparably long time (processing of 500 realizations takes approx. 30 minutes). Therefore further investigations are planned to decrease need of processing of huge number of realizations and improve speed of processing by using initial signal filtering, improving processing algorithm and hardware of the tester.

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Developed LabView Virtual Instrument (VI) for digital signal processing of sampling converter signal for measurement of serttling times of high-speed high resolution DACs is presented. Investigations performed by setting DAC output signal parameters set to noise level to 0.8 of readout levels (exceeding values of 12 bit resolutions DACs with 0.5 LSB readout levels) and also by setting noise level voltage to 4 LSB (exceeding noise level of real testers for 14 bit DACs). Investigations have shown that it is possible to achieve 3 % maximum inaccuracy by processing 15 realizations of 12 bit DAC signals and 500 realizations of 14 bit DAC signals. Ill. 3, bibl. 9 (in English; abstracts in Lithuanian, English, Russian).

Р. Квядарас, В. Квядарас. Измерение динамических параметров быстродействующих многоразрядных ЦАП // Электроника и электротехника. – Каунас: Технология, 2008. – № 3(83) . – С. 11–14.

Представлена программа генерирования цифрового массива исследуемых сигналов, их цифровой обработки и измерения времени установления многоразрядных быстродействующих ЦАП. Для исследований были генерированы массивы с уровнем белого шума равным 0,8 МЗР (что больше чем в реальных измерителях 12 разрядных ЦАП) и уровнем белого шума равным 4 МЗР (что больше чем в реальных измерителях 14 разрядных ЦАП). Погрешность измерения времени установления не превышает 3 % при цифровой обработке 15 реализации исследуемого сигнала 12 разрядных и 500 реализации исследуемого сигнала 14 разрядных ЦАП. Ил. 3, библ. 9 (на английском языке; рефераты на литовском, английском и русском яз.).

R. Kvedaras, V. Kvedaras. Sparčiųjų SAK dinaminių parametrų matavimo skaitmeninio signalų apdorojimo tyrimas // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2008. – Nr. 3(83). P. 11–14.

Pristatoma tiriamųjų signalų skaitmeninio modelio generavimo, jų skaitmeninio apdorojimo ir nusistovėjimo trukmės matavimo programa, skirta sparčiųjų daugelio skilčių SAK automatizuoto nusistovėjimo trukmėms matuoti. Tyrimams buvo generuoti SAK išėjimo impulsų skaitmeniniai masyvai, turintys 0,8 MRS signalo nusistovėjusio lygio nestabilumus (tai didesnė kaip realių 12 skilčių SAK matuoklių išėjimo signalų, nustačius 0,5 MRS atskaitos lygius triukšmų vertė) ir 4 MRS (tai didesnis kaip realiuose matuokliuose triukšmo lygis matuojant 14 skilčių SAK). Nustatyta, kad matavimo paklaida neviršija 3 %, kada apdorojama 15 tiriamųjų 12 skilčių SAK signalų ir 500 tiriamųjų 14 skilčių SAK signalų. Il. 3, bibl. 9 (anglų kalba; santraukos lietuvių, anglų ir rusų k.).