ELECTRONICS AND ELECTRICAL ENGINEERING

ISSN 1392 – 1215 *2008. No. 2(82)*

ELEKTRONIKA IR ELEKTROTECHNIKA

T170 *ELECTRONICS* / *ELEKTRONIKA*

Measurement of swtitching losses in power transistor structure

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Introduction

Increasing the efficiency and power density is nowadays main criterion in designing the power converters. This means contradictory tendencies because increasing the power density is realized by increasing the switching frequency, what results in increase of commutation losses. Just switching losses of switching element (power transistor) are main part of total losses generated during operation of power converter. The solution how to eliminate these switching losses is usage of soft-switching techniques that are realized by auxiliary circuit, or more perfectly, by utilization of parasitic elements of main circuit. There is statement that each type of switching technique is not suitable for each type of transistor, therefore an experiments have to be made to choose the best solution. Standard progress expects measuring prototype or in better case on physical converter model. Potential change of main circuit parameters is technically difficult and introduces additional cost of equipment´s development.

Power circuit and its configuration

Measuring of switching losses is realized by using well-known circuit that is shown in Fig. 1. This circuit serves only for measurement in hard-switching mode of power transistor.

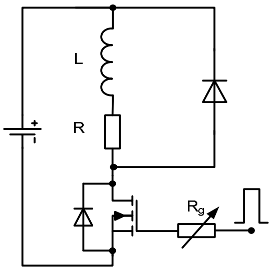

Fig. 1. Hard - switching test circuit

Therefore the need of emulation of various switching techniques (hard switching, ZVS, ZCS) lead us to construct a testing device, whose construction is realized as circuit with variable topology specific for each technique. Using this resolution it is possible to measure the losses generated by semiconductor devices during various commutation modes. In connection with switching losses it is important to have knowledge about energy that is stored in internal capacitances of power transistor (MOSFET, IGBT). This energy to a great degree has influence on turn – on losses, so special mode of measuring the internal capacitance is included.

Principle schematic of testing device is shown in Fig.2. Primary requirement was to gain exact emulation of different soft–switching techniques and consecutive interpretation of generated switching loss. Proposed topology of main circuit is modificated by additional circuits, which serves to realize required commutation technique (hard switching, ZVS, ZCS).

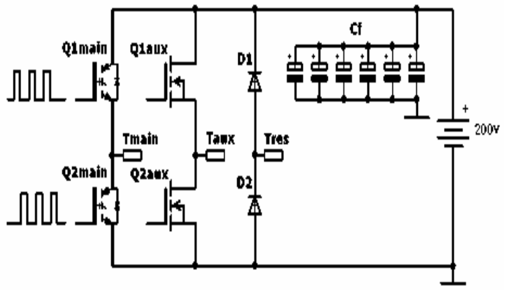

Fig. 2. Proposed circuit of testing device

Generator of gate impulses has to have ability of optional and gently–adjustable deadtime. Measuring of losses generated by semiconductor device, the method of calculation the instantaneous power is being used [2]. Construction of whole testing device has been issued from requirement of its application like teaching instrument (understanding of processes of semiconductor devices during various commutation techniques) and also as research instrument for choosing the optimal switching technique characterized by minimal losses of semiconductor device.

Control circuit and user interface

The main control unit of universal testing device is Freescale 56F8013. This DSC (Digital Signal Controller) is member of 56F800/E core-based family. It combines processing power of a DSP and functionality of microcontroller. Freescale 56F8013 is 16b DSC and includes many peripherals that are useful in industrial control and general purpose inverters.

Primary function of DSC is generating sequence of pulses for switching the controller in switching modes and for measuring the Wcap. Another function of DSC is communication with user and LCD display.

Communication with user is performed through 3 pushbuttons and reset button. One of three pushbuttons is used for setting the mode of operation (Hard, ZVS, ZCS, Wcap) and two others are used for setting the deadtime – up, down. The mode settings are made by external interrupts requests in DSC. After setting of mode, the deadtime is set to maximum value due to ensure safety conditions. The series of pulses starts when the DOWN button is pushed. Frequency of PWM modulators in DSC is 96 MHz so the finest step of deadtime can be set to approx. 10ns (1/96MHz).

All information about current switching mode and deadtime settings are displayed on 2 line matrix LCD. Because of LCD uses parallel communication and DSC has limited number of GPIO pins, the shift register between DSC and LCD is connected. DSC communicates with shift register through SPI protocol (serial communication). Block diagram of control circuit is shown in Fig. 6.

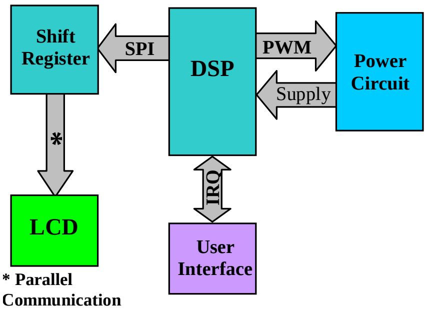

Fig. 3. Block diagram of control circuit

Experimental results

Before experiments of switching modes were realized the measurement of Wcap was made whereby MOSFET type of power transistor was used (SPP17N80C3).

After measured waveforms are being obtained (Fig. 4.1, Fig. 4.2) an exact value of internal capacitance of power transistor is able to be calculated. Because measured data (current, voltage) from oscilloscope mostly aren't in continuous form (1), it is necessary to use a discrete form of this equation as shown in expression (2).

$$W = \int_{t_1}^{t_2} i_P(t).u_P(t)dt \qquad (1)$$

$$W = \sum_{i=T_{Z1}}^{T_{Z2}} I_P[i].U_P[i].\Delta T\,, \qquad (2)$$

where T_{z1} – sequence of sample at the begin of process (turn – on/off, charging - disgarching, stabilized conductivity/non-conductivity of device); T_{z2} – sequence of sample at the end of process (turn – on/off, charging - disgarching, stabilized conductivity/non-conductivity of device); $I_P[i]$ – i-sample of current through device; $U_P[i]$ – i-sample of device's voltage; ΔT – sampling time.

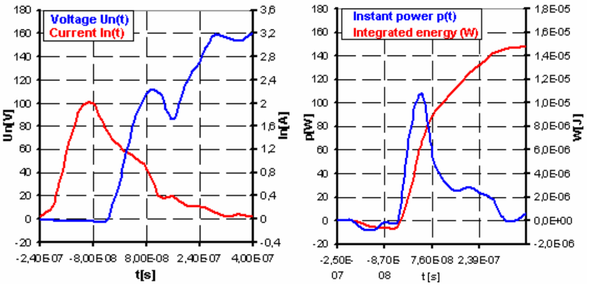

Fig. 4. Charging interval of internal capacitance (left) and instant power and absorbed energy of internal capacitance(right) of MOSFET SPP17N80C3

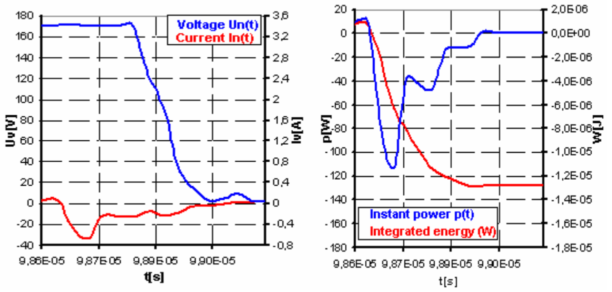

Fig. 5. Discharging interval of internal capacitance (left) and instant power and absorbed energy of internal capacitance (right) of MOSFET SPP17N80C3

It can be seen (Fig. 4, Fig. 5), that values of integrated energy of Coss are in big rate same when to compare charging and discharging interval. It is the evidence that this energy is recuperative. This energy has a huge impact on turn - on process (HS, ZCS) during which it is absorbed in body of power transistor.

After measurement were realized using equation (3) a real value of Coss was calculated. Table 1 shows values of calculated and value that is introduced by manufacturer.

$$W_{CAP} = \frac{1}{2} C_{OSS} \cdot U_{DS}^2 \Rightarrow C_{OSS} = \frac{2.W_{CAP}}{U_{DS}^2}\,. \qquad (3)$$

Table 1. Calculated and manufacturer introduced of Coss

(SPP17N80C3)	CALCULATED	MANUFACTURER
Voltage (V)	180	170
Coss (pF)	969	1500

Hard switching technique was measured using configuration of testing device shown in Fig. 1. Accordingly ZVS and ZCS mode were realized using unified topology of testing device. All measurements were realized at 50 kHz of switching frequency. During hard switching a variable parameter should be gate resistance, which value was set to 22Ω. Variable parameter during ZCS is gate resistance, which value was also 22Ω and dead – time, which value was set to 1,25us. During ZVS variable parameters are gate resistance (22Ω), dead – time (1,25us) and output capacitance C_{oss} (5nF). Supply voltage was set to U_{DS} = 200 V with load current I_D = 10A.

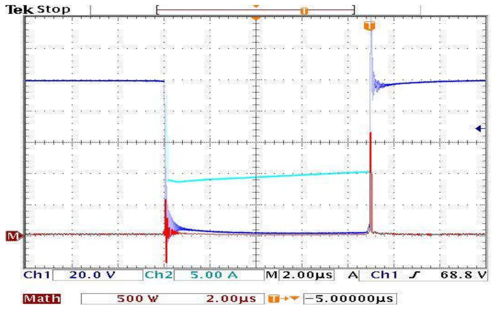

Fig. 6. Measured waveforms of voltage, current and instant power of MOSFET (SPP17N80C3) – hard switching

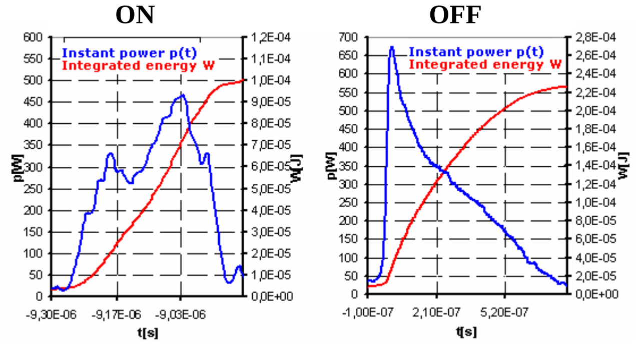

Fig. 7. Instant power and integrated energy – hard switching

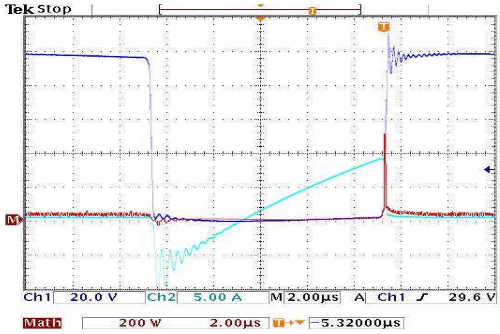

Fig. 8. Measured waveforms of voltage, current and instant power of MOSFET (SPP17N80C3) – ZVS

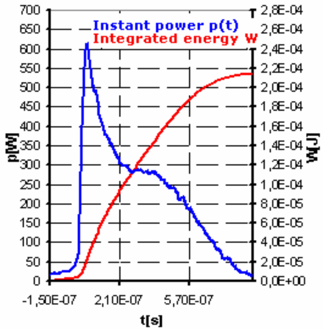

Fig. 9. Instant power and integrated energy – ZVS turn–off

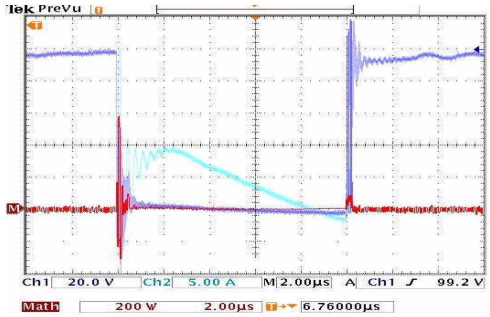

Fig. 10. Measured waveforms of voltage, current and instant power of MOSFET (SPP17N80C3) – ZCS

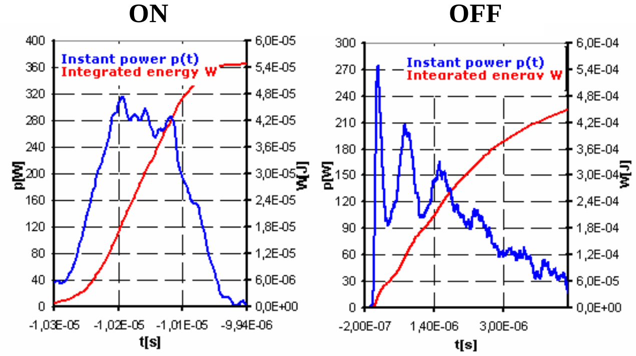

Fig. 11. Instant power and integrated energy – ZCS

After measurements have benn realized, calculation of power loss should be done. Most of data that are available from oscilloscope for calculation are in discrete form, so then it is also necessary to use equations in form (2), instead of (1) [5]. Table 2 show results of calculation of power loss during turn–on and turn–off during HS, ZVS and ZCS of SPP17N80C3.

$$P_{TOT}=\frac{1}{T}W_{CON}+\frac{1}{T}W_{ON}+\frac{1}{T}W_{TOFF}+\frac{1}{T}W_{OFF}, \qquad (4)$$

where P_{TOT} – total power loss during switching cycle; W_{CON} – conduction energy losses; W_{ON} – energy losses generated during turn–on process; W_{TOFF} – energy losses generated during turn–off process; W_{OFF} – energy losses generated during stabilized off state; T – time period of computed action.

For calculating the apportionable parts of expression (4) next equations have to be used.

$$W_{CON}=W_{OFF}=\int_{t_1}^{t_2}u_P(t).i_P(t)dt=U_T\int_{t_1}^{t_2}i_P\,dt+R_D\int_{t_1}^{t_2}i_P^{\,2}\,dt, \qquad (5)$$

where U_T – transistor's threshold voltage; I_P – time function of current flowing through the transistor; R_D – internal resistance of transistor; $t1$ – initial time of stabilized conductivity/non-conductivity of device; $t2$ – final time of stabilized conductivity/non–conductivity of device.

$$W_{ON}=W_{TOFF}=\int_{t_1}^{t_2}i_P(t).u_P(t)dt, \qquad (6)$$

where i_P – time function of device's current; u_P – time function of device's voltage; $t1$ – initial time of turn – on/off process; $t2$ – final time of turn – on/off process.

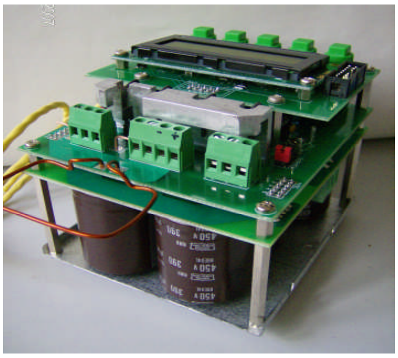

Fig. 12. Physical model of testing device

Table 2. Calculated power loss during hard–switching technique

	17N80C3		
Ploss (W)	PON	POFF	PTOT
HS	5	11,25	16,25
ZVS	—	10,75	10,75
ZCS	2,7	22,5	25,2

Table 2 shows that during hard-switching mode (Fig. 6, Fig. 7) the power transistor have generated the most amount of power loss. This is the fact of that Wcap has not been removed from body of transistor before it has turned-on and neither snubber capacitor was added to reduce the du/dt of transistor during turn-off process. Different situation happen during ZVS mode (Fig. 8, Fig.9). Before transistor had turned-on, the energy Wcap has been removed from transistor into power circuit. This effect significantly reduce total losses of transistor, where turn - off losses become dominant part of total losses. Turn - off losses should be also reduced using snubber circuit (external capacitor). The worst case for chosen transistor was ZCS mode (Fig. 10, Fig. 11), where turn-off losses become dominant part of total loss. This should be caused because of existence of post-commutating impulse after transistor has turned-off.

This experiment shows that for chosen conditions the ZVS mode is the best solution to obtain the most favourable switching performance for MOSFET SPP17N80C3.

Conclusion

Advantage of mentioned methods is possibility of determining commutation losses in semiconductor structure during specific commutation method. Designed testing device is characterized by simply variation of topology, that enables emulation of various commutation techniques and subsequently obtain information about commutation process. Mentioned knowledge is taking advantage in optimizing method of converter´s efficiency

Acknowledgement

The authors wish to thank for the financial support to Scientific Grant Agency of the Slovak Republic for the VEGA Project No. 1/3086/06, “Research of the new methods of modelling, control and simulation of mechatronic systems”, and also “Intelligent device for giguecycle fatigue test of construction materials which are being used in the field of ultrasonic frequencies”, APVV Project No.20-051705

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Submitted for publication 2007 10 10

P. Špánik, B. Dobrucký, M. Frívaldský, P. Drgoňa, I. Kurytnik. Experimental Analysis of Commutation Process of Power Semiconductor Transistor’s Structures // Electronics and Electrical Engineering. – Kaunas: Technologija, 2008. – No.2(82). – P. 75–78.

Testing device designed for experimental examination of processes in power electronics devices during various switching modes is described. Through the use of auxiliary circuits additional switching modes (ZVS, ZCS) are realized except hard switching, and turning-off with reduced current respectively. The device’s advantage is possibility of fine dead time setting, allowing us analyzing effects of this phenomenon on measurements of commutation losses. Ill. 12, bibl. 10 (in English; summaries in English, Russian and Lithuanian).

П. Шпаник, Б. Добруцки, М. Фривалдски, П. Дргона, И. Курытник. Экспериментальный анализ процесса коммутации мощных полупроводниковых транзисторных структур // Электроника и электротехника. – Каунас: Технология, 2008. – No. 2(82). – С. 75–78.

Описано испытание устройства, разработанного для экспериментальной экспертизы процессов в мощных электронных устройствах в течение различных способов коммутации. С помощью вспомогательных цепей разработаны дополнительные способы переключения (ZVS, ZCS), кроме твердого переключения и выключения с уменьшенным потоком. Преимущество устройства – возможность регулирования времени коммутации. Это разрешает анализировать потери коммутации. Ил. 12, библ. 10 (на английском языке; рефераты на английском, русском и литовском яз.).

P. Špánik, B. Dobrucký, M. Frívaldský, P. Drgoňa, I. Kurytnik. Galingų puslaidininkinių tranzistorių struktūrų komutavimo procesų eksperimentinė analizė // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2008. – Nr. 2(82). – P. 75–78.

Aprašomas prietaisas, skirtas galinguose elektroniniuose įrenginiuose vykstantiems procesams eksperimentiškai tirti, esant skirtingiems komutavimo režimams. Panaudojus pagalbinius grandynus sukurti papildomi komutavimo režimai (ZVS, ZCS), išskyrus stipraus komutavimo ir išjungimo sumažinta srove. Prietaiso pranašumas – galimybė tiksliai nustatyti komutavimo trukmę. Tai leidžia analizuoti įvairių poveikių įtaką komutavimo nuostolių matavimams. Il. 12, bibl. 10 (anglų kalba; santraukos anglų, rusų ir lietuvių k.).

DOI: 10.5755/j02.eie.11059