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Principles of Operation of Three-level Phase Shift Controlled Converter

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Introduction

One of requirements for the next generation of power supplies in constant voltage source mode is to achieve high power density with high efficiency. In nowadays, at power level 5 – 10 kW and at input voltage level 1 kV, the DC/DC converters are usually implemented with a half-bridge or with full-bridge topologies using IGBT devices. One of the drawbacks that these converters present is to maintain ZVS for a wide load range, an additional resonant inductance must be included. This in turns increases the circulating energy, which increases the conduction losses in the converter. One of the disadvantages of this topology presents in high-voltage applications is that each switch in the full-bridge DC/DC converter is subjected to the full bus voltage. In this voltage range, MOSFET devices with a high R_{DSon} may be used. This approach increases the conduction losses of the DC/DC converter. Another option for this power range is to use IGBT devices, but these devices are not suitable for high switching frequency due to their bipolar structure. One of perspective solutions of this problem is using topology, which reduces the voltage stress across the power switches. If the secondary voltage level is low, (up to 100V) then is possible to use Schottky diodes, with excellent static and dynamic parameters. In this case all power semiconductor devices have unipolar structure, appropriate for high switching frequencies.

Three-level converters

The three-level topologies seen be most suitable for given input parameters (Fig.1). These types of DC/DC converters (called three level converter [1], [7]) reduce the voltage stress across the main devices to half the level of the input voltage, achieve ZVS for the primary switches, minimize the voltage imbalance problem across the input capacitors, under abnormal operating conditions, such as a mismatch of the gate signals [7]. Because of properties of these converters is possible to use Cool MOS transistors, as main switches, up to 1400 V of input voltage. For this voltage level would be applicable only IGBTs, in conventional topologies, with worst dynamical parameters.

It is possible to use different control algorithms for these converters, with constant or variable frequency. Using phase shift control improves the soft-switching characteristic of the converter by using ZVS or ZVZCS. The special half-bridge topology is shown in Fig. 1., and the operating waveforms in Fig. 2.

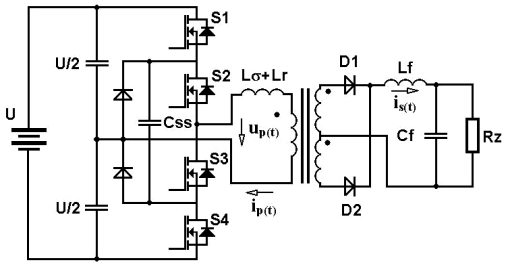

Fig. 1. Three-level phase shift controlled converter

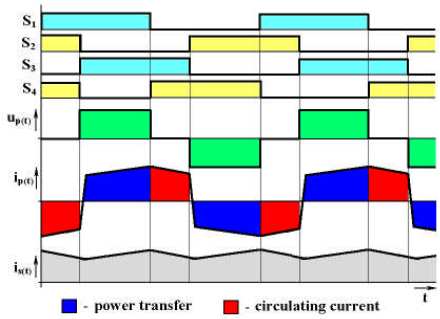

Fig. 2. Operating waveforms of three-level phase shift controlled converter

In this case, losses due to circulating energy in the freewheeling intervals can be reduced, by adding auxiliary circuits to the primary or secondary side of the converter. These modifications are not widely used in industrial applications, because they make the topology more complex. The advantages and disadvantages of this topology are similar, like of a traditional phase shifted full bridge topology [4], [7].

The resonant types, with variable - frequency control are similar to the traditional full-bridge resonant converters. Main advantages of resonant type three-level converters are eliminate problem of parasitic ringing on rectifier diodes, achieving ZVS at light load too, reducing the voltage stress across the power devices, using current driven rectifiers, with voltage filters only.

The specifications and requirements for the converter are as follows

U_{OUT} = 28 V ±2%; I_{OUT} = 200A; U_{IN} = 700 V ±10%. (1)

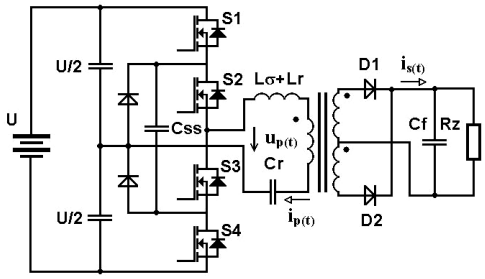

Fig. 3. Special half-bridge resonant converter

It is possible to achieve zero voltage switching (ZVS) of the main switches, above the resonant frequency of the converter by using series resonant circuit (Fig. 3.). When switching frequency is lower than resonant frequency, the converter can work under zero current switching (ZCS) condition. For power MOSFETs, the zero voltage switching method is preferred. The voltage gain characteristic of the series resonant circuit is shown in the Fig. 4., with parameters as follows: Lr = 18 µH, 120 nF, Q = {0,1264; 0,2532; 0,3804; 0,5051; 0,6341; 1,27; 1,9}.

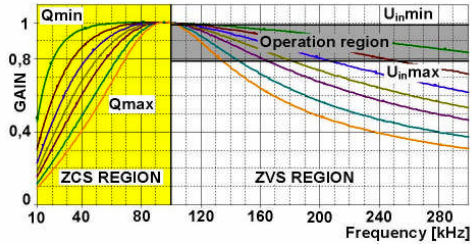

Fig. 4. DC characteristic of the series resonant circuit

It can be seen from the operating region that at light load, the switching frequency need to increase to very high to keep output voltage regulated. As input voltage increases, the converter is working at higher frequency. As frequency increases, the impedance of the resonant tank is increased. This means more energy is circulating in the resonant tank instead of transferred to output and conduction loss increase.

In the case of parallel resonant circuit achieving ZVS above the resonance is possible too and the needed frequency range for the given operating region is would be much smaller. The light load regulation problem is eliminated too. The voltage gain characteristic of the series resonant circuit is shown in the Fig. 5, with parameters as follows: Lr = 12 µH, 220 nF, Q = {19,73; 9,85; 6,56; 4,94; 3,93; 1,98; 1,31}. The problem of parallel resonant circuit is the low input impedance, which causes high amplitude of the primary current. It means higher circulating energy through that the frequency range is much smaller, and higher turn off currents for the primary switches. This turn off current can achieve usually higher values like in PWM converters.

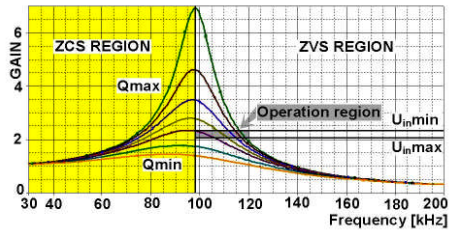

Fig. 5. DC characteristic of the parallel resonant circuit

By analysis of series and parallel resonant circuits the conclusion is that these resonant circuits cannot be optimized at given requirements for the converter. High conduction loss and switching loss will be resulted from wide input range. The series - parallel resonant circuits can combine the advantages of these basic resonant circuits [2].

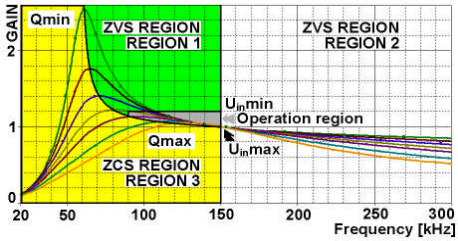

Fig. 6. DC characteristic of the CLL series - parallel resonant circuit

The voltage gain characteristic of the CLL series - parallel resonant circuit is shown in the Fig. 6., with parameters as follows: Lr = 10 µH, 110 nF, Lm = 35 µH, Q = {0,1165; 0,2333; 0,35; 0,4653; 0,5841; 1,16; 1,75} and the Bode plot of resonant circuit is shown in the Fig. 7. It can be seen that, there are two resonant frequencies and the higher is in the ZVS region, the lower is on the border of ZCS and ZVS regions. The higher resonant frequency is determined by resonant elements C_r and L_r and the higher is determined by resonant elements C_r and L_r+L_m. For a resonant converter, it is generally true that the converter reach high efficiency at resonant frequency. In the case of CLL resonant circuit the converter could be designed to operate around the higher resonant frequency or between these two resonant frequencies and could reach high efficiency.

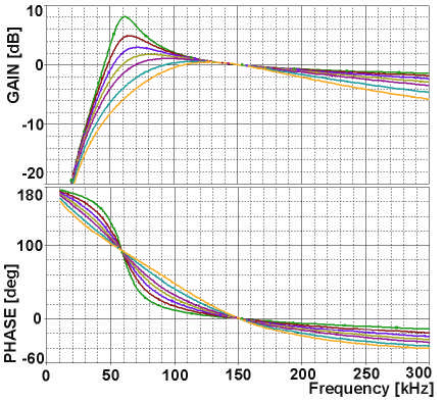

Fig. 7. Bode plot of the CLL series-parallel resonant circuit

Principle of operation of the converter

The converter has three operating regions as shown in Fig. 6. On the right side of higher resonant frequency the influence of SRC will dominant and the converter will have similar characteristics like SRC. On the left side of the higher resonant frequency at heavy load the SRC will dominant and as load get lighter the PRC will dominant. At appropriate design of resonant circuit it is possible to operate the converter on the left side of the higher resonant frequency at ZVS condition, therefore in region 1.

For simplification, in the explanation of the converter operation, it is considered that switches S_1 and S_2 or S_3 and S_4 are turned on and off simultaneously. However, it is required that a small delay be introduced into the operation between them.

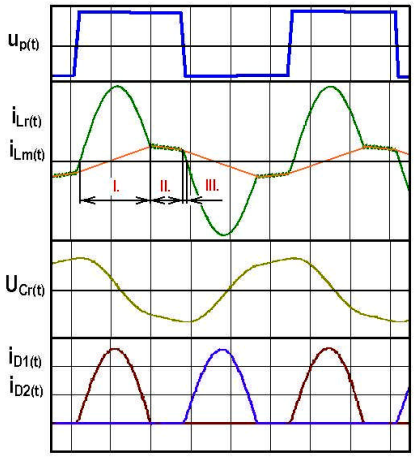

Fig. 8. Waveforms of the CLL series-parallel resonant converter in operation **region 1**, at full load

In region 1, each half of switching cycle can be divided in three intervals as shown in Fig. 8. Before the first interval begins, switches S_1 and S_2 are on, and the resonant inductor current flows through their anti-parallel diodes. The first interval begins when the primary current cross zero and the difference between half the input voltage and the reflected output voltage is applied across the resonant circuit. A resonance begins between series resonant capacitor C_r and series resonant inductor L_r. Magnetizing inductor Lm is not participates on resonance and magnetizing current is linearly charges. During this interval, the input power is delivered to the output. At the end of this interval the primary current level reaches the level of magnetizing current, and the second time interval begins. At the beginning of second time interval the resonant inductor current reaches the magnetizing current, causing the secondary side of the transformer to be disconnected from the primary side. A new resonance begins between magnetizing inductance L_m and resonant inductance L_r with resonant capacitor C_r. During this time interval the output current keeps zero, therefore the operating mode is discontinuous in this region. At the and of second and at the beginning of third time interval the switches S_1 and S_2 turn off just the magnetizing current, which reduces the turn-off losses. Also, this magnetising current, discharges the parasitic capacitances of S_3 and S_4 to zero, to turn on their anti-parallel diode, applying a negative voltage across the transformer. Since the anti-parallel diodes of S_3 and S_4 conduct the primary current, S_3 and S_4 can be turned on with ZVS. During this interval the secondary side remains disconnected, the resonance continues with the participation of magnetizing inductance L_m. At the end of this interval, primary current cross zero and a new half of a switching cycle begins.

When load becomes lighter, the voltage on resonant capacitor C_r will be lower when primary switches switched. Then secondary diodes will not conduct, the energy will flow back and forth from input, which means most of the current are circulating. This causes higher conduction loss at light load but it makes the converter operating with ZVS at very light loads.

In region 2, the converter works very similar to SRC. The natural resonant period of the resonant circuit is interrupted, because the switching frequency higher than the higher resonant frequency. The waveforms of the converter in this region are shown in Fig. 9. In this region, magnetizing inductance L_m never participates on resonance, it acts as the load of the series resonant circuit, this makes converter able to operate at no load condition without the penalty of very high switching frequency. In this region the output current is continuous, but at lighter loads, when the primary current level is near to the magnetising current converter operates in discontinuous mode. Because of reduced Lm value, the magnetising current is higher, here are more circulating current for CLL at light load compared with SRC. But the benefit is ZVS is ensured at light load condition.

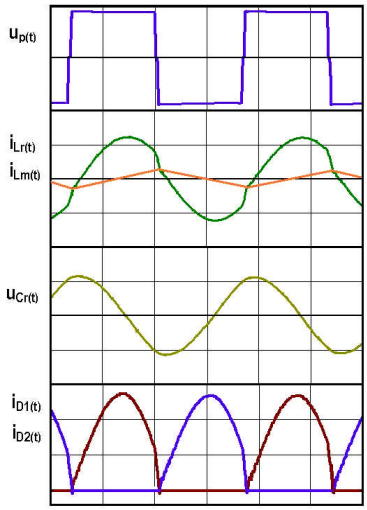

Fig. 9. Waveforms of the CLL series - parallel resonant converter in operation **region 3**, at full load

When the converter operating on the left side of higher switching frequency and the load becomes too heavy the converter will work in **region 3**. The waveforms of the converter in this region are shown in Fig. 10. When the converter is overloaded, the resonant capacitor voltage ripple is increased. If the energy stored in resonant capacitor Cr is high enough to make secondary diodes conduct, then the primary current resonates to the other direction, instead of clamping by magnetising current, at the end of resonance half-cycle. Region 3 is a ZCS region, for this converter, preferred operating regions are region 1

and region 2 in order to achieve ZVS. In the design, this mode should be prevented.

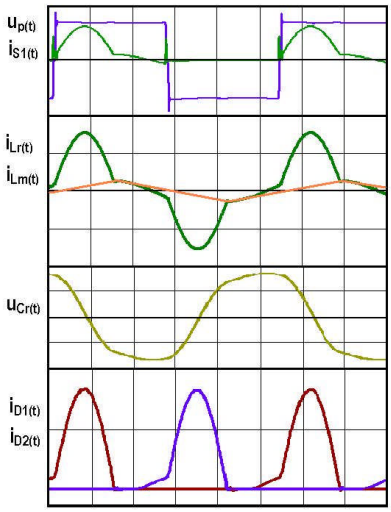

Fig. 10. Waveforms of the CLL series - parallel resonant converter in operation **region 2**, at full load

Simulation analysis of the converter

The required voltage gain (200 mV), for given input voltage variation can be set with suitable choice of magnetizing inductance of the transformer. At higher air gap lengths the DC gain will higher, but the magnetizing current of the transformer will higher too. There is a design trade of between the voltage gain (or narrower switching frequency range) and the magnetising current value.

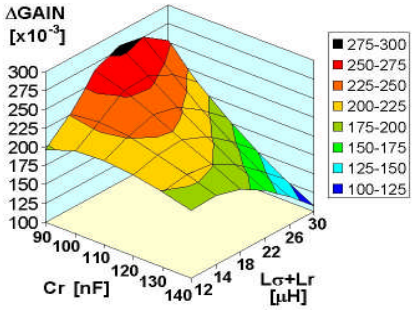

Fig. 11. Influence of resonant components on voltage gain

A typical characteristic of the influence of other resonant components on voltage gain is shown in Fig. 11. The characteristic was gained by simulation. The voltage gain difference was measured between voltage gain curves with load conditions R_Z = 135 mΩ and R_Z = 20 Ω, on a sine wave voltage fed resonant circuit at 80 μH of the magnetising inductance in 100 to 250 kHz frequency range. It can be seen that, the resonant capacitance value should be choose as small as possible to get enough voltage gain at heavy load, but this capacitance value must be enough to keep the converter operation in region 1, even at overload condition. The resonant inductor value should be chose as low as possible to get enough voltage gain at heavy load, because of conduction losses.

A simulation model was built to verify the operation and the relevant characteristics of the proposed converter, in simulation environment Orcad PSpice [5]. The main switches of the inverter were modelled with simulation models of 600 V, 43 A, 0,130 Ω MOSFETs APT6013B2FLL. The resonant circuit parameters were as follows: Cr=100nF, Lr=14μH, Lm = 55μH. The parallel resonant inductor model, Lm was created by adding gap to the ferromagnetic core model of the transformer. The model of center-taped transformer was based on a non-linear magnetic core model E65, EPCOS N97, with turns ratio equal to 10 and 13/1/1 turns in the primary and secondary, respectively [3]. Rectifier diode models were two Schottky diodes 180NQ045 in series, due to lack of limited model range in the used program. The simulation model of converter contained model of wires in each branches of the converter. Simulation model of the control circuit was proposed on the base of CD4046 IC enabling to generate signal with variable frequency. The control signals had constant dead times and variable pulse widths at variable frequency.

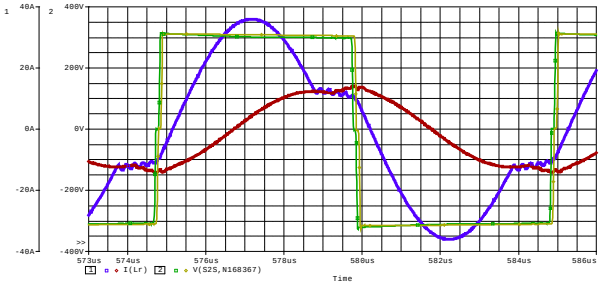

Fig. 12. Simulated waveforms of $\mathbf{u_{p(t)}}$ (**FULL LOAD**, **LIGHT LOAD**), and $\mathbf{i_{p(t)}}$ (**FULL LOAD**, **LIGHT LOAD**), at U_{in}=620 V, f_S =100 kHz

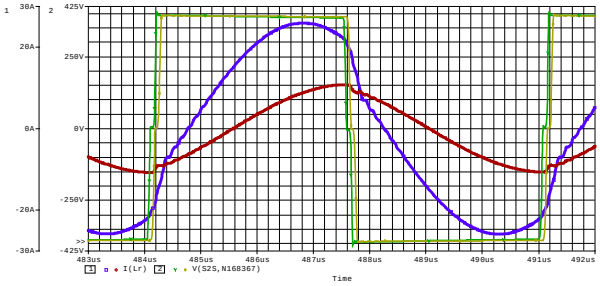

Fig. 13. Simulated waveforms of $\mathbf{u_{p(t)}}$ (**FULL LOAD**, **LIGHT LOAD**), and $\mathbf{i_{p(t)}}$ (**FULL LOAD**, **LIGHT LOAD**), at U_{in}=780 V, f_S =143,6 kHz

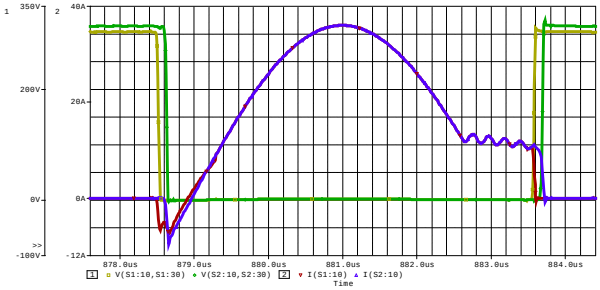

Fig. 14. Simulated waveforms of $i_{S1(t)}$, $i_{S2(t)}$ and the $u_{DS;S1(t)}$, $u_{DS;S2(t)}$ at U_{in} = 620 V, f_S =100 kHz (**FULL LOAD**)

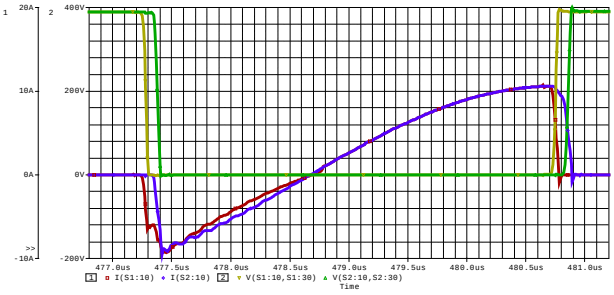

Fig. 15. Simulated waveforms of $i_{S1(t)}$, $i_{S2(t)}$ and the $u_{DS;S1(t)}$, $u_{DS;S2(t)}$ at U_{in} = 780 V, f_S =143,6 kHz (**LIGHT LOAD**)

Two extremes in operation conditions were investigated on proposed simulation model. The first extreme happens when the converter input voltage is at the minimum, at full load. Then the switching frequency is the lowest. The second extreme happens, when the input voltage is at the maximum, at light load. Then the switching frequency achieves the maximum. The converter was designed to work around the higher resonant frequency, f_H = 134,5 kHz.

In Fig. 12 and 13 the inverter part output voltages $u_{p(t)}$, and primary currents $i_{p(t)}$, are shown at full load (R_Z = 135 mΩ) and at light load (R_Z = 1 Ω) conditions at 620 V and at 780 V of input voltage. It can be seen that the shapes of the inverter part output voltage waveforms $\boldsymbol{u_{p(t)}}$ are nearly square wave, with nearly 50% duty cycle. The primary current $\boldsymbol{i_{p(t)}}$ at full load condition has quasi sine waveform, with amplitude 36,1A (at U_{IN} = 780V), and at light load it follows the magnetizing current. The converter works in region 1 at 620V of input voltage.

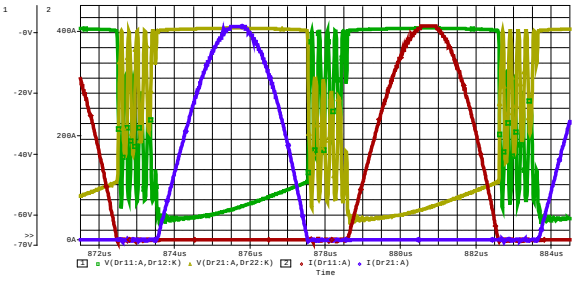

Fig. 16. Simulated waveforms of $i_{D1(t)}$, $i_{D2(t)}$ and the $u_{D1(t)}$, $u_{D2(t)}$ at U_{in} = 620 V, f_S =100 kHz (**FULL LOAD**)

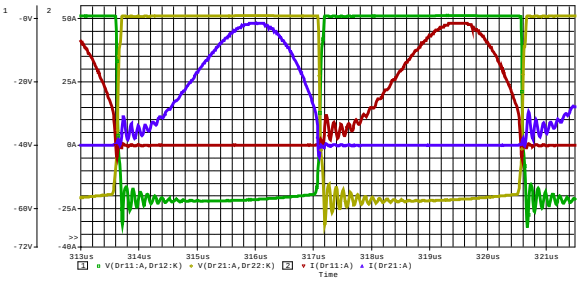

Fig. 17. Simulated waveforms of $i_{D1(t)}$, $i_{D2(t)}$ and the $u_{D1(t)}$, $u_{D2(t)}$ at U_{in} = 780 V, f_S =143,6 kHz (**LIGHT LOAD**)

In Fig. 14 and 15 the current and voltage waveforms of main transistors are shown at full load and at light load conditions. It can be seen that, the voltage stress of main switches is reduced to the half of the input voltage, and the waveforms do not contain sizable over-voltage oscillations. The main switches are turned on at real ZVS, and the turn off current is reduced to the value of magnetizing current (10,5A), what will reduce the turnoff losses.

The output rectifier diodes commutate naturally, and their voltage waveforms do not contain sizable over-voltage oscillations at turning off, as shown in Fig. 16 and 17. The maximum value of diode reverse voltage does not exceed 75V, without any snubber circuit. The maximum voltage drop on forward biased diodes was 1,54V (at I_{OUT} = 207A, U_{IN} = 620V), because in simulation model both were modelled with two Schottky diodes 180NQ045 in series because of limited part library of used simulation program.

Due to luck of this rectifier model the most part of power loss incurred in rectifier diodes, as shown in Fig. 18. Correct dimensioning of rectifier diodes could reduce these significant losses. The main part of this power loss is conduction loss. In Fig. 18 and 19 the power loss distribution is shown at full load and at light load conditions. The power loss distribution becomes homogenous at light loads.

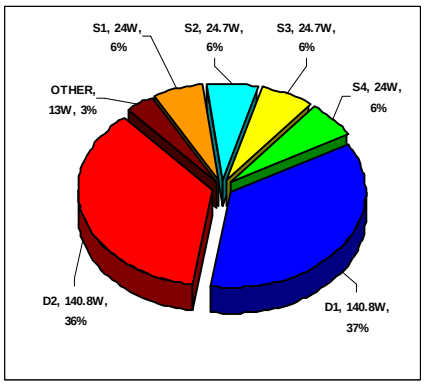

Fig. 18. Power loss distribution of the converter, at U_{in} = 620 V, f_S =100 kHz, P_{IN} = 6162W, P_{OUT} = 5770W, I_{OUT} = 206A, U_{OUT} = 28V, η = 93,4%

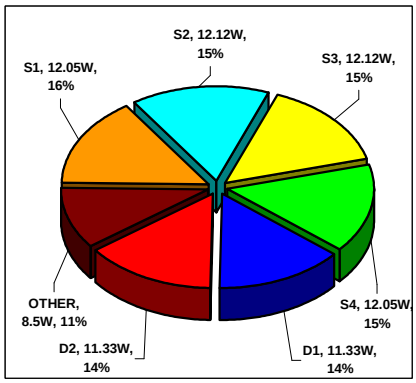

Fig. 19. Power loss distribution of the converter, at U_{in} = 780 V, f_S =143,6 kHz, P_{IN} = 870W, P_{OUT} = 790,5W, I_{OUT} = 28.1A, U_{OUT} = 28V, η = 90,86%

At efficiency determinations the input power was measured on the input voltage source and the output power on the load resistance. Fig. 20 shows simulated efficiency curves at different input voltage values and at constant

output voltage 28 V. The efficiency decreases as input voltage decreases. When input voltage decreases, the converter operates at lower switching frequency to compensate input voltage variation. In region 1 with decreasing switching frequency the circulating energy increases, resulting higher conduction losses. The efficiency of the converter at full load is around 93,5 % and is higher then 90 % even at light loads (above $I_{on}/10$).

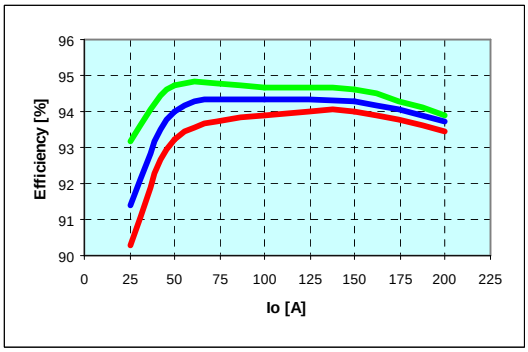

Fig. 20. Efficiency of the converter, at U_{OUT} = 28V, U_{in} = 780 V, U_{in} = 700 V, U_{in} = 620 V

Conclusions

It was shown that this converter works according to theoretical assumptions, on a detailed simulation model. The voltage stress of main switches is reduced to the half of the input voltage, the parasitic ringing on rectifier diodes is reduced, the main switches were turn on at ZVS for any load conditions and turned off at reduced (magnetizing) current. The converter achieves high efficiency (around 94%) at given input voltage variations and at wide range of load conditions. These characteristics make the proposed converter an interesting option for high voltage, middle power applications.

Acknowledgements

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A soft switching resonant DC/DC converter is presented in this paper. The converter is based on a three-level topology with Cool MOS transistors and uses variable frequency control. The principle of operation and some characteristics of the converter are analysed on a simulation model. Ill. 20, bibl. 8 (in English; summaries in English, Russian and Lithuanian).

Г. Кацсор, П. Шпаник, Я. Дудрик, М. Люфт, Э. Шихта. Принципы работы трехуровнего конвертера, контролируемого сдвигом фазы // Электроника и электротехника. – Каунас: Технология, 2008. – No. 2(82). – С. 69–74.

Анализируется плавно переключающий резонансный конвертер постоянного тока. Конвертер основан на топологии с тремя уровнями с «Cool» транзисторами МОП структуры и использует контроль переменной частоты. Принцип операции и некоторые особенности конвертера проанализированы используя имитационную модель. Ил. 20, библ. 8 (на английском языке; рефераты на английском, русском и литовском яз.).

G. Kácsor, P. Špánik, J. Dudrík, M. Luft, E. Szychta. Fazės poslinkiu valdomo trijų lygių keitiklio veikimo principai // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2008. – Nr. 2(82). – P. 69–74.

Analizuojamas tolygiai komutuojantis rezonansinis nuolatinės srovės keitiklis. Keitikli veikimas pagrįstas trijų lygių topologija, kurioje naudojami MOP struktūros „Cool“ tipo tranzistoriai. Keitiklyje naudojamas kintamo dažnio valdymas. Veikimo principas ir kai kurie keitiklio ypatumai analizuoti naudojant imitacinį modelį. Il. 20, bibl. 8 (anglų kalba; santraukos anglų, rusų ir lietuvių k.).

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