The 90 nm CMOS Charge Sensitive Preamplifier

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Introduction

The charge created by the interaction of the high energy particles in the sensor is very small and has to be amplified in a low-noise, very low power circuit before any further signal processing. The signal induced on the electrodes of the sensor is transferred to the readout chip, where it is integrated and amplified in a CSP. The preamplifier design is critical since it should match the detector interface. The circuit should be fast with low noise performance. The preamplifier output signal is in many cases amplified and shaped in a subsequent stage, called the shaper. In its simplest form it is constructed as a RC-CR filters that shapes the signal into a semi-Gaussian pulse form. The shaper optimizes the signal-to-noise ratio and band-limits the signal to remove low-frequency noise. But usually pulse shaping amplifier is not used to minimize power consumption [1].

The front-end chips are fabricated in state-of-the-art industrial silicon CMOS or GaAs MESFET processes [2]. This allows more logic to be introduced into a pixel or the use of a smaller pixel size. In particular, the low power and high integration of the CMOS 90 nm technology make it an attractive choice for the implementation of low noise front-end electronics in high resolution imaging detection systems.

With their small size and low cost, MEMS-micromachined inertial sensors have a wide range of applications in physics experiments, space, automotive, consumer electronics and biomedical areas. The design of CSP circuits with high sensitivity, low noise and large dynamic range is very important. These charge sensitive preamplifiers can be readily interfaced with MEMS–micromachined inertial accelerometers for converting the capacitance value to an output voltage for further signal processing and analysis [3].

This paper presents the design aspects for the high-speed, ultra-low power CMOS differential, cascade preamplifier (an outline specification is given in Table 1, together with preliminary simulated data) using 90 nm technologies. A description of the circuitry with high-value feedback device and the leakage current compensation circuits will be presented. The "charge to voltage" gain,

peaking time, noise simulations and descriptions of the actual circuit will also be presented.

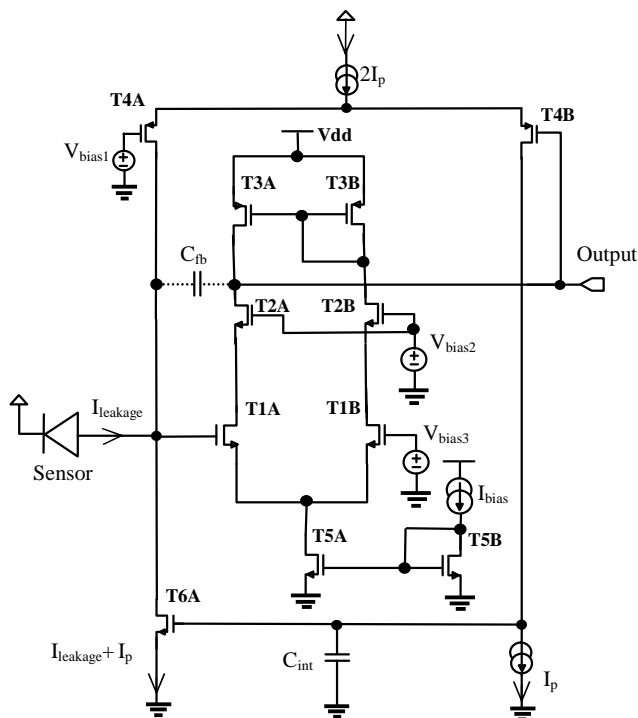### Design of the Charge Sensitive Preamplifier

Fig. 1. Simplified structure of a CMOS differential cascade amplifier with automatic current compensation

Fig. 1 shows the schematic of the simplified structure of a CMOS differential cascade charge sensitive preamplifier (CSP) with automatic current compensation. CSP consists of an operational amplifier with a feedback capacitor C_{fb} which is discharged by resistor R_{fb}, which is implemented by PMOS transistors (T4A and T4B) operating in the linear region. The capacitor C_{fb} is used to integrate the input signal, i.e. the voltage on C_{fb} which is proportional to the total charge pulse coming from the radiation sensor (1):

$$K \approx \frac{Q_{in}}{C_{fb}}, \qquad (1)$$

where K is the "charge to voltage" gain, Q_{in} is the input charge.

As can be seen from this equation, to get the biggest gain we should decrease the feedback capacitance. In our case, value of this capacitance is the sum of the transistors T1A, T2A parasitic capacitances and equal to 1 fF. The value of the feedback resistance R_{fb} is typically in the tens Megaohm range. In our case, this resistance is (2):

$$R_{fb} = \frac{1}{g_{mT2A}} + \frac{1}{g_{mT2B}} \approx 80 M\Omega, \qquad (2)$$

where g_{mT4A} and g_{mt4B} are common-source transconductances of transistors T4A and T4B. This configuration provides a constant current fast return to zero through the transistors T4A and T4B controlled by the $2I_p$ current. The complete bias current $2I_p$ is steered through T4B while the current through T4A is turned off. The input node is therefore discharged with a net current of I_p, independent of the leakage current I_{leak}. The current in the leakage compensation device T6A is regulated so that it equals $I_{leak} + I_p$ in the equilibrium state. The capacitor C_{int} plays a substantial role in the described leakage current compensation method. Its value has to be sufficiently high in order to prevent the circuit from oscillating. Positive leakage currents lower than $2I_p$ and negative currents lower than I_p can be compensated in each pixel. The idea for current compensation method lying at the background of this article had been scooped from [4].

The operational amplifier consists of a pair of n-channel transistors for the input T1A and T1B, driving a p-channel (T3A, T3B) current mirror stage as active load and a pair of n-channel cascade (T2A, T2B) transistors depress the Miller effect at the input and improve the gain factor of the amplifier. The Miller effect makes the input capacitance C_{in} seems significantly larger than just the capacitance C_{gs} (gate-source capacitance) of the input transistor T1A. C_{in} must be low, because it plays a crucial impact on the CSP peaking time, the signal-to-noise ratio and band-limits [5, 6].

The DC voltage gain of the operational amplifier is approximated by (3):

$$A_{DC} \approx \frac{-g_{mT1A}}{g_{dsT1A} \cdot \frac{g_{dsT2A}}{g_{mT2A}} + g_{dsT3A}}, \qquad (3)$$

where g_{mT1A} and g_{dsT1A} are the transconductance and the output conductance of the transistor T1A; g_{mT2A} and g_{dsT2A} of transistor T2A respectively, g_{dsT3A} is the output conductance of the active load transistor T3A. As can be seen from this equation, the DC voltage gain of the preamplifier is determined by not only the W/L ratios of the T1A, T3A transistors, but also by the ratio of the transconductance and the output conductance of the cascade T2A transistor. In our case, this ratio is (4):

$$\frac{g_{dsT2A}}{g_{mT2A}} << 1. \qquad (4)$$

The n-channel transistors T5A, T5B act as the tail current source pair. The transistor T5A is placed in a pixel CSP and the diode connected transistor T5B, which is biased by the output current of an 8-bit DAC, make together a current mirror. This circuit uses about 500 nA bias current I_{bias} from the V_{dd}=1 V power supply source and the total power P_{tot} of about 0.5 μW.

The cascade bias voltage V_{bias2} is generated locally in every pixel. It gives the possibility to disable the CSP in every pixel. The bias voltage denoted with V_{bias1} and V_{bias3} are generated by two 8-bit DAC converters, which is placed outside of the pixel matrix. The bias voltage V_{bias1} drive the transconductance of T4A, T4B transistors i.e. the feedback resistor R_{fb} (2). The bias voltage V_{bias2} sets the "zero" level of the output signal.

The noise performance of a sensor readout system is generally expressed as the equivalent noise charge (ENC) at the CSP input, usually expressed as the sum of the independent contributions [6, 7, 8]: leakage current contributions, thermal or Johnson noise (the following contributions belong to the parallel noise source), flicker (1/f), transistor channel noise and white noise contributions (belong to the serial noise source). It is well known, that the best input transistor width must exist for which the flicker (l/f) noise and the transistor channel noise contribution, is minimal. The best W depends of the flicker noise, the transistor channel noise with respect to the white noise [9]. The power consumption of the CSP must be kept very low in most applications in order to limit the heat dissipated in the very small active area of the sensor, and the cooling of electronics and sensor becomes difficult.

Considering very low power consumption of the differential, cascade preamplifier and the optimal flicker and transistor channel noise, the bias current I_{bias} have been fixed at 500 nA, when the input transistor gate width W is 450 nm.

The main design parameters are given in Table 1.

Table 1. Main simulated and design parameters of the preamplifier

Technology	90 nm CMOS
Power supply voltage V_{dd}	V_{dd}= +1 V
CSP bias current	I_{bias}= 0.5 μA
Leakage current compensation bias current $2I_p$	6 nA
Power consumption P_{CSP}	0.5 μA·1 V= 0.5 μW
Input transistor dimension T1A size	W/L= 450 nm/90 nm
Charge to voltage gain K	60…90 mV/kē
Peaking time τ_P	35...45 ns
Decay time τ_D	< 150 ns
Equivalent noise charge (ENC)	<160 ē
Feedback resistor R_{fb}	80…100 MΩ
Feedback capacitor C_{fb}	≈1 fF

Simulation results

The circuit was implemented with a 90 nm CMOS technology manufactured at IBM [10]. This technology allows us to implement both analog and digital circuits on the same substrate operating off a single V_{dd}=1 V supply. Computer simulation has been performed with the

Simulation Program with Integrated Circuit Emphasis (SPICE) simulator. The SPICE simulation of the preamplifier is performed using the BSIM4 model of this technology process. The U.C. Berkeley BSIM4 model is an industry-standard model for deep-submicron MOSFET analog and digital circuit design. The simulations were performed for one channel, includes the electrical model of the transmission line between the sensor and the CSP. In order to test the response of the CSP to an injected charge pulse, or a train of charge pulses, a known charge pulse was injected into the CSP. The simulation of the CSP is optimized for a CdZnTe sensor, because this material has the high atomic number and gives high detection efficiency relative to Si [11].

The output response for the CSP at the input charge equal 1 kē (160 aC), are presented in Fig. 2 for sensor capacitance C_{sen}=30 fF. The CSP output signal is a semi-Gaussian pulse form with an exponential a rise time constant and a decay long time constant.
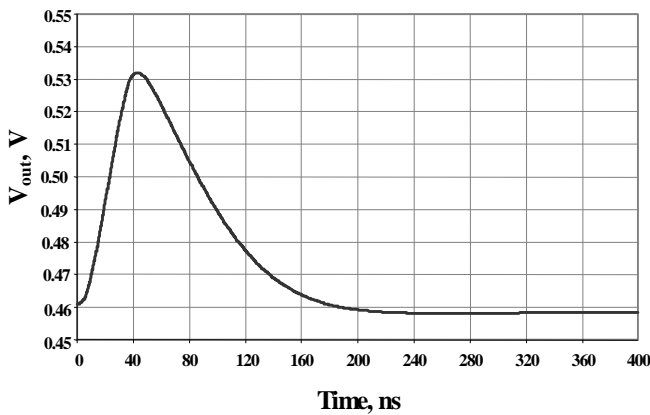

Fig. 2. Simulations of the CSP output waveform of injected charge (Q_{in}=1 kē, C_{sen}=30 fF, T=27 ℃, CdZnTe sensor)
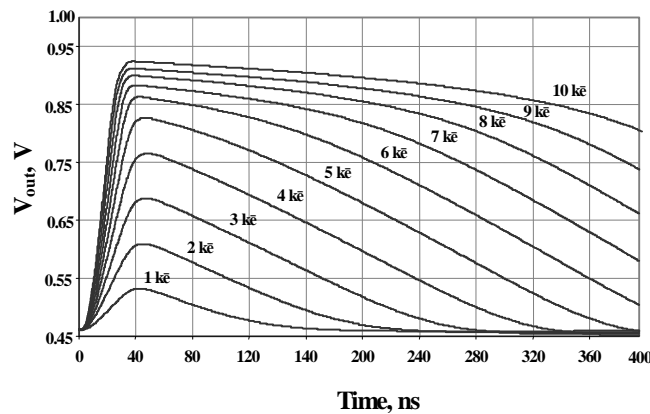

Fig. 3. Simulations of the CSP output waveform for ten values of injected charge (Input charge steps l kē…10 kē, C_{sen}=30 fF, T=27 ℃, CdZnTe sensor)

In Fig. 3 is shown the simulated response of the CSP when excited by a current impulse Q·δ(t) at the input. The input signals are charge steps 1 kē…10 kē with applied to a 30 fF capacitor at the preamplifier input. The preamplifier shows a good linearity up to 6 kē. The nonlinearity is less than 2 % for the output voltage of 0.8 V.
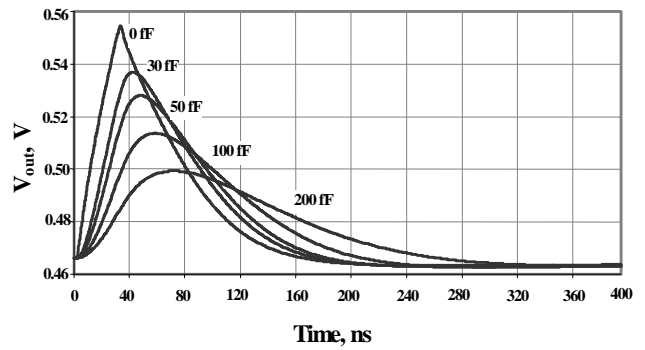

Fig. 4. Real signal response of the preamplifier for different input capacitance (Q_{in}=1 kē, T=27 ℃, CdZnTe sensor)
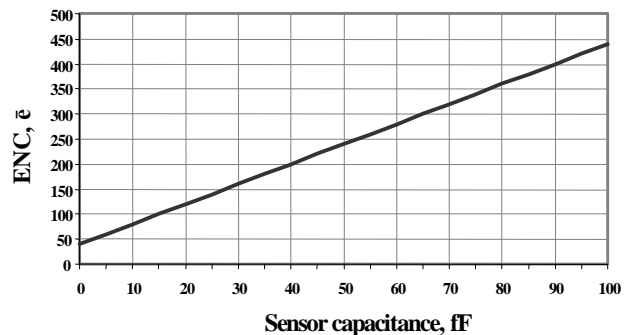

Fig. 5. ENC versus the sensors capacitance (Q_{in}=1 kē, T=27 ℃, CdZnTe sensor)

Fig. 4 shows the peaking time versus sensor capacitance. The simulation shows the peaking time of 25 ns at the 0 fF input capacitance and a strong dependence on the sensor capacitance. The expected peaking time for 300 μm-thick CdZnTe sensor (C_{sen}=30 fF) for the preamplifier is about 45 ns, charge-to-voltage gain is about 71 mV/kē. From this figure, a "charge to voltage" gain of the chain is maximum, and approximately equal 88 mV/kē, while the sensor capacitance is 0 fF. In all sense, the preamplifier has unipolar response. Each preamplifier dissipates 0.5 μW power. Increase of power consumption is undesirable, since from the sensor and the CSP creates the matrix of a large number of elements (from 10^5 to 10^7 channels)

Information lost in the sensor cannot be restored later; therefore the ENC of the sensor and the CSP has to be minimized. The optimal input transistor characteristics of the CSP and the optimal peaking time are selected so, that to get the minimal total ENC. A plot of ENC as a function of C_{sen} at 27°C is shown in Fig. 5. The simulated noise relationship is 40+4 ē/fF resulting in 160 ē for the 30 fF sensor capacitance.

Conclusions

We have designed a high-speed CMOS differential cascade preamplifier with the leakage current compensation circuit using 90 nm technologies. The cascades depress the Miller effect and improve the gain factor of the preamplifier. Computer simulation was carried out with the SPICE simulator using the BSIM4S transistors parameters of the IBM 90 nm CMOS

technology. The advantage of this design is its low-noise level, high speed and high gain with very low-power consumption of 0.5 µW/preamplifier. The equivalent noise charge was less than 160 electrons for a sensor capacitance of 30 fF. The nonlinearity of the preamplifier was less than 2 % for the output voltage of 0.8 V. The preamplifier has unipolar response with the peaking time less than 45 ns and the gain is about 60…90 mV/kē. The circuit architecture of CSP designed in this paper needs to be modified slightly in future research to get lesser noise and power consumption.

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V. Barzdėnas, R. Navickas. The 90 nm CMOS Charge Sensitive Preamplifier // Electronics and Electrical Engineering. – Kaunas: Technologija, 2008. – No. 1(81). – P. 69–72.

The design aspects for low-power, low-noise CMOS charge sensitive preamplifier (CSP), that use a MOSFET transistor as a feedback resistor and leakage current compensation for use with radiation sensors are presented. Computer simulation was carried out with the SPICE simulators using the BSIM4 parameters of the IBM CMOS 90 nm and has shown to simulate CSP with the differential cascade amplifier. The advantage of this CSP design is its low-noise level, high speed and high gain with very low-power consumption of 0.5 µW for the whole preamplifier. The preamplifier has unipolar response with the peaking time of about 35...45 ns and the gain is about 60…90 mV/kē. Equivalent noise charge is less than 160 ē, when the input charge is 1…10 kē and the sensors capacitance is equal to 30 fF. These CSP's are the most widely used for hybrid pixel sensors for high energy particle physics experiments of the charge detection and for MEMS-micromachined inertial accelerometers. Ill. 5, bibl. 11 (in English; summaries in English, Russian and Lithuanian).

В. Барзденас, Р. Навицкас. 90 нм КМОП зарядочувствительный предусилитель // Электроника и электротехника. – Каунас: Технология, 2008. – № 1(81). – С. 69–72.

Представлены аспекты проектирования зарядочувствительных предусилителей (ЗЧП) с компенсацией утечки тока для субмикронной 90 нм КМОП технологии, в которой используют транзистор MOSFET как резистор обратной связи. Компьютерное моделирование было выполнено при помощи программных пакетов SPICE, используя параметры BSIM4 IBM CMOS 90 нм. Предусилитель имеет униполярный ответ с длительностью фронта выходного импульса $\tau_p \approx 35...45$ нс и с коэффициентом преобразования приблизительно 60 … 90 мВ/Кэ. Эквивалентный шумовой заряд - меньше чем 160 ē, когда входной сигнал $Q_{вх}=1…10$ кē и входная ёмкость точечных сенсоров $C_{сен}$ = 30 фФ. Ил. 5, библ. 11 (на английском языке; рефераты на английском, русском и литовском яз.).

V. Barzdėnas, R. Navickas. 90 nm KMOP krūviui jautrus prieššstiprintuvis // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2008. – Nr. 1(81) – P. 69–72.

Submikroninei 90 nm KMOP technologijai sumodeliuotas ir išanalizuotas labai mažos galios ir mažų triukšmų krūviui jautrus prieššstiprintuvis (KJP) su grįžtamojo ryšio MOSFET tranzistoriais ir jutiklio nuotėkio srovės kompensavimo grandine. Modeliavimas atliktas su SPICE programų paketais, naudojant IBM kompanijos KMOP 90 nm tranzistorių BSIM4 modelius. Tokio KJP privalumai yra žemas triukšmo lygis, didelė greitaveika, o panaudotos pakopos leidžia sumažinti Millerio efektą ir padidinti perdavimo koeficientą, esant labai mažai 0,5 µW prieššstiprintuvio naudojamajai galiai. Skaičiuojant gauti tokie pagrindiniai KJP parametrai: vienpolio išvesties signalo registravimo trukmė $\tau_p \approx 35...45$ ns, o perdavimo koeficientas 60…90 mV/kē. Ekvivalentinis triukšmų krūvis, kai įėjimo signalas Q_{in} kinta nuo 1 iki 10 kē ir jutiklio talpa C_{sen} lygi 30 fF, yra mažesnis nei 160 ē. Il. 5, bibl. 11 (anglų kalba; santraukos anglų, rusų ir lietuvių k.).