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Probabilistic-based Defect/Fault Characterisation of Complex Gates from Standard Cell Library

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Introduction

The need for development of new approaches for defect/fault analysis of VLSI circuit is growing and becomes even more important as we move further into the sub-micron devices. Yield loss in ICs fabrication and testing of the manufactured ICs now are major bottlenecks in the production of qualitative VLSI circuits. For instance, it is predicted that the test costs for the emerging deep sub-micron technologies will actually surpass the fabrication cost [1,2,4]. When new materials and processes are introduced, the new failure mechanisms are appeared and different behaviour of faulty circuits caused by defects is exhibited. It means that relative success in providing the high quality of testing by traditional test generation methods and tools cannot be guaranteed. For example, it is forecasted that the margin of error for automatic test equipment accuracy will be up to 50 percent by the year 2012 [2,3]. Such situation forces the development of new approaches for more precise and more detailed defect/fault analysis in VLSI circuits in order to decrease yield loss and to improve test quality.

The necessity of precise and detailed defect/fault analysis is explained by the fact that traditional fault models (which are used by test developers) become less effective. Very popular in the test quality estimation, which are widely used by test developers, are stuck-at fault models (SAF), e.g stuck-at-0 (SA0) and stuck-at-1 (SA1) fault models. These models are used for the test preparation for coverage of physical defects in the CMOS digital ICs. Unfortunately, traditional SAF model does not accurately represent the real physical defects and as a result high SAF coverage cannot guarantee high quality of testing [5,6]. It is explained by the fact that when the test developers use SAF model only, they ignore the real behaviour of a gate in CMOS integrated circuit and SAF model does not adequately represent the majority of IC defects and new failure mechanisms in deep sub-micron technologies [6]. To replace abstract fault models like SAF by realistic defect models we need more detailed approach for defect/fault analysis.

Basics of defect/fault characterisation of standard gates

To be realistic the defect/fault analysis should be layout-driven and should take into account the peculiarities of ICs physical design. These facts are well known [7-11], but unfortunately they are usually ignored in engineering practice through problem complexity, i.e. complexity of the precise defect/fault analysis for the whole IC.

Proposed approach is cell-based and is focused on the precise defect/fault characterisation of standard CMOS gate from industrial cell library. The growth of popularity of standard cell-based design guarantees that approach will be useful and will not be ignored in engineering practice. The probabilistic-oriented approach to the analysis of CMOS physical defect is focused on:

a) precise analysis of gate layout geometry;
b) defect size distribution and density of physical defects obtained on the basis of statistically meaningful information;
c) careful identification of real faulty function from actual behaviour of failure circuit;
d) test-based faults characterisation for finding the best sequence of test patterns for all faults detecting.

In the presented description of complex gate characterisation we consider only short and open defect types in conductive layers of gate layout, because they are the most common fault sources in present-day CMOS digital circuits [2,12]. However, the proposed approach can be extended to other type of physical defects.

Two basic destinations of the process of standard gates characterisation are defined as follows: this process should provide the design for testability (DFT) and design for manufacturability (DFM) via the investigation of gates from the standard cell library designed by commercial VLSI design system, namely Cadence™ design system.

The process of probabilistic-based defect/fault characterisation includes the solution of the next tasks [6]:

1) Formation of its own model of the conductive layers of gate layout: to do this the output text files generated by Cadence Layout Editor (files containing the information about conductive layers of gate layout) are processed.
2) Estimation of probability of occurrence of shorts between nodes and opens in certain branches of a circuit graph: to do this the computational experiment with the use of critical area model of conductive layer of gate layout is carried out for the estimation of probability of shorts/opens.

3) Identification of types of faulty functions resulting from probable defects of short/open type in a gate: to do this the analogue simulation of a gate with introduced short or open defect is used.
4) Estimation of probability of different faulty functions resulting from defects: the vector of probable kinds of faulty functions resulting from defects of short/open type and the vector of these faults probabilities are formed. The list of defects, types of faulty functions caused by these defects, and probabilities of occurrence of these faults are main results of probabilistic analysis.
5) Estimation of the effectiveness of input test patterns for detection of faulty functions caused by physical defects: to do this the defect coverage table is determined.
6) Estimation of optimal sequence of input test pattern for defects detection: to do this the usefulness of the test pattern is estimated as test pattern possibility to detect the greatest number of defects, the sum of probabilities of occurrence of which is the highest.

The probabilistic-based fault characterisation of a great number of different standard gates is computational expensive, therefore it causes the necessity of automation. So, a special software tool has been developed for the application of the proposed methodology in engineering practice. This software tool is named ***FIESTA–EXTRA*** (***F***aults ***I***dentification and ***ES***timation of ***T***est***A***bility by ***EXTRA***ction of faults probabilities, kinds of faults and usefulness of test patterns for faults detection) [14,15]. Structurally FIESTA–EXTRA consists of four basic components-extractors: a) extractor of probabilities of faults (EPF); b) extractor of kinds of faults (EKF); c) extractor of the effectiveness/usefulness of test vector components (EUT).

Figure 1 demonstrates the process of complex gates defect/fault characterisation for defects of short type [14] by the main extractors of FIESTA-EXTRA software.

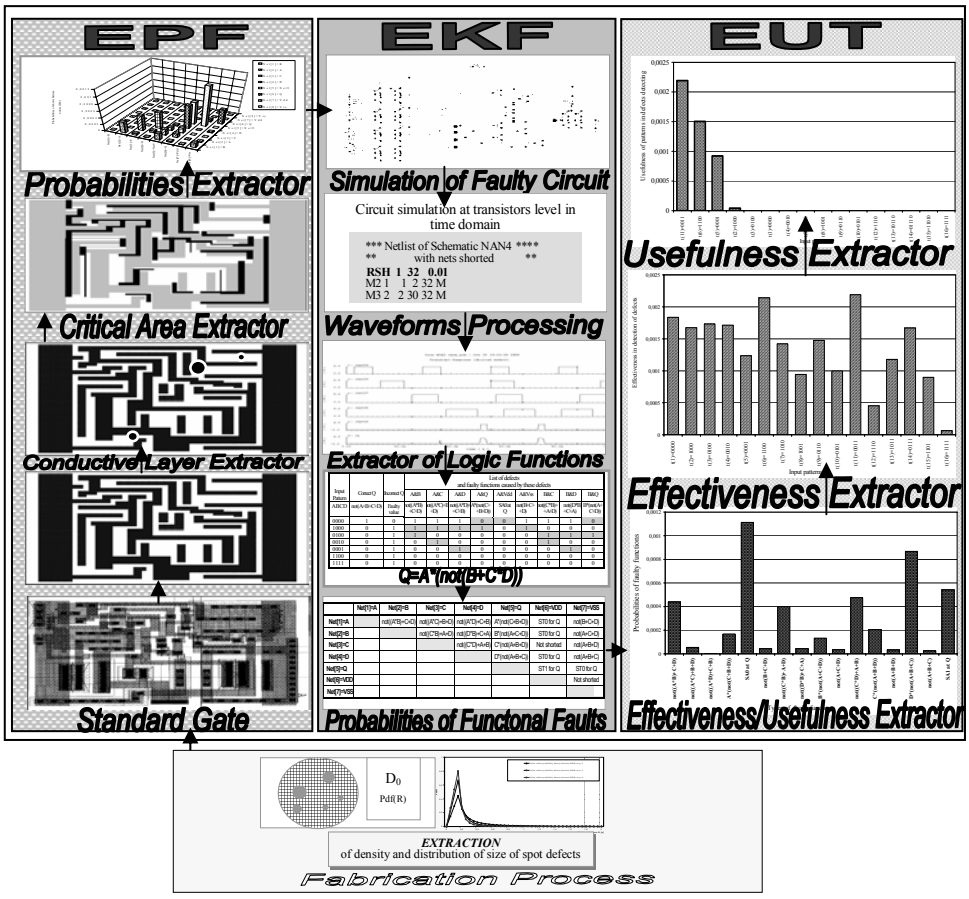

Fig. 1. Process of complex gates characterisation by FIESTA-EXTRA software

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Probabilistic analysis of physical defects in gates layout

The main task of the EPF is determination of the probabilities of occurrence of shorts and opens caused by defects in conductive layers of the gate layout. Defect size distribution and density of defects (for a given layer of layout) extracted from the fabrication process and complete layout of a gate from standard cell library are the input data for the process of defects probabilities determination. Intermediate output data of EPF are the defined values of the probabilities of shorts between certain nodes and opens in certain branches of a circuit graph. These data are the inputs for extractor of kinds of faults where only probable shorts and opens determined by EPF will be simulated at transistors level in order to identify the types of functional faults. Process of extraction of probabilities of defects includes the next techniques:

Extraction of conductive layers of gate layout. In this stage we form the own model of conductive layers of gate layout for autonomic functioning of our software independently from the commercial VLSI design system [14-16]. The model of a conductive layer is formed as the

S matrix, each element $s[i,j]$ of which indicates the belonging of the area $d \times d$ [μm^2] to the corresponding net of schematic. For each conductive layer ***S*** matrices are formed by the processing of output text files generated by Cadence Layout Editor [14-16].

Extraction of critical area. For the estimation of the total probability of occurrence of shorts and opens the well-known concept of critical area extraction is used [13]. Using ***S*** matrix model the technique for the estimation of the distribution of total critical area for shorts between nets and for opens in branches is realized. In this case each element of the matrix $s[i,j]$ reflects the belonging of the area $d \times d$ [μm^2] to the corresponding critical area for short between certain nets and critical area for open in certain branch. Figure 2 demonstrates the extraction of critical area for double and triple shorts for certain defect radius from the Metal 1 layer of 0.8 μm CMOS Nor2 complex gate. The extraction of defects including triple shorts testifies to the preciseness of the analysis of gate layout geometry.

Extraction of the probabilities of shorts/opens. Using the model of critical area, we can determine the probability of certain shorts/opens for a given defect radius. In this stage of characterisation the total probability of occurrence of defects and the distribution of this probability between certain shorts/opens on the given defect radius range are estimated. To do this the computational experiment is carried out with the extraction of the critical area from a given layer of layout. For instance, the critical area for shorts and opens is a function of the defect radius *R*. The product of defect size distribution and the defined probability for a given defect radius $Pdf(R) \times P_{Total}(R)$ integrated over the range of defect radius is taken as a measure of the probability. For example, as the critical area for shorts is a function $S_{CrAr}(R)$ of defect radius *R*, the total probability of shorts $P_{Sh_{Total}}$ in a certain layer of the investigated gate is equal [6]:

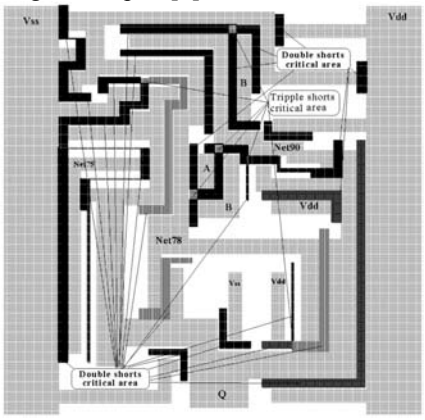

Fig. 2. Critical area extraction for shorts from Metal 1 layer.

$$P_{Sh_{Total}}(R_{Start} \le R \le R_{Stop}) = D_0 \int_{R_{Start}}^{R_{Stop}} P_{Sh_{Total}}(R) \cdot Pdf(R)dR =$$

$$= D_0 \int_{R_{Start}}^{R_{Stop}} \left(S_{CrAr}(R) \Big/ S_{GtAr} \right) \cdot Pdf(R)dR,$$

where R_{Start} – one half of a minimum distance between the shapes in a certain layer of layout; R_{Stop} – statistically well-founded value of *R* upper limit; S_{GtAr} - area of the gate, D_0 – real defect density. The probabilities of shorts between certain nodes (nets) of a circuit are determined by analogy:

$$P_{Sh_{ij}}(R_{Start} \le R \le R_{Stop}) = D_0 \int_{R_{Start}}^{R_{Stop}} P_{Sh_{ij}}(R) \cdot Pdf(R)dR =$$

$$D_0 \int_{R_{Start}}^{R_{Stop}} \left(S_{CrAr_{ij}}(R) \Big/ S_{GtAr} \right) \cdot Pdf(R)dR,$$

where $P_{Sh_{ij}}(R_{Start} \le R \le R_{Stop})$ is the probability of short between *i*-th and *j*-th nodes at defect radius range $[R_{Start} \div R_{Stop}]$; $S_{CrAr_{ij}}(R)$ is a critical area for short between non-equipotential shapes belonging to *i*-th and *j*-th circuit nodes in a certain layer of the gate layout.

The diagram presented in Figure 3 illustrates the distribution of the extracted probabilities of shorts between circuit nodes in Metal 1 layer for Nor2 gate.

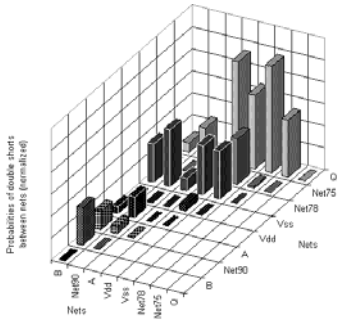

Fig. 3. Distribution of shorts total probability between nodes

On the basis of the extraction of the probabilities of shorts/opens we obtain probable defects of short/open types and their values of probabilities of occurrence. Only these probable defects will be introduced one by one into the gate schematic. Then they will be modelled at the transistor level for the identification of type of functional fault caused by the introduced short or open.

Identification and probabilistic analysis of functional faults caused by defects in gate layout

The main problem in this stage of standard gate characterisation is to correctly represent the realistic behaviour of a faulty circuit in fault model. The behaviour of the digital circuit with short or open can be correctly represented when we treat this circuit in the same way as the analogue circuit. In spite of the purely digital function of a gate, we should carry out the analogue simulation of the circuit (with introduced short/open) in time domain. On the basis of inputs/outputs waveforms obtained from such simulation the actual logic function performed by the faulty circuit is determined.

Probable defects and netlist of the circuit extracted from the layout form the input data for the extractor of kinds of faults. Set of the identified types of functional faults is the main output data of this process. Process of extraction of kind of faults includes two main sequential sub-processes dedicated to the simulation of failure circuit and extraction of logic function.

Simulation of failure circuit provides the modelling of the circuit with the introduced short or open by analogue circuit simulator in order to obtain the waveforms, which will reflect the influence of defect on the behaviour of digital circuit. First stage of this process is the representation of the probable short (or open) by low-Ohm (or high-Ohm) resistor or resistor with another value and its inserting into the netlist of gate schematic. Second stage is connected with the use of SPICE simulator for carrying out the transient analysis of the circuit with the introduced resistor, modelling the physical defect.

Extraction of logic function. The extraction of failure logic function by EKF is based on the detailed analysis of waveforms obtained from faulty circuit simulation. This process includes: a) automatic formation of the truth tables on the basis of input/output waveforms; b) extraction of logic function from the obtained truth tables. Special attention is paid to the careful processing of the input/output waveforms and the extraction of types of functional faults for more complex cases. These complex cases appear when the result of shorts/opens transforms the combinational circuit into sequential one, or provokes the timing hazard type fault, or modifies the own logic function of the gate into analogue or undetectable function.

The main results of EKF work are the types of functional faults and their values of probabilities of occurrence. Example of results obtained by EKF for 0.8 μm CMOS Nor4 complex gate is given in Table 2 (logic diagram of Nor4 complex gate is shown in Fig.4.)

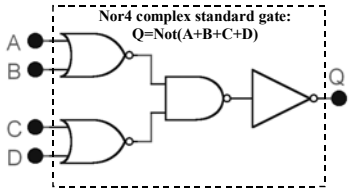

Fig. 4. Logic diagram of Nor4 complex gate.

Table 1. Identified types of functional faults in Nor4 gate and their probabilities

Defects of short type (shorted Net_i&Net_j)	Type of identified functional faults caused by defects	Probabilities of identified functional faults
Q&Vdd; Net10&Vss	SA1_for_Q	1,25E-09
Q&Net10	(A+B+D+C)	1,20E-09
Net9&Vdd	not(A+B)	2,21E-10
Net9&Net10	(((C+D)*not(A+B))+(C*D))	1,88E-09
Net8&Vdd	not(C+D)	2,83E-09
Net8&Net10	(((A+B)*not(C+D))+(A*B))	1,52E-09
C&Vss	not(A+B+D)	2,47E-11
C&Net9	C*(not(A+B+D))	1,68E-09
D&Net9	D*(not(A+B+C))	1,04E-10
C&D	not((C*D)+A+B)	1,07E-09
B&Vss	not(A+C+D)	1,39E-11
B&Net8	B*(not(A+C+D))	2,14E-10
B&C	not((C*B)+A+D)	1,43E-10
B&D	not((D*B)+C+A)	4,41E-10
A&B	not((A*B)+C+D)	3,53E-10
A&Net8	A*(not(C+B+D))	9,58E-10
A&C	not((A*C)+B+D)	1,11E-11
A&D	not((A*D)+C+B)	2,00E-10
A&Vdd; D&Vdd; C&Vdd; Q&Net8; Q&Vss Net8&Vss; Q&Net9; Net9&Vss; Net10&Vdd	SA0_for_Q	1,98E-09

Test-based defect/fault characterisation

After the kinds of functional faults and their probabilities are determined using the EPF and EKF we are able to find the components of a test vector for detecting these faults. On the basis of the determined values of the probability of occurrence of these faults the estimation of the effectiveness and usefulness of the test patterns for detecting physical defects is possible. It is the process of extraction of effectiveness/usefulness of test vector components that is realised by corresponding part of software – EUT. Depending on the type of the functional fault and on the logic function of the gate the fault may be detected by several components of test vector. On the contrary, some of the components of test vector detect several functional faults. We can estimate the effectiveness of test vector components for the detection of the functional faults. To do this we sum the probabilities of the functional faults detected by certain component of test vector. Table 2 contains the estimated effectiveness of test vector components for defects detecting in Nor4 complex gate.

Considering the fact that in many cases a fault is detected by several components of test vector, we use the concept of usefulness of test vector components. The usefulness of the test vector component depends on its ability to detect the greatest number of faults, the sum of probabilities of which is the highest on condition that there

are no faults detected by several components [6]. The estimated usefulness of the test vector components in defects detecting for Nor4 gate are shown in Figure 5.

Such estimation of the usefulness of test vector components allows to improve the work on the development and generation of test cycles and to provide high quality of tests. The high quality of test and improvement of work of the test developers is provided by finding the best sequence of patterns for the detection of all faults and by reducing the average length of the sequence of patterns to a minimum. The diagrams in Figures 6,7 show the obtained optimal sequence of test patterns for the gates from cell library in 0.8 μm CMOS technology.

Table 2. Effectiveness of the test vector components in shorts detection for the Nor4 gate

Test vector components	Defects detected by component of test vector	Effectiveness
V(0)=0000	A&Net8 A&Vdd B&Net8 D&Net9 D&Vdd C&Net9 C&Vdd Net8&Net10 Net8&Q Net8&Vss Net9&Net10 Net9&Q Net9&Vss Net10&Q Net10&Vdd Q&Vss	9,53E-09
V(1)=1000	A&B A&D A&C A&Net8 Net8&Net10 Net8&Vdd Net10&Q Net10&Vss Q&Vdd	8,31E-09
V(2)=0100	A&B B&D B&C B&Net8 B&Vss Net8&Net10 Net8&Vdd Net10&Q Net10&Vss Q&Vdd	7,95E-09
V(3)=1100	Net8&Net10 Net8&Vdd Net10&Q Net10&Vss Q&Vdd	6,79E-09
V(4)=0010	A&C B&C D&C C&Net9 C&Vss Net9&Net10 Net9&Vdd Net10&Q Net10&Vss Q&Vdd	7,47E-09
V(5)=1010	Net10&Q Net10&Vss Q&Vdd	2,44E-09
V(6)=0110	Net10&Q Net10&Vss Q&Vdd	2,44E-09
V(7)=1110	Net8&Net10 Net10&Q Net10&Vss Q&Vdd	3,96E-09
V(8)=0001	A&D B&D D&C D&Net9 Net9&Net10 Net9&Vdd Net10&Q Net10&Vss Q&Vdd	6,36E-09
V(9)=1001	Net10&Q Net10&Vss Q&Vdd	2,44E-09
V(10)=0101	Net10&Q Net10&Vss Q&Vdd	2,44E-09
V(11)=1101	Net8&Net10 Net10&Q Net10&Vss Q&Vdd	3,96E-09
V(12)=0011	Net9&Net10 Net9&Vdd Net10&Q Net10&Vss Q&Vdd	4,54E-09
V(13)=1011	Net9&Net10 Net10&Q Net10&Vss Q&Vdd	4,32E-09
V(14)=0111	Net9&Net10 Net10&Q Net10&Vss Q&Vdd	4,32E-09
V(15)=1111	Net8&Net10 Net9&Net10 Net10&Q Net10&Vss Q&Vdd	5,84E-09

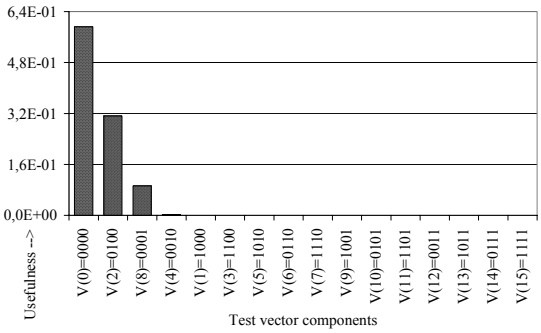

Fig. 5. Usefulness of test vector components for physical defects detection for Nor4 complex gate

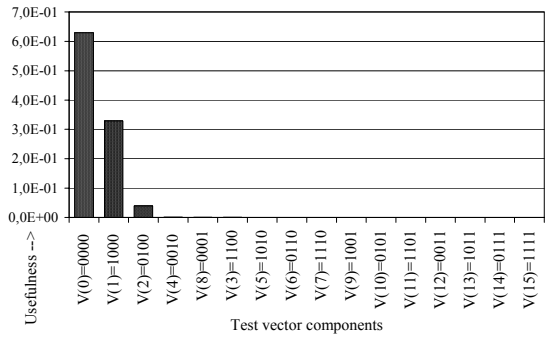

Fig. 6. Optimal sequence of test patterns for physical defects detection in And2_Nor3 complex gate

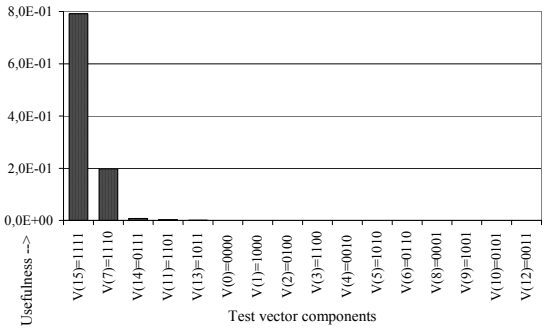

Fig. 7. Optimal sequence of test patterns for physical defects detection in Nan4 complex gate

The results of test-based characterisation of complex gates have been successfully used by test developers for hierarchical defect-oriented fault simulation of digital circuits. It is shown that using SAF models (which ignore the actual behaviour of failure circuit) leads to overestimation of test sets quality [6,17].

Conclusions

According to the above-described process of defect/fault characterisation complex gates from any industrial standard cell library can be investigated using FIESTA-EXTRA software. Such probabilistic and test-based characterisation allows: - to find optimal sequence of test vectors for detecting faults caused by physical defects; - to improve the quality of test sets for CMOS circuits, and - to increase the VLSI testability by gates layout

modification decreasing the probability of occurrence of not detectable faults. The precise analysis of gate layout geometry and its sensitivity to physical defects provides the possibility for layout optimisation aimed at decrease of the yield loss resulting from the influence of physical defects in manufacturing.

References

1. **Sengupta S., Kundu S., Chakravarty S., Parvathala P., Galivanche R., Kosonocky G., Rodgers M., Mak TM.** Defect-based test: a key enabler for successful migration to structural test // Intel Technology Journal Q1'99, available on the Web (URL: http://intel.com/technology/itj/ q11999/pdf/defect_ based.pdf).
2. **1997 SIA Roadmap**. Summary for MR&DCAN'98. June, 25, 1998.
3. **Announcements**. Mentor Graphics raises the bar on ensuring reliability testing of complex electronic systems with new Bist technology // available on the Web: http://www.edtn.com/ TestandMeasurement/prod014.html).
4. **International** Technology Roadmap for Semiconductors. 1999 Edition.
5. **Soden JM., Hawkins CF.** Quality testing requires quality thinking // In: Proc. Int. Test Conference, 1993. - P. 596.
6. **Blyzniuk M., Kazymyra I., Kuzmicz W., Pleskacz W., Raik J., Ubar R.** Probabilistic analysis of CMOS physical defects in VLSI circuits for test coverage improvement // Microelectronics Reliability, 2001. - Vol. 41/12. – P. 2023-2040.
7. **Maly W., Shen JP., Ferguson FJ.** Systematic characterization of physical defects for fault analysis of MOS IC cells // Proc. International Test Conference, Philadelphia, October 1984. – P. 390-399.
8. **Shen JP., Maly W., Ferguson FJ.** Inductive fault analysis of MOS integrated circuits // Proc. IEEE Design and Test, December 1985. – P. 13-26.
9. **Nigh P., Maly W.** Layout-driven test generation // Proc.. International Conf. on Computer Aided Design, 1989. - P.154-157.
10. **Jacomet M., Guggenbuhl W.** Layout-dependent fault analysis and test synthesis for CMOS circuits // IEEE Trans. on CAD, 1993. – Vol.12. – P. 888-899.
11. **Chess B., Freitas A., Ferguson FJ, Larrabee T.** Testing CMOS logic gates for realistic shorts // Proc. International Test Conference, IEEE, 1994 – P. 395-402.
12. **Predictions** Software Ltd. Process Yield Enhancement. // Edinburgh Technology Transfer Centre, available on the Web: http://www.icyield.com/yield_enhan_proc.html.
13. **Stapper C.H.** Modeling of defects in integrated circuit photolithographic patterns // IBM J. Res. Develop. 1985. – Vol. 29, No.1. – P. 461-475.
14. **Blyzniuk M., Kazymyra I.** Development of the special software tools for the defect/fault analysis in the complex gates from standard cell library // Proc. of the IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT'01), San Francisco, USA, October 2001. – P. 375-383.
15. **Blyzniuk M, Kazymyra I.** FIESTA-EXTRA: Cell-Oriented Software for the Defect/Fault Analysis in VLSI Circuits // Accepted for publication Proc. of IEEE 24rd International Conference on Microelectronics (MIEL 2004), Nis, Serbia and Montenegro, May, 2004.
16. **Blyzniuk M., Kuzmicz W., Panchak T., Pleskacz W.** Graphical User Interface of FIESTA – Software for Faults Identification and Estimation of Testability of VLSI Circuits // Proc. of the symposium on Contemporary computing in Ukraine, ACM Press New York, NY, USA, 2000 (ACM Digital Library: http://doi.acm.org /10.1145/352491.352513).
17. **Blyzniuk M., Cibaková T., Gramatova E., Kuzmicz W., Lobur M., Pleskacz W., Raik J., Ubar R.** Hierarchical defect-oriented fault simulation for digital circuits // Official ETW'2000 Proc., IEEE Computer Society Press, Portugal, May 2000. – P. 69-74.

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Pateikiama sudėtingų loginių elementų paklaidų analizė. Įrodyta, kad paklaidų atsiradimo priežastis yra gamybos defektai. Analizė atlikta tikimybiniais metodais, taip pat naudojant klasikinę FIESTA-EXTRA programinę įrangą. Išanalizuoti loginių elementų topologinių matmenų bei fizinių defektų tankių identifikavimo galimybės. Il. 7, bibl. 17 (anglų kalba; santraukos lietuvių, anglų ir rusų k.).

M. Blyzniuk, I. Kazymyra. Probabilistic-based Defect/Fault Characterisation of Complex Gates from Standard Cell Library // Electronics and Electrical Engineering. – Kaunas: Technologija, 2004. – No. 3(52). –P. 67-72.

The process of probabilistic-based defect/fault characterisation of complex gates from industrial cell library is considered. The aim of defect/fault characterisation is the realistic representation of physical defects influence on gate behaviour in fault models. The characterisation process is focused on the precise analysis of gate layout geometry, defect size distribution, and density of physical defects, on careful identification of real faulty function from actual behaviour of failure circuit, and on test-based fault characterisation for finding the best sequence of test patterns for all faults detecting. The description of cell-oriented software FIESTA-EXTRA for the automation of the process of gates defect/fault characterisation is presented. The obtained results of gates characterisation from industrial standard cell library in 0.8 μm CMOS technology are analysed. Ill. 7, bibl. 17 (in English; summaries in Lithuanian, English, Russian).

М. Блызнюк, И. Казымыра. Вероятностное описание дефектов и ошибок в сложных логических элементах стандартной библиотеки // Электроника и электротехника. – Каунас: Технология, 2004. — № 3(52). –С. 67-72.

Рассматривается процесс вероятностного описания дефектов и ошибок сложных логических элементов из стандартной библиотеки. Основной целью описания дефектов и ошибок является реалистическое представление в моделях ошибки влияния физических дефектов на функционирование логического элемента. Процесс описания сфокусирован на детальном анализе топологии логического элемента, вероятности распределения размеров и плотности физических дефектов, точной идентификации действительной ошибочной функции на основе анализа поведения неисправной схемы и ориентированном на тестирование описании ошибок для нахождения наилучшей последовательности тестовой комбинации для выявления всех неисправностей. Представлено описание программного средства FIESTA-EXTRA для автоматизации процесса описания дефектов и ошибок логических элементов из стандартной библиотеки. Проанализированы полученные результаты описания логических элементов из стандартной промышленной библиотеки элементов КМОП технологии (0,8 мкм). Ил. 7, библ. 17 (на английском; рефераты на литовском, английском и русском яз.).

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