ELECTRONICS AND ELECTRICAL ENGINEERING
ISSN 1392 – 1215 *2007. No. 7(79)*
ELEKTRONIKA IR ELEKTROTECHNIKA

MICROELECTRONICS
T 171
MIKROELEKTRONIKA

Investigation of Porous Silicon Layers as Passivation Coatings for High Voltage Silicon Devices

D. K. Šalucha
Semiconductor Physics Institute,
A. Goštauto str. 11, LT-01108 Vilnius, Lithuania, phone: +37061681157, e-mail: d.salucha@gmail.com
A. J. Marcinkevičius
Vilnius Gediminas Technical University, Computer Engineering Department,
Naugarduko str. 41–437, LT–03227 Vilnius, Lithuania, phone: +370 5 2744772, e-mail: Albinas.Marcinkevicius@el.vtu.lt

Introduction

Porous silicon (PS) can be considered as a silicon crystal having a network of voids in it. The nanosized voids in the Si bulk result in a sponge-like structure of pores and channels surrounded with a skeleton of crystalline Si nanowires. In this paper, is proposed to use porous silicon layer as dielectric and passivation layer in SCR thyristors and diodes. The physical properties of porous silicon are fundamentally determined by the shape and diameter of pores, the thickness and the relative content of Si, voids, and in some cases, the relative content of different Si compounds in the formed porous layer. These parameters depend on preparation conditions, so that it is possible to design materials with physical properties of those between Si and air (or the medium which fills the pores). In addition, when the feature size of the Si wires is less than a few nanometers, various quantum-size effects occur which make PS even more fascinating. Because of its versatility and tunable/designable characteristics, PS has become a popular material among scientists and technologists, and has been applied in various fields during the past two decades.

The porous silicon structure is formed by electrochemical etching of Si wafers in electrolytes including hydrofluoric acid (HF) and surfactants (mainly ethanol). Ethanol is often added to facilitate evacuation of H_2 bubbles; these bubbles can easily leave the surface because of the decreased surface tension of the liquid. Additionally, the bubbling enhances the liquid circulation in the electrolyzation cell, which helps the transport of reactants and side products. To be able to synthesize uniform layers with high reproducibility, the applied anodic current density and etching time are monitored, controlled and kept at a particular constant level required during the process. Typical anodization arrangements are schematically shown in Fig. 1 [1].

For p-type Si, the holes are the majority charge carriers, so the p-type PS (p-PS) layers are fairly easily produced. Conversely, n-type PS (n-PS) is very difficult to form, as a result of the lack of holes.

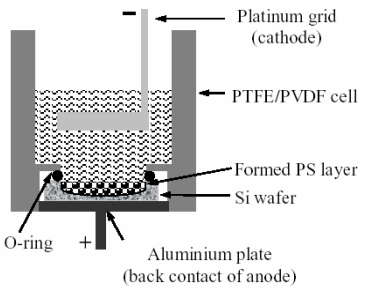

Fig. 1. The schematic diagram of experimental setup for preparing n-PS layer vertical arrangement

Previously, most of the research done on PS has been made on hole-rich p-type Si. Up till now, to get an n-PS layer, illumination has still been the popular way (even indispensable way) to generate the holes required in the electrochemical etching process on the hole-poor n-type samples.

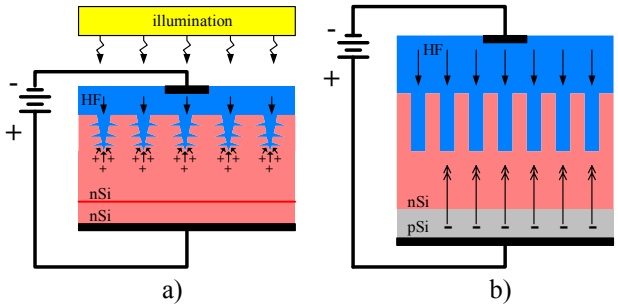

Fig. 2. Two mechanisms of creation the PS: a) the mechanism skecth with the iliumination - assistance approach, and b) the mechanism skecth with the bottom-hole-assisted approach

Yet, the actual photo-energy absorbing by Si atoms is very sensitive to the illumination-source intensity Fig. 1 a) and electrolyte environment, and the conditions are not constant in the process. Since the illumination intensity is related to the distance besides the absorption of the light in the device itself, only top-layer atoms are photo-excited and only the surface layers under illumination generate the electron-hole pairs. The etching rate will gradually decrease with depth from top-to bottom layers because the illumination is very difficult to reach the deeper layers. Therefore, cone-shape pores in PS structures are often formed by this way [2]. In other words, the only-illumination-assisted etching approach is depth limited. In this paper, a new approach (named as bottom-hole-assisted approach) is proposed for manufacturing n-PS layers. A mount of holes are supported by a forward biased np-junction in which the p-layer plays the role as a hole-source underneath the n-layer. When the assistance of illumination is applied, the electron-hole pairs are generated and accumulating only on the top surface layers in which some tiny lateral etching accompanies with the vertical etching. On the other hand, in the bottom-hole-assisted approach as Fig. 2 b), an electrical field across the anode and cathode forward biases the np junction, and holes flow straight-upward from p- to n-region. Sufficient holes can reach to the pore tips to participate in chemical reaction during the etching process, even in the dark.

Experiment

The schematic diagram of the experimental setup for preparing n-PS layer is given in Fig. 1. The main body of the HF electrolyte container is made of teflon materials. And, the apparatus is designed in a horizontal arrangement. Also, the PS samples are prepared on Si (111). Here a mixture of HF and C_2H_5OH is utilized as the etching solvent in different volumes. The illustrative equation [2] of the overall process during PS formation can be expressed as below:

$$Si + 2HF + 2h^+ \rightarrow SiF_2 + 2H^+, \qquad SiF_2 + 4HF \rightarrow H_2 + H_2SiF_6. \tag{1}$$

In the equation, the etching rate is determined by the hole (h^+) generation.

The anodization in *galvanostatic* (current-controlled) mode is used. It is normally preferred, because it supplies the required charge for the reaction at constant rate, regardless of any evolution — during anodization — of the cell electrical impedance, ultimately leading to more homogeneous and reproducible material. The anodization can be modulated. The modulation is most easily achieved by varying the applied current density [2, 3]. Modulation results in controlled changes of the microstructure and the porosity of PS along the growth direction. For example, PS multilayer films can be simply created by varying the current density in time. Then is available layered PS with different porosity in each layer.

Like samples were taken dies after groove etching before glass passivation (Fig. 3) and final passivated thyristor with central gate. In Fig. 3 is shown the figure of thyristor with etched groove, for diodes there is not groove from bottom side.

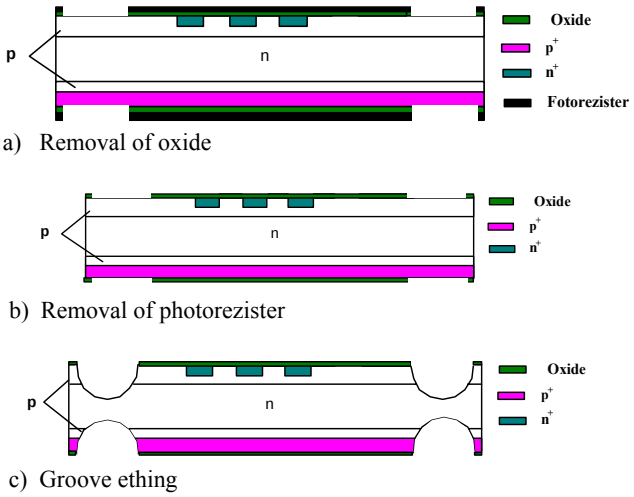

Fig. 3. Summary of technological process, from which point the samples were taken: a) removal of oxide, b) removal of photoresister, c) groove etching

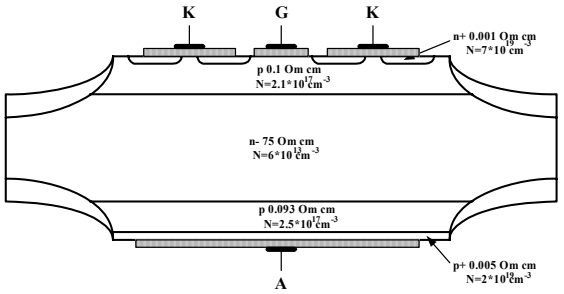

Fig. 4. Cross-section of thyristor, with central gate electrode

The purpose is to create PS layer in the groove herewith performing gettering operation to extract impurities from bulk to electrochemical oxide.

The PS samples, investigated in this thesis, were synthesized on n-type Si wafers by anodic etching using a conventional single-tank electrolyzation cell (Fig. 1). The wafers were boron-doped and polished along the (111) crystal plane direction. The electrolytes were prepared by mixing HF solution and absolute ethanol (C_2H_5OH) in various volumetric ratios.

Table 1. Effect of anodization condition on the formation of PS

Increasing the values of:	Porosity	Etching rate	Critical current
HF concentration	Decreases	Decreases	Increases
Current density	Increases	Increases	-
Anodization time	Slightly increases	Slightly decreases	-
Temperature	-	-	Increases
Wafer doping (p-type)	Decreases	Increases	Increases
Wafer doping (n-type)	Increases	Increases	-

As listed [1] in Table 1, the properties of the PS can be tuned through the manufacturing conditions, such as electrolyte concentration (c), current density (J) and etching time (t). The anodizing current densities were stabilized and the etching times were controlled by a

computer (AUTOLAB, GPES-General Purpose Electrochemical System v 4.9). To create freestanding membranes an electropolishing step was applied in the last stage of anodization to detach the formed porous layers from the wafer. Each sample was flushed in absolute ethanol and stored in a separate container. When it was applicable, the samples were freshly made before the particular post-fabrication and/or analyses processes.

The biasing voltage was monitored during single PS layer fabrication to detect anomalies, such as significant changes in voltage due to leakage. In Fig. 5 a typical voltage monitored during an etching is shown. It is included here due to the curious curve shape. The plot contains surprisingly many features considering the sample was etched with a constant current. There is a transient region in the beginning which may be ascribed to a build up of charge before etching begins, e.g. due to an activation energy. The irregular sawtooth pattern may be due to local oxide build-up and etching, as in the current-burst model or due to hydrogen bubbles interfering with electrolyte flow [4].

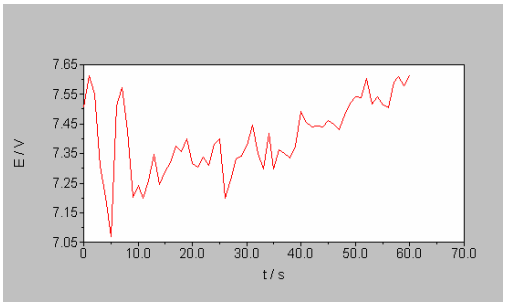

Fig. 5. During etching with constant current the varying voltage is measured. There is a transient period at the start which after a few seconds goes over into an irregular saw tooth pattern. This oscillation may be linked to oxide build up and etch in the pores, however, this is not well understood

In Fig. 6 you can see the selection of electrochemical etching rates. In this experiment, constant current density (700 mA/cm^2) and variable the duration of etching.

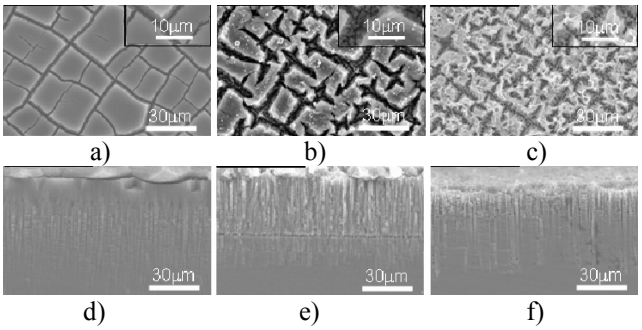

Fig. 6. The top view (a-c) and the cross-section (d-f) SEM images of the PS samples with different electrochemical etching durations: a), d) t = 60 s, b), e) t = 20 s, c), f) t = 10 s

In Fig 6. we can see that very thin PS layer was made. This layer was formed in the diode groove and it was very complicated to get there and to take a picture this etched area. After the formation pf PS layer the samples with PS layer were annealed in H_2 atmosphere for 1 hour in 550°C degrees of temperature [3]. Annealing process was used to get impurities from bulk and to gather impurities in electrochemical PS layer. In one variation this electrochemical oxide was etched in alkali solution for 20 seconds, in other variation this oxide was left and before passivation freshened in HNO_3:HF:CH_3COOH solution for 5 seconds.

The influence of the passivation on the diodes voltage blocking capabilities is shown in Table 2, where are presented the reverse characteristics of the best non-passivated and passivated devices. The breakdown voltage of the passivated diode was extended by about 25% (comparing with standard technological process).

Table 2. U_{RRM} values of PS layer formation experiment

	STD passivation	With PS layer	With PS layer
After groove etching, before glass passivation	700-800V	800V	800V
After annealing operation	--	850V	850V
After PS layer etching	--	--	900V
After glass (Pb-B-Si-Al) passivation	1800-1900V	1900-2000V	2000-2100V

Groove profile after removing electrochemical oxide (Fig. 7a) and glass SiO_2-PbO-Al_2O_3-B_2O_3 passivation (Fig. 7 b).

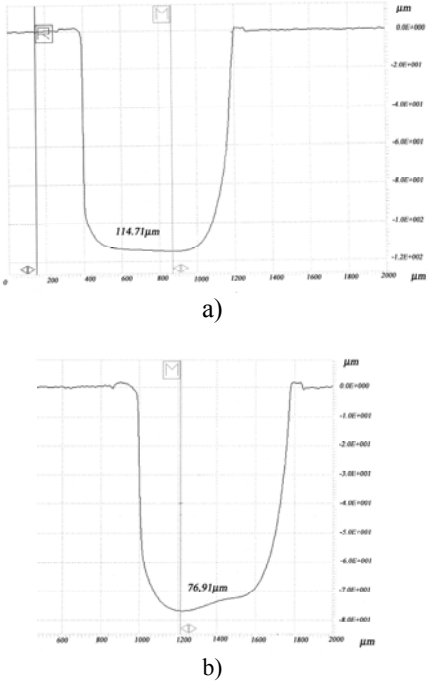

Fig. 7. Groove after etching (a) and groove after glass (Pb-B-S-Al) passivation (b). *(Measured with profilometer Dektak 8)*

As shown in Fig. 7 a), the groove depth before passivation is 114,71 µm, after passivation left groove depth is 76,91 µm, that means the thickness of passivated glass layer is 37,8 µm. As shown in Fig 1 b), there is an

undulation of glass surface in the bottom of the groove. This undulation can be explained by singularity of technological glass passivation process parameters, such as, heating and cooling temperature gradients.

Conclusions

The creation electrochemical PS layer for power devices passivation is proposed. PS layers having different thickness and porosity were prepared and analyzed. The dependence of the thickness on the anodization time and the effect of current density and electrolyte composition on the porosity were determined and found proportional within a good range.

The spontaneous oxidation of the PS structure is a disadvantage in the applications of the PS layers. This aging effect can be eliminated by partial or full oxidation of the porous material. For this reason, it is proposed to etch formed electrochemical oxide with gathered impurities inside the layer.

Obviously, improved results could be explained of growing broader the groove. But with removing the oxidized layer collectively removes gathered impurities from the bulk, what couldn't effect growing broader of the groove.

References

1. **Andrea Edit Pap.** Investigation of Pristine and Oxidized Porous Silicon // Faculty of technology, University of Oulu, Finland. – 2005. – P. 13–45.
2. **Jia-Chuan Lin, Wei-Lun Chen and Wei-Chih Tsai.** Photoluminescence from n-type porous siliconlayer enhanced by a forward-biased np-junction // Optics Express. – 2006. – Vol. 14, No. 21. – P. 47–52.
3. **Yue Zhao, Deren Yang, Dongsheng Li, Minghua Jiang.** Annealing and amorphous silicon passivation of porous silicon with blue light emission // Applied Surface Science 252. – 2005. – P. 1065–1069.
4. **Bilyalov R., Matic Z., Poortmans J., Schomann F., Schmidt W.** Synergetic effect of aluminum and thermally treated porous silicon for bulk passivation of multicrystalline silicon // IEEE Transactions on Electron Devices. – 2005. – P. 291–294.

Submitted for publication 2007 03 01

D. K. Šalucha, A. J. Marcinkevičius. Investigation of Porous Silicon layers as Passivation Coatings for high voltage Silicon Devices // Electronics and Electrical Engineering. – Kaunas: Technology, 2007. – No. 7(79). – P. 43–46.

The porous silicon layer as the passivation coating for high voltage devices is proposed. PS layers having different thickness and porosity were prepared and analyzed. The dependence of the thickness on the anodization time and the effect of current density and electrolyte composition on the porosity were determined and found proportional within a good range. For this reason, is proposed to etch formed electrochemical oxide with gathered impurities inside the layer. Imroved rezults could be explained of growing broader the groove. But with removing the oxidized layer collectivelly removes gathered impurities from the bulk, what couldn`t effect growing broader of the groove. A new bottom-hole-assisted approach based on a forward biased np-junction for manufacturing n-PS layer is discussed. Illumination is an optional hole-source in the fabrication of n-type PS. The bottom-hole-assisted approach can overcome the illumination-limitation and depth-limitation problems in conventional only-illumination-assisted approach. With the bottom-hole-assistance, the anodization etching is almost anisotropic. Ill. 7, bibl. 4 (in English; summaries in English, Russian and Lithuanian).

Д. К. Шалуха, А. И. Марцинкявичюс. Исследование пористых кремниевых слоев как покрытия пассивирования для высоковольтных устройств // Электроника и электротехника. – Каунас: Технология, 2007. – № 7(79) . – С. 43–46.

Предложен пористый кремниевый слой как покрытие пассивирования для высоких устройств напряжения. Были зделаны и проанализированы пористые кремниевые слои, имеющие различную толщину и пористость. Это предложено, чтобы снять сформированную электрохимическую окись с собранными примесями(загрязнениями) в слое. Обсуждается новый помогшийся забоем подход, основанный на передовом предубежденном np-соединении для того, чтобы изготовлять слой n-PS. Помогшийся забоем подход мог преодолеть ограничение освещения и проблемы ограничения глубины в обычном, только освещение помогало. Ил. 7, библ. 4 (на английском языке; рефераты на английском, русском и литовском яз.).

D. K. Šalucha, A. J. Marcinkevičius. Porėto silicio dangų pritaikymas galingų silicio prietaisų pasyvacijai // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2007. – Nr. 7(79) – P. 43–46.

Galingų puslaidininkinių prietaisų pasyvacijai pasiūlytas porėtojo silicio sluoksnio panaudojimas. Išnagrinėti skirtingų storių ir porėtumo sluoksniai. Nagrinėjama sluoksnio storio priklausomybė nuo elektrocheminio ėsdinimo trukmės, srovės tankio ir tirpalo koncentracijų. Siūlomas elektrocheminio oksido, kuriame po atideginimo iš tūrio ištrauktos priemaišos, nuėsdinimas. Pramušimo įtampų verčių pagerėjimą galima būtų paaiškinti nuėsdinant sudarytąjį elektrocheminį oksidą, kartu nuimamos priemaišos, geteravimo metu ištrauktos iš bandinio tūrio. Aptartas būdas porėtojo silicio sudarymui, papildomai sudarant anodo srityje p laidumo sritį. Ši sritis yra panaudojama kaip skylių šaltinis, kurį atstoja bandinio apšvietimas šviesa. Panaudojant šviesą yra apribojamas sluoksnio sudarymo gylis ir bandinio ruošimas bet kokiomis sąlygomis. Naudojant pasiūlytąjį metodą, anodinis ėsdinimas yra beveik anizotropinis ir neturi minėtųjų trūkumų. Il. 7., bibl. 4 (anglų kalba; santraukos anglų, rusų ir lietuvių k.).