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Signal Simulation in Folding and Interpolating Integrated ADC

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Introduction

Simulation of dynamic characteristics of the signal sample and hold, folding and interpolating devices is presented in the literature [1–4]. In this work we will present the signal simulation results of the integrated 8 – bit ADC, in which the above mentioned signal transformation circuits are used.

CMOS (0.35 μm) and SiGe 7–8 – bit folding–interpolating converters with the number of samples per second from 10 million to 2 milliard are considered in [5–7]. Block schemes, static–dynamic parameters, frequency characteristics of separate blocks of converters and experimental research results are presented. The converter structure, circuitry solutions and interfaces between separate blocks of signal transformation and decryption are not revealed in the mentioned literature.

The analysis of construction of the 8–bit 4 milliard samples per second converter and simulation results of dynamic characteristics are presented in this work.

Analysis of construction of the sample and hold, folding and interpolating ADC

The created functional scheme of the 8–bit ADC with signal transformation circuits is presented in Fig. 1. It consists of the sample and hold circuit SHC, 6 folding blocks F1–F6, the interpolation block IB, logic "exclusive or" element block XOR, the comparator block CB, the encryption block EN and signal delay blocks DB1–DB4. The basic electrical circuits of blocks were created and simulation of their characteristics was performed.

The analog input signal passes to the sample and hold circuit SHC (Fig. 1). SHC is controlled by clock signals, which are matched with the comparator clock signals so that the signal samples are used for further processing when the signal does not vary. It allows avoiding the signal conversion distortion related to different delays in the signal and clock circuits of comparators.

After SHC, the signal passes to the signal folding blocks F1 – F6, and also to the 4–bit parallel ADC. Thus, half of bits are processed by the parallel converter. Practically, it is much more important half of bits as they transmit information about higher bits of the signal, and the error of even one bit would cause an impermissibly large signal distortion.

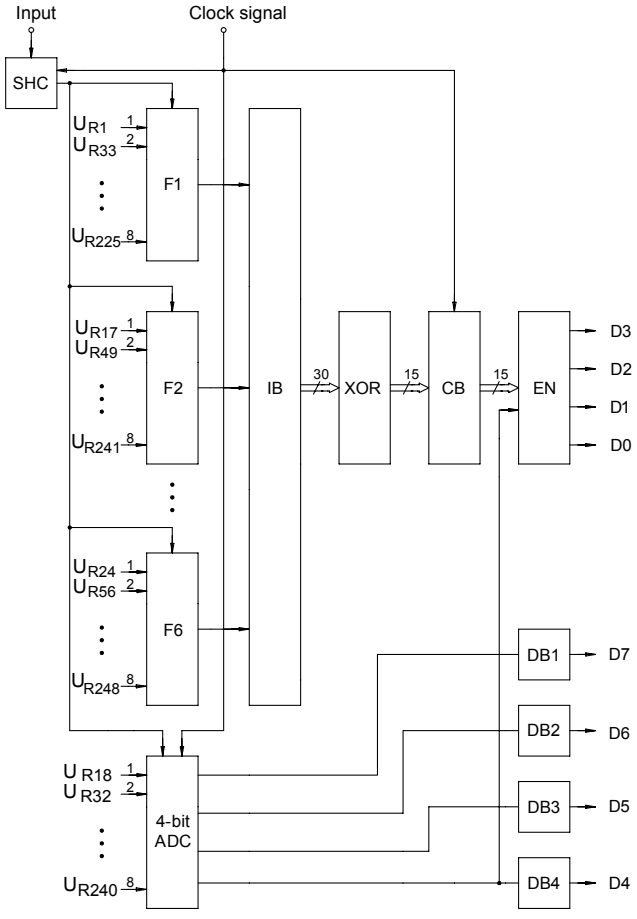

Fig. 1. Diagram of the structure of the 8–bit folding and interpolating analog–to–digital converter

Lower 4 bits are processed in the folding and interpolating blocks after which a much smaller number of comparators is needed than in the case of the parallel converter.

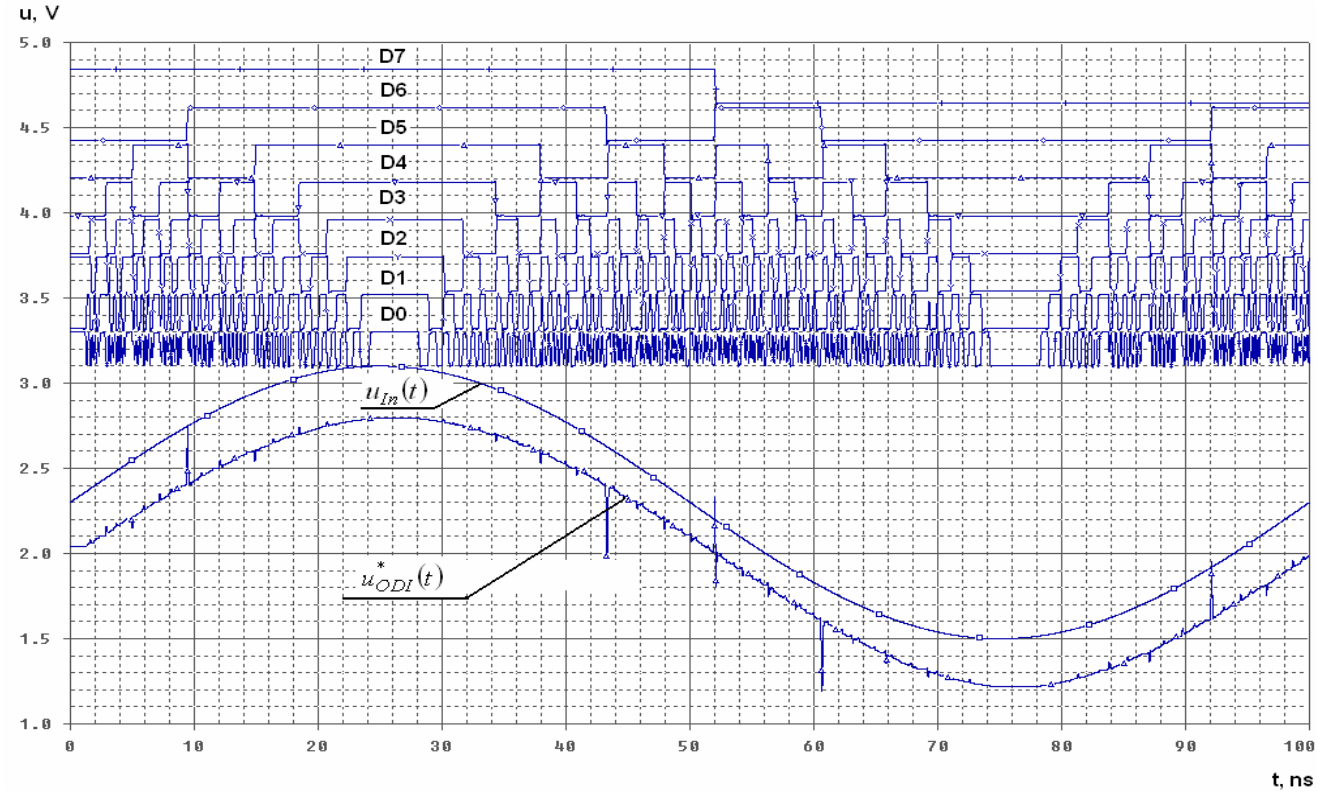

Fig. 2. Time diagrams of input and output signals of the 8–bit folding – interpolating ADC

Both the 4–bit parallel comparator and the folding blocks (F1 – F6) are switched to the reference voltage formation circuit in a certain order.

From folding blocks the signals pass to the interpolating circuit block and then together with signals of higher bits – to the decoding circuit blocks. The 8–bit binary signal is obtained in the decoder output.

Simulation of characteristics of the folding – interpolating converter

The main parameters of the simulated converter are presented in Table 1.

Table 1. Parameters of the sample and hold, folding and interpolating ADC.

Frequency of the converter analog sine signal	(0–100) MHz
Number of binary bits	8 bits
Frequency of the converter clock pulses	4 GHz
Amplitude of the analog sine signal	1.6 V
Supply voltage of the converter	3.3 V
Folding coefficient	8
Interpolation coefficient	6
Minimal dimension of technology corresponding to the bipolar transistor model parameters	0.5 μm

Time diagrams of input and output signals of the 8–bit folding – interpolating ADC are presented in Fig. 2. In the figure there are also presented:

$u_{IN}(t)$ is the simulated input signal, the frequency of which is 10 MHz;

D0 – D7 are ADC digital outputs corresponding to the binary code, where D7 is the output of the highest bit, and D0 is the output of the lowest bit;

$u^*_{ODI}(t)$ is „DAC imitation output" – the signal simulated by the package P–Spice according to equations (1) and (2).

For the simulation of the converter electric circuits by the program package P–Spice the parameters of the 0.5 μm technology bipolar transistor models were used.

When simulating a full ADC system with sample and hold, folding and interpolation circuits, it is important to compare the input signal with the signal which was reproduced according to the output 8–bit binary code of the converter. For this purpose a digital–to–analog converter should be used. In this work we simulate the DAC function by the P–Spice package using an empirical equation (1):

$$u_{ODI}(t) = u_{D0}(t) + 2u_{D1}(t) + 4u_{D2}(t) + 8u_{D3}(t) + \\ + 16u_{D4}(t) + 32u_{D5}(t) + 64u_{D6}(t) + 128u_{D7}(t), \qquad (1)$$

here $u_{ODI}(t)$ is the DAC „imitation" output voltage; $u_{D0} - u_{D7}$ are the digital output voltages of the simulated ADC.

In Fig. 2, alongside with the input sine signal the signal reproduced from the binary code D0–D7 is presented, which is calculated by the following empirical equation:

$$u^*_{ODI}(t) = \frac{u_{ODI}(t)}{32} - U_0, \qquad (2)$$

here $U_0 = 23{,}5$ V.

As it can be seen in Fig. 2, the analog signal reproduced from the ADC output binary code agrees well with the input sine signal. Pulse peaks in the reproduced

sine signal appear due to inaccuracies of compatibility of ADC delay circuits.

By simulating the folding – interpolating ADC the time characteristics of output signals D0–D7 were also obtained at different input analog signal frequencies (5, 10, 15, 20, 30, 40, 50, 100, 500, 1000 MHz). The time characteristics of the converter output signals at 10, 20, and 40 MHz are shown in Fig. 4–6.

These characteristics show that the change range of the binary code 8–output signals is from 3.1 to 3.3 V at input signal frequencies up to f_{max} = 10 MHz. By further increasing the frequency, the pulse amplitudes of lowest bits decrease (Fig. 5, 6).

Having analyzed time diagrams of the converter output signal, the dependence of the effective number of bits change on the frequency of the input analog signal was determined (Fig. 3).

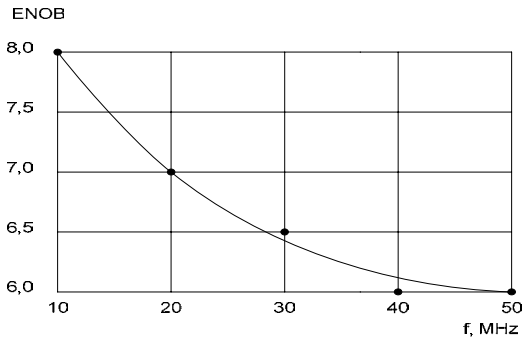

Fig. 3. Dependence of the effective number of bits (ENOB) on the input signal frequency f

The characteristic in Fig. 3 shows that the effective number of bits of the created folding – interpolating converter is 8 bits at the input signal maximum frequency of 10 MHz. By increasing the input signal frequency, the number of effective bits decreases and the accuracy of 6 bits is obtained at the input signal frequency of 50 MHz. The frequency can be improved by using transistor models of more advanced technology (SiGe or CMOS 0.35 μm) or by reducing the folding and interpolation coefficients.

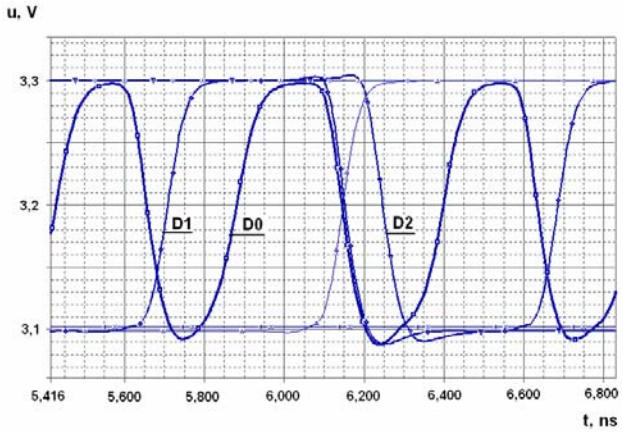

Fig. 4. ADCS output signals at the 10 MHz input frequency

As it can be seen in Fig. 4, all eight digital output signals fit into the range from 3.1 to 3.3 V. By predetermining the understandable error of 10 % according to voltages, we still see that the error is not exceeded. Thus, the number of effective bits is equal to 8 bits.

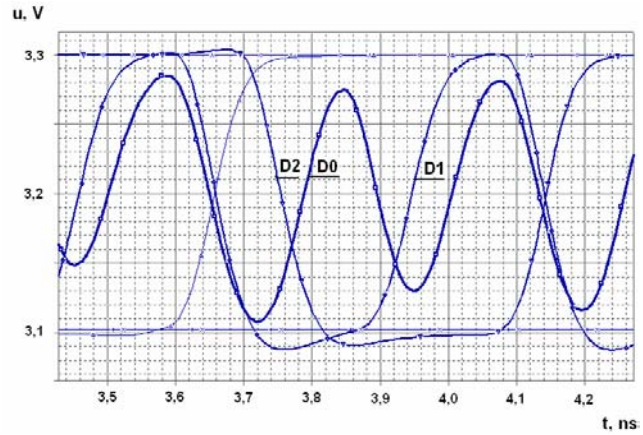

Fig. 5. ADC output signals at the 20 MHz input frequency

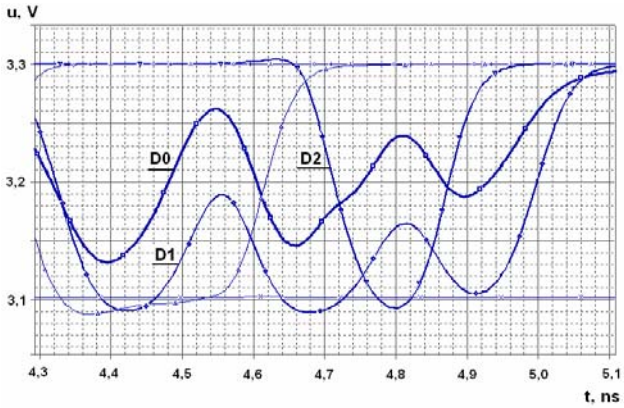

Fig. 6. ADC output signals at the 40 MHz input frequency

By simulating by computer with the Pentium 4 processor, the clock frequency of which is 3 GHz and RAM of 1 GB, one cycle of the transient process simulation lasted about 8 hours when calculating a full input signal sinusoid (Fig. 2) and about 1 hour when calculating short time periods (Fig. 4–6).

Conclusions

The structure of the folding and interpolating analog–to–digital converter was created, which includes the signal sample and hold, folding and interpolating circuits, the electric schemes of which are formed on the basis of bipolar silicon transistors.

The methodology of simulating dynamic characteristics of the 8–bit binary converter was developed as well as dynamic characteristics of the converter with signal transformation circuits were simulated and parameters were investigated.

It has been determined that the maximum number of bits per second of such a converter reaches $4 \cdot 10^9$, and the number of effective bits is 8 when the analog signal maximum frequency is 10 MHz. By increasing the analog signal frequency, the number of effective bits decreases and it is equal to 4 at 100 MHz. The analog signal maximum frequency of the folding – interpolating ADC

can be increased by reducing the folding and interpolating coefficients. The investigation has shown that when the interpolation coefficient is K = 4 and the folding coefficient is M = 3, the analog signal f_{max} for the 8–bit converter can be about 1 GHz. The converter speed would increase by improving parameters of the transistor models.

References

1. **Marcinkevičius A., Jasonis V.** Analoginės atminties schemos parametrų skaičiavimas signalo laikymo veikoje // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2006. – Nr. 2 (66). – P. 31 – 35.
2. **Jasonis V., Poviliauskas D., Marcinkevičius A.** Simulation of the Integrated Signal Folding Circuit with P–Spice // Electronics and Electrical Engineering. – Kaunas: Technologija, 2007. – No. 1 (73). – P. 37 – 40.
3. **Marcinkevičius A., Jasonis V.** Calculation of Interpolation Parameters in the Comparator Analog Information Converters // Electronics and Electrical Engineering. – Kaunas: Technologija, 2006. – No. 5 (69). – P. 5 – 8.
4. **Marcinkevičius A., Jasonis V.** The Calculation of Dynamic Errors in Signal Transformation Circuits of Analog – to – Digital Converters for Mechatronic Systems // Solid State Phenomena. – Trans Tech Publications, Switzerland, 2006. – Vol. 113. – P. 131 – 136.
5. **Vessal F., Salama C. A. T.** An 8–Bit 2–Gsample/s Folding–Interpolating Analog–to–Digital Converter in SiGe Technology // IEEE Journal of Solid – State Circuits, 2004. – Vol. 39, No. 1. – P. 238 – 241.
6. **Li Y., Sanchez–Sinencio E.** A Wide Input Bandwidth 7–bit 300–Msample/s Folding and Current–Mode Interpolating ADC // IEEE Journal of Solid – State Circuits, 2003. – Vol. 38. – No. 8. – P. 1405 – 1410.
7. **Liu M. H., Liu S. I.** An 8–bit 10 MS/s Folding and Interpolating ADC Using the Continous–Time Auto–Zero Technique // IEEE Journal of Solid – State Circuits, 2001. – Vol. 36. – No. 1. – P. 122 – 128.

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The structure of the folding and interpolating analog-to-digital converter, which includes the signal sample and hold, folding and interpolating circuits, the electric circuits of which are formed on the basis of silicon bipolar transistors of the 0.5 μm technology, is presented. The methodology of simulation of dynamic characteristics of the created 8-binary bit converter and calculation of the digital output signal form was developed. The results of simulation of dynamic characteristics of the converter with signal transformation circuits and investigation of frequency parameters are presented. It has been determined that the maximum number of samples per second of such a converter reaches $4 \cdot 10^9$, and the number of effective bits with the analog signal maximum frequency of 10 MHz is 8. It has been shown that by increasing the analog signal frequency the number of effective bits of the converter decreases and at the 50 MHz frequency it is equal to 6. The investigations have shown that the analog signal maximum frequency of the folding-interpolating ADC can be increased by reducing the folding and interpolation coefficients. When the interpolation coefficient is K = 4 and the folding coefficient is M = 3, the analog signal f_{max} for the 8-bit converter could be about 1 GHz. Ill. 6, bibl. 7. (in English; summaries in English, Russian and Lithuanian).

А. И. Марцинкявичюс, В. Ясонис, Д. Повиляускас. Моделирование сигналов в интегральном свёрточно интерполяционном АЦП // Электроника и электротехника. – Каунас: Технология, 2007. – № 5(77) . – С. 29–32.

Приведена структура свёрточно интерполяционного АЦП (СИАЦП), в состав которого входит устройство выборки и хранения, схемы свёртки и интерполяции сигнала. Электрические схемы разработаны на биполярных транзисторах с параметрами моделей при 0,5 микронной технологии. Создана методика моделирования динамических характеристик и расчета сигналов восьмиразрядного СИАЦП. Представлены результаты исследования частотных характеристик и основных точностных параметров такого АЦП. Показано, что максимальная частота выборки достигает 4 ГГц, и при частоте аналогового сигнала 10 МГц обеспечивается восьмиразрядная точность преобразования. Установлено, что при увеличении максимальной частоты аналогового сигнала точность преобразования уменьшается и при частоте 50 МГц падает до 6 разрядов. Исследования показали, что дальнейшее увеличение быстродействия СИАЦП возможно при уменьшении коэффициентов свёртки и интерполяции цепей трансформации аналогового сигнала. При коэффициенте интерполяции K = 4 и коэффициенте свёртки M = 3, восьмиразрядная точность может быть получена при максимальной частоте аналогового сигнала около одного ГГц. Ил. 6, библ. 7 (на английском языке; рефераты на английском, русском и литовском яз.).

A. J. Marcinkevičius, V. Jasonis, D. Poviliauskas. Signalų modeliavimas sąsūkos ir interpoliacijos integriniame ASK // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2007. – Nr. 5(77). – P. 29–32.

Pateikta sąsūkos ir interpoliacijos analoginio-skaitmeninio keitiklio sandara. Į jį įeina signalų imties ir laikymo, sąsūkos ir interpoliacijos grandynai, kurių elektrinės schemos sudarytos silicio dvipolių tranzistorių pagrindu, esant 0,5 mikrometro technologijai. Sudaryta sukurto 8 dvejetainių skilčių keitiklio dinaminių charakteristikų modeliavimo ir skaitmeninių išėjimo signalų formos skaičiavimo metodika. Pateikti keitiklio su signalo transformacijos grandinėmis dinaminių charakteristikų modeliavimo ir dažninių parametrų tyrimo rezultatai. Parodyta, kad tokio keitiklio maksimalus imčių skaičius per sekundę siekia $4 \cdot 10^9$, o efektyviųjų bitų skaičius, kai analoginio signalo maksimalus dažnis 10 MHz, lygus aštuoniems. Parodyta, kad, didinant analoginio signalo dažnį, keitiklio efektyviųjų bitų skaičius mažėja ir, esant 50 MHz, lygus 6. Tyrimais nustatyta kad sąsūkos ir interpoliacijos ASK analoginio signalo maksimalų dažnį galima padidinti mažinant sąsūkos ir interpoliacijos koeficientus. Esant interpoliacijos koeficientui K = 4 ir sąsūkos koeficientui M = 3, analoginio signalo f_{max} 8 bitų keitikliui galėtų būti apie 1 GHz. Il. 6, bibl. 7 (anglų kalba; santraukos anglų, rusų ir lietuvių k.).