ELECTRONICS AND ELECTRICAL ENGINEERING
ISSN 1392 – 1215 *2006. Nr. 6(70)*
ELEKTRONIKA IR ELEKTROTECHNIKA

MICROELECTRONICS
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MIKROELEKTRONIKA

Nanotechnology Problems using VMOS, UMOS

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Introduction

VMOS, UMOS („V“–groove – metal – oxide – silicon) transistors drain and gate are formed in the groove of “V” or “U” form. Expanding channel area, therefore VMOS and UMOS structures may be used in the power chips. Using VMOS, UMOS means saving 40% more of free space than using NMOS technology.

Nanostructures dimensions are very small, so it is important to keep pn splice at a right depth, during the all semiconductor manufacturing technological process.

For analyzing of influence of each technological operation on structure formation, mathematical simulation program SUPREM IV is used. VMOS and UMOS technological operation was simulated in micro and nano level.

VMOS, UMOS structure

MOS transistor structure is two dimensional–planar. VMOS and UMOS transistor structure is three-dimensional. Drain and gate are formed in the groove of “V” and “U” shape. Source area is just in the surface of the substrate (Fig. 1).

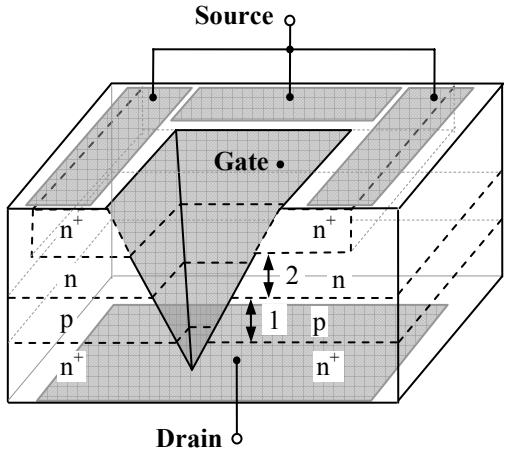

Fig. 1. Structure of VMOS transistor: 1 – channel; 2 – electron drift region

Drain is using n^+ layer like earthen bus, therefore decreasing used space on the silicon substrate. Channel in the VMOS transistor is placed through all perimeter of “V”-groove. Such transistor has high source current.

Etching process proceeds until the groove of pyramid form crosses doped n^+, diffusion n type and epitaxial p type layers. The top of the pyramid must reach n^+ layer. The layer of p type is 1 μm thick. This layer realizes VMOS and UMOS transistor channel [1].

Mathematical simulation of VMOS, UMOS technological processes

Using program SUPREM IV [2] VMOS technological process simulation was performed. VMOS manufacturing begins from n^+ plate (phosphorus concentration $1.0 \cdot 10^{17}$ at./cm^3) boron doping. Boron doping is carried out at 1000 ºC temperature, 20 min at $1.0 \cdot 10^{17}$ at./cm^3 gas concentration. Epitaxial n conductance and 3 μm thickness layer (phosphorus concentration $1.0 \cdot 10^{14}$ at./cm^3) is formed after boron doping operation. Thin SiO_2 layer is formed at 1000 ºC temperature, 10 min and in the dry O_2. 0.2 μm thickness Si_3N_4 layer is deposited on the thin SiO_2 layer. Then photolithography is performed and windows are opened for ion implantation. Boron implantation dose is $1.0 \cdot 10^{12}$ C/cm^2, energy – 90 keV. Two boron doped layers are obtained: upper – using ion implantation, lower – using diffusion method.

All these conditions of technological processes determinate boron impurities distribution (Fig. 2).

After boron doping operation, LOCOS oxide layer is formed using local oxidation in the wet O_2, 1000 ºC temperature and 100 min. Windows for n^+ regions are created using photolithography. Resulting regions will be the source of the transistor. Using arsenic ion implantation sources are formed. Arsenic implantation dose is $1.0 \cdot 10^{14}$ C/cm^2, energy – 150 keV. Then, on the source regions LOCOS oxide layer is formed. Oxidation is preceding in wet O_2, at 1000 ºC temperature 100 min. After oxidation “V“-grooves are etched, growing 0.1 μm thickness SiO_2

layer, etching contacting windows and forming 0.1 μm thickness aluminum film.

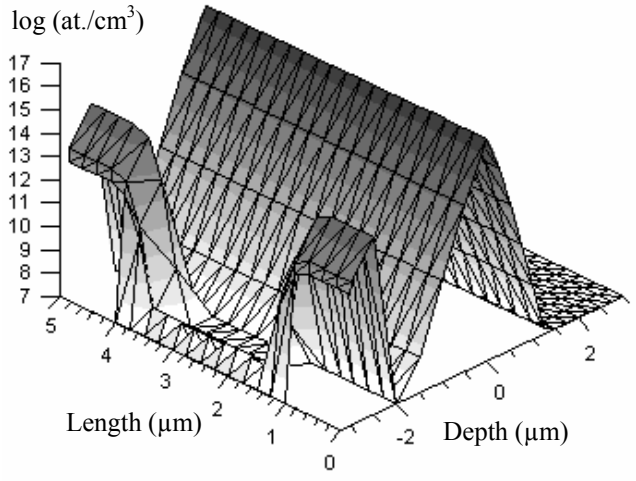

Fig. 2. Mathematical simulation results: chemical boron concentration before LOCOS oxide forming

Impurities distribution and pn splices regions localization demonstrate that the impurities mostly distribute after LOCOS oxide forming technological process (Fig. 3) [3]. The comparison of 2 and 3 figures shows, that then performing high temperature oxidation process, boron impurities diffuse from high-doped regions to adjacent layers.

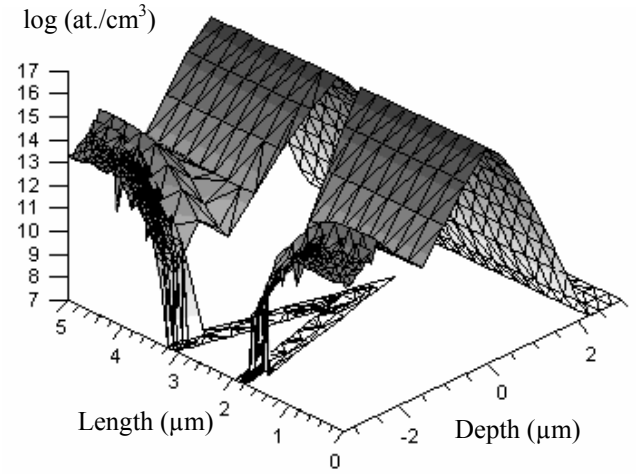

Fig. 3. Mathematical simulation results: chemical boron concentration after LOCOS oxide forming

In this instance, pn splices variation after oxidation reaction is very small, because VMOS semiconductor dimensions are big enough. Impurities re-distribution after high-temperature process producing nano-semiconductors is very important, because due to thermal diffusion, atoms penetrations depth orthogonal and standard deviations emerge. In order to prevent thermal impurities diffusion effect new methods are searched. One of solutions is to reduce number of high-temperature technological processes in semiconductors manufacturing process.

Phosphorus and arsenic impurities distribution producing VMOS transistor is given at Fig. 4 and 5. VMOS structure layers situation is given in Fig. 6. Channel length $L \approx 1$ μm, electron drift region $l \approx 0.8$ μm.

Comparing UMOS and VMOS structures from technological viewpoint, it is easier to make "U" form groove than "V" form groove.

VMOS and UMOS technology take seven photolithographic operations whereas NMOS typical technology takes six photolithographic operations

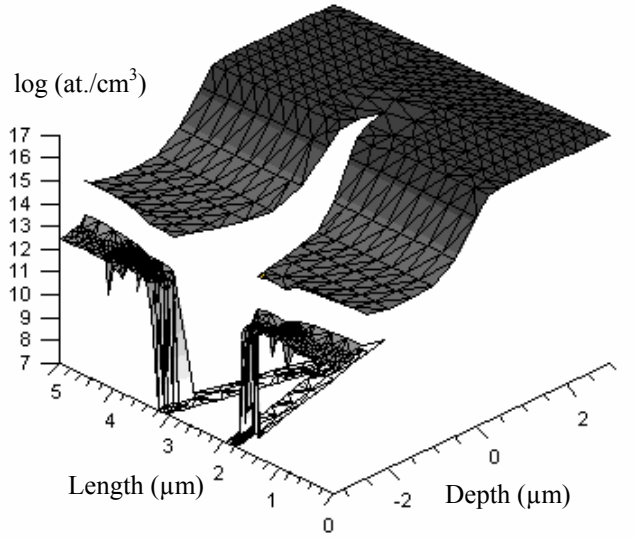

Fig. 4. Mathematical simulation results: chemical phosphorus concentration after LOCOS oxide forming

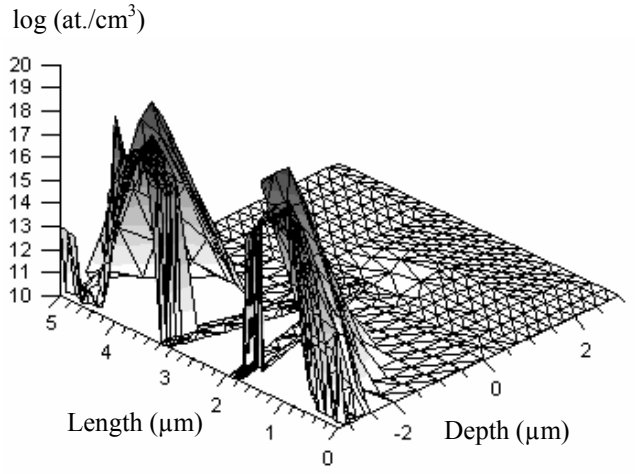

Fig. 5. Mathematical simulation results: chemical arsenic concentration

VMOS, UMOS structures in nanotechnology

Manufacturing of nanostructures is starting with n^+ conduction Si plate (phosphorus ion concentration $1.0 \cdot 10^{17}$ at./cm^3) boron doping as in the usual VMOS, UMOS industrial technology. The boron doping is processing at the 700 ºC degrees temperature, 1 min at $1.0 \cdot 10^{17}$ at./cm^3 gas concentration. Thus p conduction areas are formed.

Temperature and required time depends on proper doping degree and depth. Dimensions of manufactured nano-structures are very small. Consequently, tight control of the depth of the impurities penetration and their separation must be exercised using high temperature

technological processes. In this way, temperature and time of boron doping operation are signally lesser than in the usual VMOS, UMOS manufacturing technological process.

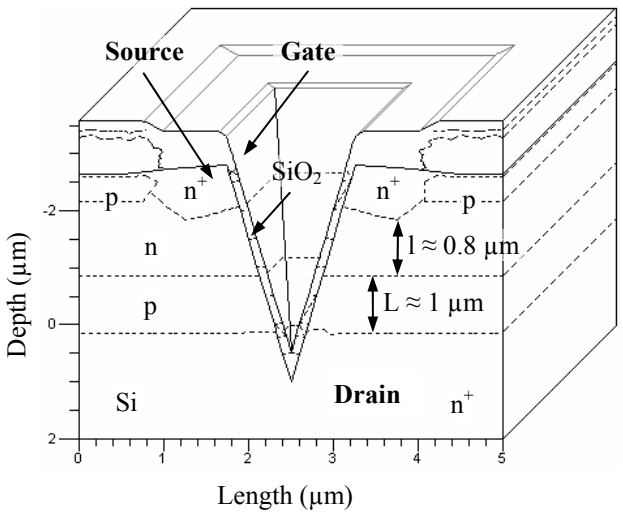

Fig. 6. Mathematical simulation results: VMOS structure layers situation

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After boron doping operation epitaxial n conduction 80 nm thickness layer is being formed (phosphorus ion concentration $1.0 \cdot 10^{14}$ at./cm^3). Above it thin SiO_2 layer at 950 ºC temperature, 2 min and in the dry O_2 is formed. Onto the SiO_2 layer Si_3N_4 layer is deposited thickness of which is 20 nm. Then photolithography is performed and windows opened for boron impurities doping. Usually in this stage the ion implantation is used. If the depth of boron doping is very small, the operation is complicated.

After making mathematical simulation of Si surface boron doping process, it is true to say, that lesser doping depth available when using thermal impurities diffusion. For getting deeper doping depths it is advisable to use ion implantation technology.

Ion and semiconductor atoms influence probability increase at ion implantation. Semiconductor crystal structure is braking due to this influence. Braked areas – clusters – are formed dimension of which are 5 – 10 nm. Clusters make interconnections when doping dose is high. Therefore, large amorphous areas form. Clusters re-crystallize by plate annealing at 600-800 ºC degree temperature [4, 5].

For forming nano- VMOS, UMOS structures 10nm boron doping impurities depth is necessary. It is done by using the boron impurities diffusion at the 900 ºC degrees temperature, 1 min at $1.0 \cdot 10^{22}$ at./cm^3 gas concentration.

The advantages of diffusion – it comes easy to adjust and control such parameters like pn splice depth, surface impurities concentration and impurities distribution [4].

After boron doping operation using local oxidation at 800 ºC degree temperature, 10 min and in the dry O_2, LOCOS oxide layer is formed. By means of the photolithography windows are opened for n^+ area forming which will be source's areas. For making source's n^+ areas arsenic impurities are used which are inserted using diffusion at the 800 ºC degrees temperature, 10 min at $1.0 \cdot 10^{22}$ at./cm^3 gas concentration.

One more oxidation reaction after arsenic doping is not performed, contrarily to micro-VMOS and UMOS structures formation. Total impurities re-distribution occurs and formed pn splices disappear. This oxidation reaction is used for LOCOS oxide layer rising.

Mathematical simulation using program SUPREM IV results of nano-VMOS and UMOS manufacturing technological operations is illustrated in Fig. 7–10. Channel length L ≈ 15 nm, electron drift region l ≈ 50 nm.

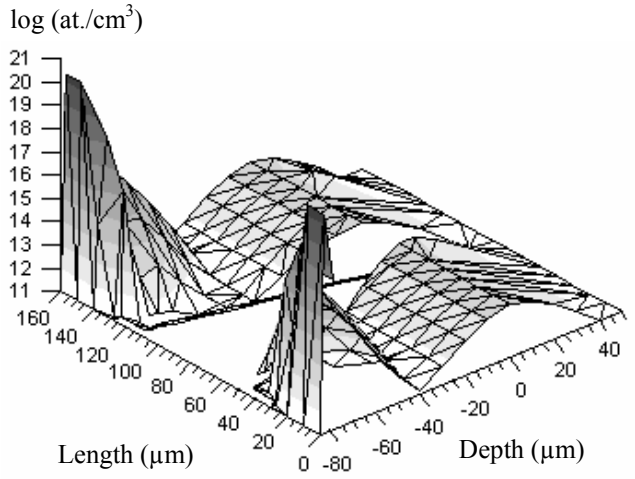

Fig. 7. Mathematical simulation results: chemical boron concentration

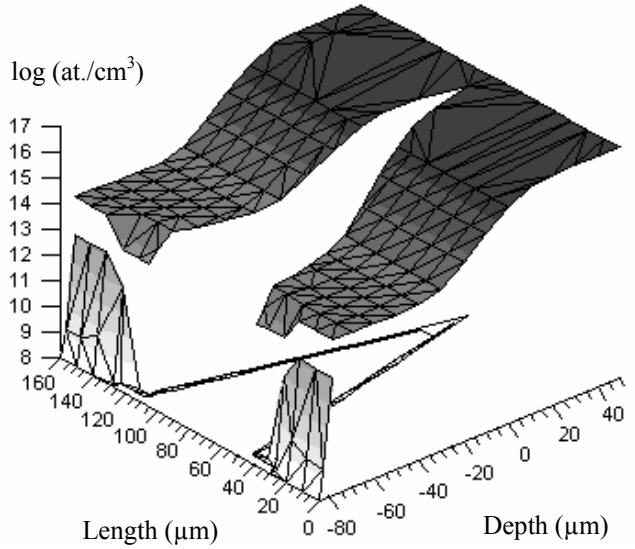

Fig. 8. Mathematical simulation results: chemical phosphorus concentration

Conclusions

1. To use ion implantation forming nano-structures is getting complicated due to small doping depth.

2. After making mathematical simulation with program SUPREM IV of Si area boron doping process, it was noticed, that for getting lesser doping depths it is advisable to use thermal impurities diffusion neither ion implantations technology.

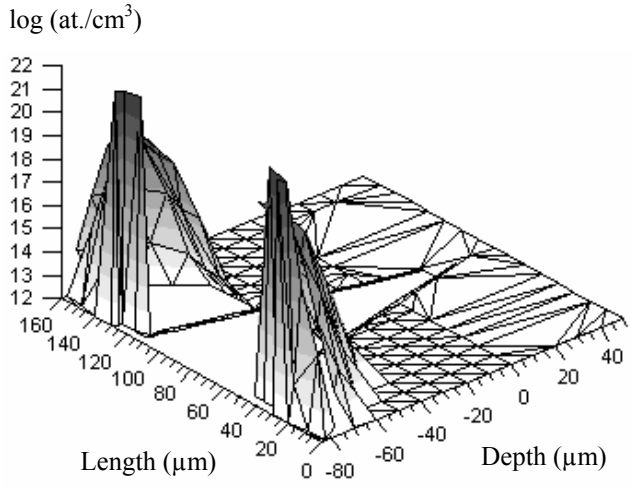

Fig. 9. Mathematical simulation results: chemical arsenic concentration

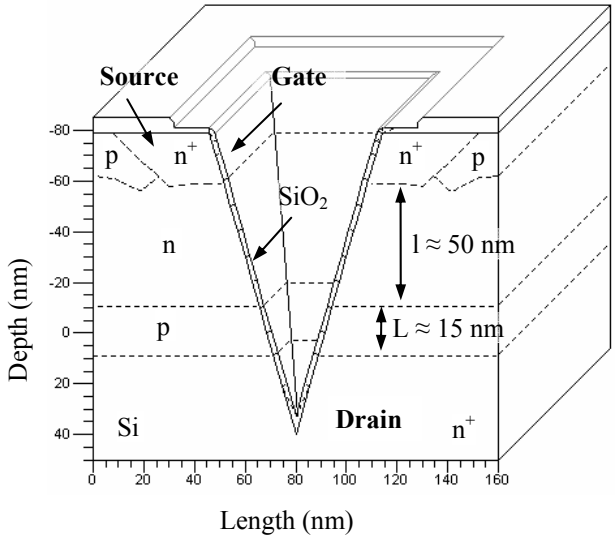

Fig. 10. Mathematical simulation results: VMOS structure layers situation

3. Impurities re-distribution after high-temperature process is important when producing nano-semiconductors, because due to thermal diffusion atoms penetrations depth orthogonal and standard deviations arise.

4. To prevent thermal impurities diffusion effect new methods are searched. As one of solutions – high-temperature technological processes number reduction at semiconductors manufacturing process.

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Submitted 2006 03 02

T. Keršys, D. Andriukaitis, R. Anilionis. Nanotechnology Problems using VMOS, UMOS // Electronics and Electrical Engineering. – Kaunas: Technologija, 2006. – No. 6(70). – P. 79 –82.

VMOS, UMOS transistors drain and gate are formed in the groove of "V" or "U" form. Channel area is expanded, therefore VMOS and UMOS structures may be used in power chips. Using VMOS, UMOS 40% more free space is saved than using NMOS technology. Nanostructures dimensions are very small, so it is important to keep pn splice at a right depth, during all semiconductor manufacturing technological process. Analyzing influence of each technological operation on structure formation mathematical simulation with program SUPREM IV is used. VMOS and UMOS technological operation was simulated in micro and nano levels. Ill. 10, bibl. 5 (in English; summaries in English, Russian and Lithuanian).

Т. Кяршис, Д. Андрюкайтис, Р. Анилёнис. Проблемы в нанотехнологии используя VMOS, UMOS // Электроника и електротехника. – Каунас: Технология, 2006. – №. 6(70). – С. 79 –82.

Исток и сток VMOS, UMOS транзисторов сформированы в ячейке "V" или "U" формы. Используя VMOS, UMOS можно сэкономить на 40% больше площади чем используя NMOS технологию. Габариты наноструктур очень малы, поэтому pn области очень важно удержать в нужной глубине во время всего технологического процесса производства интегрального элемента. Для анализа влияния каждой технологической операции на изменения сформированных структур использована программа математического моделирования SUPREM IV. VMOS и UMOS технологические процессы моделированы на микро и нано- уровнях. Ил. 10, библ. 5 (на английском языке; рефераты на английском, русском и литовском яз.).

T. Keršys, D. Andriukaitis, R. Anilionis. Nanotechnologijų problemos formuojant VMOS, UMOS // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2006. – Nr. 6(70). – P. 79 –82.

VMOS, UMOS tranzistoriaus ištaka ir užtūra formuojama „V" arba „U" formos duobutėje, gaunamas didelis kanalo plotas, todėl VMOS ir UMOS struktūras galima naudoti galingose mikroschemose. Naudojant VMOS, UMOS, sutaupoma maždaug 40% daugiau ploto negu naudojant NMOS technologiją. Nanostruktūrinių darinių matmenys yra labai maži, todėl svarbu skirtingo laidumo pn sritis išlaikyti reikiamą gylį viso integrinio grandyno gamybos proceso metu. Analizuojant kiekvienos technologinės operacijos įtaką formuojamos struktūros pokyčiams, panaudota matematinio modeliavimo programa SUPREM IV. VMOS ir UMOS gamybos technologiniai procesai modeliuojami mikro- ir nanolygmenyse, Il. 10, bibl. 5. (anglų kalba, santraukos anglų, rusų ir lietuvių k.).