ELECTRONICS AND ELECTRICAL ENGINEERING

ISSN 1392 – 1215 *2006. Nr. 5(69)*

ELEKTRONIKA IR ELEKTROTECHNIKA

ELECTRONIC

T170

ELEKTRONIKA

Structural Model of Electronic Device Manufacturing Process Quality

A. Žickis

Department of Electronics Engineering, Kaunas University of Technology,
Studentų str. 50, LT-51368 Kaunas, Lithuania, tel. +370 37 351389, e–mail: andrius.zickis@gmail.com

Introduction

During optimization of entirety of electronic device (ED) manufacture and control processes, it is required to form the structural model of quality of these processes, to select manufacture efficiency indexes, assess influence of separate process components on the quality of the product, manufacture efficiency and control. This need is conditioned by interaction between ED component features, interconnections between technological manufacture processes (TP) and integral impact of these processes on the quality of produced device. ED manufacture quality control is the alternative to the decisions of systemic quality transfer model. With increase of model complexity and systematic level the demands for the performance of control measures (analysis and decision-making models), memory and information amounts and its systematization also rapidly increases. Therefore it falls to select rational (at least technically acceptable) level of model systematic (complexity) [1]. Even though modeling principles in essence remain traditional, but the structure of model itself and dependencies are determined by the features of manufactured ED. During assembly of printed circuit board based ED units from separate structure-level components (so-called radio elements) corresponding structure model [2] is formed. At the present time such model is suitable only for the final stages of ED assembly. Considerably larger part of manufacture process consists of microcomponent manufacture TP. Quality transfer functions of these TP have not been modeled yet.

The formation structural quality model of microcircuit manufacture process

During investigation of this model many quality requirements for the component distribution, component compatibility (according to their reliability) achievement and other problems emerge. Let's try to form such a model. Each TP or its component provides a respective probability of defect-free manufacture, is used by different intensity, and resources are needed in order to increase its quality. Thus, it is needed to solve problems of systemic synthesis during synthesis of TP or their entirety.

It is possible to analyze the microcircuit manufacture using the conception of quality transfer function of each TP (or its component), and it is possible to form requirements for each TP or its component by using microcircuit quality requirements. After input control, the raw materials, materials, semi-manufactures and purchased assembly elements, which are characterized by quality parameters $\beta(t)$, during TP form a microcircuit with quality parameter [2]

$$m(t) = W(t) \cdot \beta(t); \qquad (1)$$

here $W(t)$ – TP quality transfer function (it is determined by TP component quality indexes).

Let's select a part of microcircuit manufacture process, structure of which is presented in Fig. 1.

In Fig. 1: M0 – storage processes of materials (raw materials); M1÷6 – material usage in various TP. T1.(1÷5) – substrate manufacturing TP: T1.1 – monocrystal growing; T1.2 – cutting of semiconductor chip into plates; T1.3 – plate cutting; T1.4 – plate polishing; T1.5 – plate control. T2 – plate cleaning; T3 – substrate coating with oxide layer. T4.(1÷9) – TP of the 1st photolithography: T4.1 – preparation of plate surface; T4.2 – coating using photoresist (PR) layer; T4.3 – drying of PR layer; PR exposing (T4.4a – contact photolithography; T4.4b – projection photolithography); T4.5 – development of PR layer; T4.6 – fixation of PR layer; T4.7 – layer etching through PR mask; T4.8 – PR removal; T4.9 – PR removal from renewed plates. T5(K2) – visual control of the 1st photolithography.

In this figure solid lines represent manufacture TP, numbers of which are indicated at the left (bottom), and their quality (non-defectivity) indexes – at the right side (bottom). Control processes are denoted by rectangles of dashed and solid lines. Probabilities of process being defective are shown in the circles, and material and raw material rejection probabilities (when they are taken from storages) – by ellipses. Dashed line rectangles symbolize material and raw material usage processes during manufacture. $\{q_{Mi}\}$ – defectivity of *i*–material (raw

material) conditioned by storage accumulation. $q_{M(Mi)}$ – overall (after storage operations) defectivity level of i – material (raw material).

Let's form a quality transfer function of a part of microcircuit manufacture process.

Let's estimate microcircuit substrate manufacture quality parameters $m_{T1.(1\div5)}$.

$$m_{T1.1}(t) = W_{T1.1}(t) \cdot \beta'_{M1}(t); \quad (2)$$

$$\beta'_{M1}(t) = 1 - q'_{M1}(t); \quad (3)$$

$$W_{T1.1}(t) = 1 - q_{T1.1}(t); \quad (4)$$

$$q'_{M1}(t) = f_{M1}[q_{M(M1)}(t), q_{M1}(t), t], \quad (5)$$

here $q'_{M1}(t)$ – defectivity level of handling process of a group of materials; $q_{T1.1}$ – process efficiency level; f_{M1} – $q'_{M1}(t)$ dependence on $q_{M(M1)}(t)$ and $q_{M1}(t)$ etc.

All remaining q'_M will be found analogously

$$m_{T1.2}(t) = W_{T1.2}(t); \quad (6)$$

here

$$W_{T1.2}(t) = 1 - q_{T1.2}(t). \quad (7)$$

Quality parameters of remaining TP (plate abrasion, plate polishing) are found in the same manner as in case of quality parameter $m_{T1.2}(t)$. Quality parameter of all TP before the first control is found:

$$m_{T1.(1\div4)}(t) = m_{T1.1}(t) \cdot m_{T1.2}(t) \cdot m_{T1.3}(t) \cdot m_{T1.4}(t). \quad (8)$$

Quality parameter of the first control and after that – quality parameter of entire plate manufacture is expressed as:

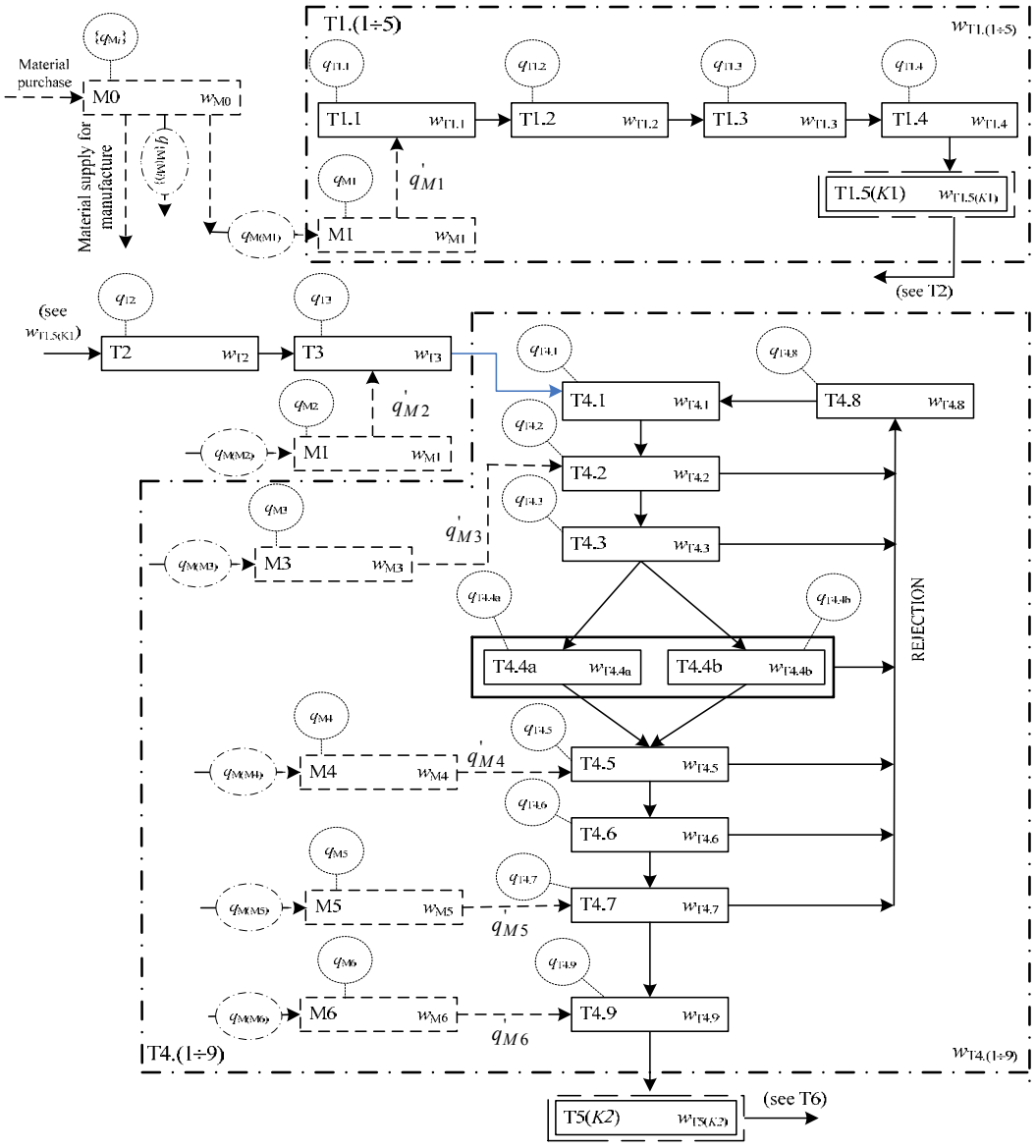

Fig. 1. Structural diagram of manufacture processes of a part of microcircuit

$$m_{T1.5(K1)}(t) = 1 - \left(1 - m_{T1.(1\div4)}(t)\right) \cdot \frac{a_{K1}(t)}{\sqrt{n_{K1}}}; \quad (9)$$

$$a_{K1}(t) = \frac{q_{K1}(t)}{1 - m_{T1.(1\div4)}(t)}; \quad (10)$$

$$m_{T1.(1\div5)}(t) = m_{T1.5(K1)}(t) = W_{T1.(1\div5)}(t); \quad (11)$$

here n_{K1} – number of control operations; $a_{K1}(t)$ – rejection level after TP, after which control operation is applied; $q_{K1}(t)$ – the level till which the rejection probability is decreased by K1 control operation.

$$m_{T2}(t) = W_{T2}(t); \quad (12)$$

$$m_{T3}(t) = W_{T3}(t) \cdot \beta'_{M2}(t); \quad (13)$$

here

$$\beta'_{M2}(t) = 1 - q'_{M2}(t); \quad (14)$$

$$W_{T3}(t) = 1 - q_{T3}(t). \quad (15)$$

Let's try to express quality parameter of the 1st photolithography $m_{T4.(1\div9)}(t)$. First we find the amount of production $((b_{T4.8}(t))$, which enters the $T4.8$ process repeatedly (see Fig. 1)

$$b_{T4.8}(t) = q^{(')}_{T4.2}(t) + q_{T4.3}(t) + q_{T4.4a}(t) + q^{(')}_{T4.5}(t) + q_{T4.6}(t) + q^{(')}_{T4.7}(t); \quad (16)$$

here

$$q^{(')}_{T4.2}(t) = 1 - m_{T4.2}(t) = 1 - \left(W_{T4.2}(t) \cdot \beta'_{M3}(t)\right); \quad (17)$$

$$q^{(')}_{T4.5}(t) = 1 - m_{T4.5}(t) = 1 - \left(W_{T4.5}(t) \cdot \beta'_{M4}(t)\right); \quad (18)$$

$$q^{(')}_{T4.7}(t) = 1 - m_{T4.7}(t) = 1 - \left(W_{T4.7}(t) \cdot \beta'_{M5}(t)\right). \quad (19)$$

Let's find the quality parameter of plate preparation process for the 1st photolithography

$$m_{T4.1}(t) = \eta_{T4.1} \cdot W_{T4.1}(t) + \eta_{T4.8} \cdot W_{T4.8}(t) \cdot W_{T4.1}(t) = W_{T4.1}(t) \cdot (\eta_{T4.1} + \eta_{T4.8} \cdot 1); \quad (20)$$

here $\eta_{T4.1}$ and $\eta_{T4.8}$ are flow significance coefficients.

Production flow significance coefficients after plate surface preparation and photoresist removal from renewed plates are calculated

$$\eta_{T4.1} = \frac{1}{1 + b_{T4.8}}, \text{ o } \eta_{T4.8} = \frac{b_{T4.8}}{1 + b_{T4.8}}. \quad (21)$$

Further quality parameters of the other process are evaluated

$$m_{T4.2}(t) = W_{T4.2}(t) \cdot \beta'_{M3}(t); \quad (22)$$

$$m_{T4.3}(t) = W_{T4.3}(t). \quad (23)$$

When searching for photoresist exposing quality parameter it is possible to select contact or projection photolithography. In both cases the quality parameter is calculated analogously. We select contact photolithography

$$m_{T4.4a}(t) = W_{T4.4a}(t). \quad (24)$$

$T4.5$ process quality parameter is estimated next

$$m_{T4.5}(t) = W_{T4.5}(t) \cdot \beta'_{M4}(t). \quad (25)$$

Quality parameters of all other processes are described analogously as already mentioned parameters. Now we will write the quality parameter of entire first photolithography before the visual control

$$m_{T4.(1\div9)}(t) = m_{T4.1}(t) \cdot m_{T4.2}(t) \cdot m_{T4.3}(t) \cdot m_{T4.4}(t) \times \times m_{T4.5}(t) \cdot m_{T4.6}(t) \cdot m_{T4.7}(t) \cdot m_{T4.8}(t) \cdot m_{T4.9}(t). \quad (26)$$

After the 1st photolithography the quality parameter of the visual control:

$$m_{T5(K2)}(t) = 1 - \left(1 - m_{T4.(1\div9)}(t)\right) \cdot \frac{a_{K2}(t)}{\sqrt{n_{K2}}}; \quad (27)$$

here

$$a_{K2}(t) = \frac{q_{K2}(t)}{1 - m_{T4.(1\div9)}(t)}. \quad (28)$$

Indexes are the same as in (10).

Now we can already express the general quality level, which has been received after all microcircuit manufacture and control processes, indicated in the Fig. 1

$$m^*_{T5(K2)}(t) = m_{T1.5(K1)}(t) \cdot m_{T2}(t) \times \times m_{T3}(t) \cdot m_{T5(K2)}(t). \quad (29)$$

Quality level of the other (remaining) microcircuit manufacturing process part is calculated analogously. It can be shown, that this part additionally span $T_6 \div T_{45}$ processes, which are not presented here due to a limited size of the paper. Then general microcircuit quality level is expressed as:

$$m_{\Sigma}(t) = m^*_{T5(K2)(t)} \cdot \prod_{i=6}^{45} m_{Ti}(t); \quad (30)$$

here $m_{Ti}(t)$ quality parameter of TP with index i, considering the influence of control operations intended for some of them in the structural diagram.

Quality functions of printed circuit unit manufacture $(\{m_{SMi}(t)\})$ [3], ED assembly $(\{m_{Si}(t)\})$, adjustment $(\{m_{ri}(t)\})$ and other $(\{m_{KTi}(t)\})$ processes [4] are modeled analogously. In such manner integral ED quality model is received

$$m_{El}(t) = \prod_{i=1}^{n_M} m^{n_i}_{\Sigma i}(t) \cdot \prod_{j=1}^{n_{SM}} m^{n_j}_{SMj}(t) \cdot \prod_{v=1}^{n_S} m^{n_v}_{Sv}(t) \times \times \prod_{e=1}^{n_r} m^{n_e}_{Re}(t) \cdot \prod_{d=1}^{n_{KT}} m^{n_d}_{KTd}(t); \quad (31)$$

here n_M, n_{SM}, n_S, n_R ir n_{KT} – numbers of different microcircuits, printed circuit board assembly units,

assembly processes, adjustment processes and other processes in ED; n_i, n_j, n_v, n_e ir n_d – numbers of *i*-type microcircuits, *j*-PCB units and other components in ED.

The value of each model component (e.g. $m_{\Sigma i}(t)$) depends on the investors who invest in manufacture measures (e.g. $C_{gi}(t)$) and also depend on control of these measures (e.g. $C_{gvi}(t)$). Therefore

$$m_{\Sigma i} = f_{\Sigma i}\left(C_{gi}(t), C_{gvi}(t), t\right). \quad (32)$$

Then

$$m_{E\text{Į}}(t) = \prod_{i=1}^{n_M} m_{\Sigma i}^{n_i}(t) \cdot \left(C_{Mgi}(t), C_{Mgvi}(t), t\right) \times$$
$$\times \prod_{j=1}^{n_{SM}} m_{SMj}^{n_j}(t) \cdot \left(C_{SMgj}(t), C_{SMgvj}(t), t\right) \times$$
$$\times \prod_{v=1}^{n_S} m_{Sv}^{n_v}(t) \cdot \left(C_{Sgv}(t), C_{Sgvv}(t), t\right) \times$$
$$\times \prod_{e=1}^{n_R} m_{Re}^{n_e}(t) \cdot \left(C_{rge}(t), C_{rgve}(t), t\right) \times$$
$$\times \prod_{d=1}^{n_{KT}} m_{KTd}^{n_d}(t) \cdot \left(C_{KTgd}(t), C_{KTvd}(t), t\right). \quad (33)$$

Prices of separate component manufacture measures and prices of manufacture control are indicated in formula (33) in the brackets.

The global or partial ED manufacture quality level optimization is performed using this operator:

$$\max_{\substack{C_{gj} \\ C_{gvj}}} m_{E\text{Į}}(t) \Big| \Sigma(C_{gj} + C_{gvj}) \le C_u; \quad (34)$$

here C_u – provided assets for ED manufacture and its control.

It is possible to minimize expenses required by manufacture and its control, if appointed ED quality level is maintained.

Main objective of the further research – optimal complexity of ED manufacture process quality model.

Conclusions

There is a need for complex research of structural diagram of TP in order to achieve the optimal level of ED manufacturing quality. Separate TP quality level dependences on expenses determine the economical manufacture process optimization model. Big number of TP during ED manufacture determines the complexity of quality model, and at the same time it poses a problem of optimal model complexity.

References

1. **Balaišis P., Eidukas D., Valinevičius A., Žilys M.** Informacinių elektroninių sistemų efektyvumas. – Kaunas: Technologija, 2004. – 356 p.
2. **Eidukas D., Balaišis P.** Elektroninių įtaisų kokybė. – Kaunas: Technologija, 1998. – 232 p.
3. **Bagdanavičius N., Žickis A.** Efficiency of Electronic Device Manufacturing Process Control // // 26tn Int. Conf. Information Technology Interfaces ITI 2004, June 7-10, 2004, Cavtat, Croatia. ISSN 1330-1012. – P. 495–500.
4. **Stephen A. Campbell.** The Sciences and Engineering of Microelectronic Fabrication. – New York: Oxford University Press, 2001. – 603 p.

Submitted for publication 2006 03 07

A. Žickis. Structural Model of Electronic Device Manufacturing Process Quality // Electronics and Electrical Engineering. – Kaunas: Technologija, 2006. – No. 5(69). – P. 37–40.

It is offered to assess the level of manufacturing quality by using quality transfer functions of separate processes. A part of process structure of micro-circuit manufacturing was selected for modeling. Quality transfer function was created for a part of micro-circuit manufacturing process. Flow sizes of circulating ED components during manufacturing processes are considered when calculating this function. Overall micro-circuit quality level calculation technique and integral ED quality model was introduced. Operator for global or partial ED manufacturing quality level optimization was presented. Ill. 1, bibl. 4 (in English; summaries in English, Russian and Lithuanian).

А. Жицкис. Структурная модель качества производственного процесса электронных устройств // Электроника и электротехника. – Каунас: Технология, 2006. – №. 5(69). – С. 37–40.

Предложен метод оценки уровня качества процесса производства электронных устройств на основании передаточных функций качества его компонентов. В качестве примера составлена структурная схема процесса изготовления интегральных микросхем. Заданы функции передачи качества каждого этапа производства (с учетом качества предыдущих операций), на основании которых составлена модель всего процесса. Показана возможность оптимизации уровня качества производственного процесса по экономическому критерию. Ил. 1, библ.4 (на английском языке; рефераты на английском, русском и литовском яз.).

A. Žickis. Struktūrinis elektroninių įtaisų gamybos proceso kokybės modelis // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2006. – Nr. 5(69). – P. 37–40.

Siūloma gamybos kokybės lygį vertinanti, naudojant atskirų procesų kokybės perdavimo funkcijas. Modeliavimui pateikta dalis mikrograndyno gamybos proceso struktūros. Sudaryta mikrograndyno gamybos proceso dalies kokybės perdavimo funkcija. Apskaičiuojant šią funkciją atsižvelgiama į gamybos proceso cirkuliuojančių EĮ komponentų srautų dydžius. Pateiktas bendro mikrograndyno kokybės lygio apskaičiavimo metodas ir integrinis EĮ kokybės modelis. Pateiktas globalaus ar dalinio EĮ gamybos kokybės lygio optimizavimo operatorius. Il. 1, bibl. 4 (anglų kalba; santraukos anglų, rusų ir lietuvių kalbomis).