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Etching Process Simulation in MOS Nanoscale Structures

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Introduction

Integral circuit (IC) and their elements must be released with high precision.

After a photo mask has been created a layer under the resist is etched.

Etching process is described by etch rate – dimension of thickness per unit. A large etch rate is an advantage in technological process. Too high etch rate is treated as a lack, because it is difficult to control etching process. Etch process rate can commonly reach hundreds nanometers per minute [1, 2].

The lateral extent of etch under the photo resist mask is created. This is the biggest appearance in wet etching process. Wet etching is the slowest and less controllable etching process.

Si crystal lattice

Every technological process involves MOS transistors or IC, less or more. Every technological process related to the past one (for example: diffusion depends on wafer (crystal lattice) quality, which depends on technological process temperature) [3].

Crystal state of substance influence its structural elements – atoms of crystal lattice.

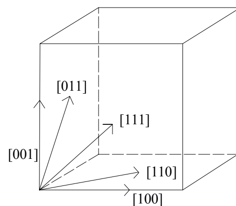

Fig. 1. Crystal orientations in the cubic system [2]

A crystal is an array of atoms, repeated in a regular manner in three dimensions. Crystal lattice has a cubic symmetry, when each edge of crystal lattice is of the same length. Every direction in a crystal can be characterized using three dimensional coordinate system – x, y, z. In a cubic crystal a formed crystallographic plane exists (over atoms) that is perpendicular to the vector which is going along the direction of three dimensional coordinate system – x, y, z (Fig.1). Crystallographic planes orientation is described using numbers x, y, z, which are known as Miller indices [2].

Silicon has the basic diamond crystal structure – two merged face centered cube (FCC) cells offset by a/4 in x, y, z.

MOS technological process

Micro relief of wafers makes influence on IC elements and their parameters. Substrates of high quality mono crystals are used for semiconductor manufacturing.

Wafer of semiconductor device has contrary conductance compare with channel of MOS transistor.

Performance of MOS transistors depends on the parasitic capacities and resistances (Fig. 2).

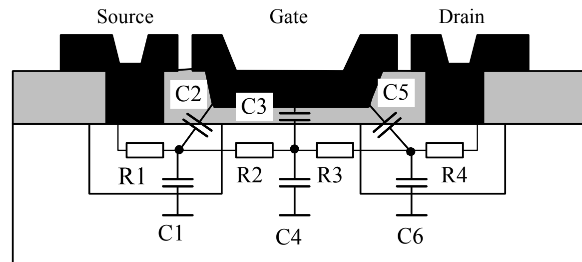

Fig. 2. Parasitic MOS transistors elements: R1 – source resistance; R2, R3 – spread gate channel resistance; R4 – drain resistance; C1 – source-substrate capacity; C2 – gate-source capacity; C3 – gate-channel capacity; C4 – channel-substrate capacity; C5 – gate-drain capacity; C6 – drain-substrate capacity

After input voltage has changed, current source changes slowly, because parasitic capacities must charge or discharge through parasitic resistances. Self charge or self discharge process is slowest if capacities and resistances increase.

In order to improve MOS structure the parameters of parasitic capacitances – gate-source, gate-drain – have to be minimized. In order to reduce parasitic capacitances we must avoid lateral diffusion, which is formed under the gate electrode. The size of the gate electrode must be the same during all technological processes in order to avoid source-drain channel shortening. The area of element formation must be the same during all technological

processes. Separation of MOS elements can be produced using local oxidation [4, 5] and silicon on sapphire technologies.

Local oxidation (*LOCOS (Local Oxidation of Silicon))* is used in MOS technology (Fig. 3). Thermically grown silicon oxide separates semiconductor elements. It is necessary to get hole with less lateral etched side wall. The lateral oxidation can be formed during local oxidation. Therefore length of the source-drain channel decreases, because source and drain regions can be moved under the gate. A large attention must be paid to this process [4].

Silicon on sapphire (*SOS* (*Silicon on Sapphire))* is an integrated circuit manufacturing technology. It is a hetero-epitaxial process that consists of a thin layer of silicon grown on a sapphire (Al_2O_3) wafer and etching of this epitaxial layer (Fig. 4).

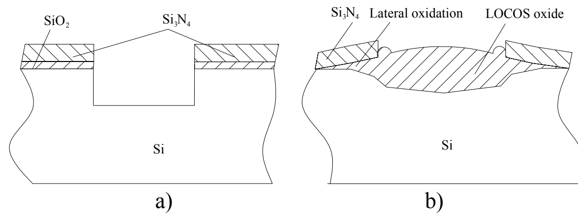

Fig. 3. LOCOS technology: a – hole etching; b – local oxidation of silicon

Created silicon regions are isolated by wafer from bottom and from the side by air space. It is necessary to avoid lateral encroachment during region formation, because "active" length of region where transistors are formed can be reduced.

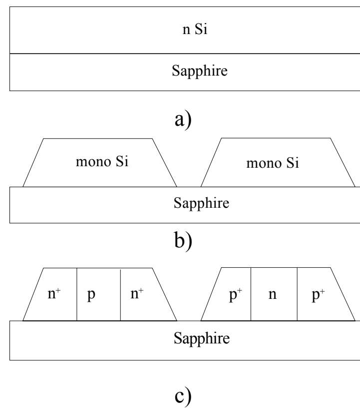

Fig. 4. SOS technology: a – epitaxial of silicon; b – creation of separated regions of silicon; c – formation of NMOP and PMOP transistors

MOS transistor is characterized by the output characteristic ($I_D(U_{DS})$). It is connected by common-source scheme. The inversion layer charge density varies in the channel between the source and the drain from 0 to L, channel voltage varies from 0 to U_{DS}:

$$\int_0^L I_D dy = -\mu C_{ox} B \int_0^{V_{SI}} (U_{GS} - U_{DS} - U_C - U_T) dU_C, \quad (1)$$

$$I_D = -\mu C_{ox} \frac{B}{L}((U_{GS} - U_T)U_{DS} - \frac{U_{DS}^{\ 2}}{2}), \ for \ \ U_{DS} < U_{GS} - U_T, \quad (2)$$

where μ – the mobility, cm^2/V; C_{ox} – capacitance per unit area, μF; B – gate width , nm; L – gate length , nm; U_{GS} – gate-source voltage, V; U_{DS} – drain-source voltage, V; U_C – inversion channel voltage, V; U_T – threshold voltage, V. Output current is directly proportional to channel length (formula (2)). It follows that decrease of channel length increases slope of transistor output characteristics, threshold voltage and drain current.

Etching process simulation

Etching process is simulated with ACES *(Anisotropic Crystalline Etch Simulation)* [6]. ACES is based on dynamic Cellular Automata (CA) model. It uses the static atom model and uses large number of atoms, which are interconnected in a lattice. Wet etching is applied.

For common etching process analysis we use test photo mask. Etching process is simulated in silicon depending on crystallographic planes orientation. The main task is to get configuration of structures shown in Fig. 3 and Fig. 4. Test photo mask is shown in Fig. 5.

Simulation is done when time is set to t = 0,6; 1,2; 3; 4,2; 5,4; 6 s, crystallographic planes orientation are(Fig. 6):

a) Surface crystallographic planes orientation – (100), edges – (100);

b) Surface crystallographic planes orientation – (100), edges – (110);

c) Surface crystallographic planes orientation – (110), edges – (110);

d) Surface crystallographic planes orientation – (111), edges – (110).

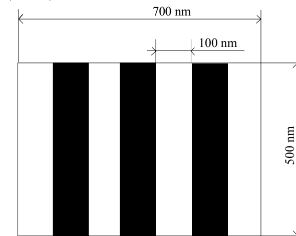

Fig. 5. Test photo mask is used for etching process simulation

Result is shown in Fig. 7, when surface and edges crystallographic planes orientation – (100), in Fig. 9 – (110), edges (110). Measurement changes of "active" regions depending on etching time and crystallographic planes orientation are shown in Fig. 8 and Fig.10.

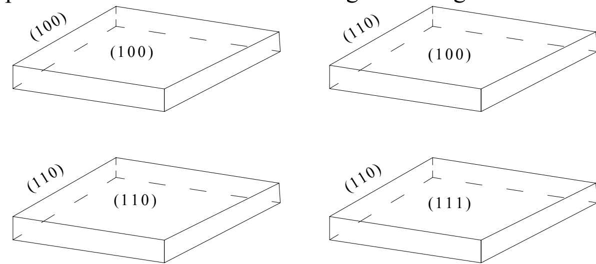

Fig. 6. Silicon crystal lattice orientation used for etching process simulation

Etching rate depends on crystallographic planes orientation. The highest etching rate is reached in

substance with crystallographic planes orientation (110), 23 nm/s. The biggest lateral etching belongs to substance with crystallographic planes orientation (100), 17 nm/s on both sides together (Fig. 7–8).

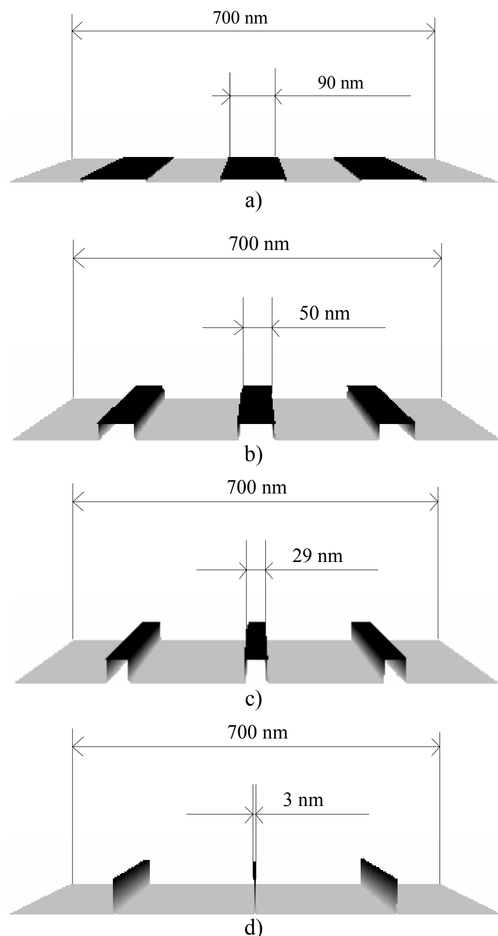

Fig. 7. Si etching process simulation, when surface crystallographic planes orientation – (100), edges – (100): a – t=0,6 s; b – t=3 s; c – t=4,2 s; d – t=6 s

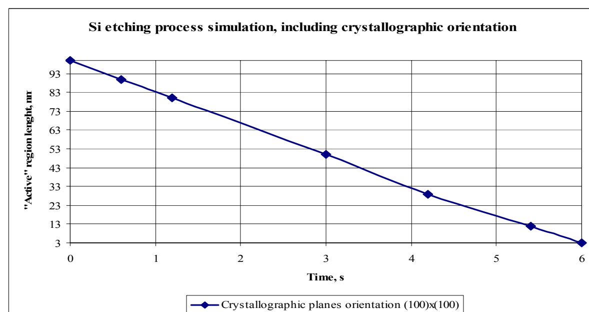

Fig. 8. Si etching process simulation – "active" region dependence on etching time including crystallographic planes orientation

"V" form grooves could be formed; therefore the length of "active" region, designed for MOS transistor, becomes short. In this way MOS parameters are influenced.

Si with crystallographic planes orientation (110) has the lower lateral encroachment, 1 nm/s on both sides together (Fig. 9–10). The hole is formed with pitched side wall (Fig. 9), contrarily with Fig. 7, where side wall is vertical etched. Holes with pitched side walls worsen element isolation parameters.

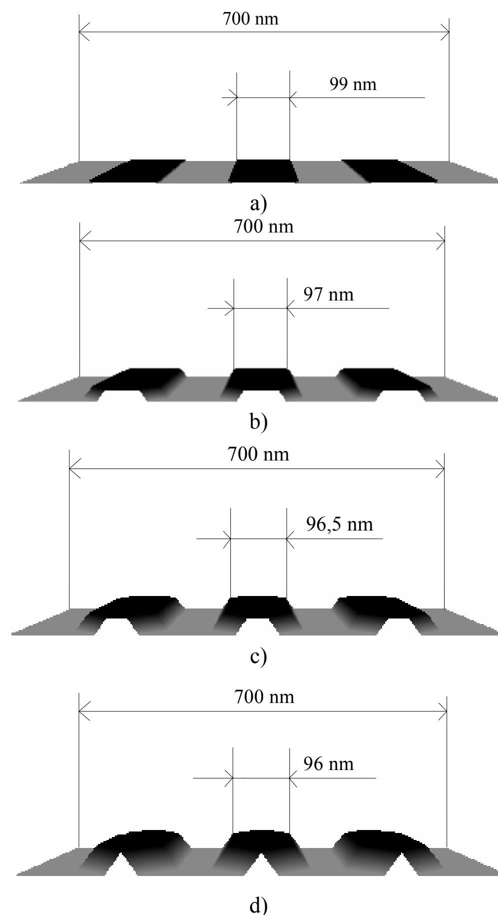

Fig. 9. Si etching process simulation, when surface crystallographic planes orientation – (110), edges – (110): a – t=0,6 s; b – t=3 s; c – t=4,2 s; d – t=6 s

There are 8 planes in substances with crystallographic planes orientation (111), which suspend etching process; therefore the etching result (curve) is not given. Simulation was performed with silicon surface crystallographic planes orientation – (111), edges – (110). Simulation result is shown on Fig.11, etching process proceeded only where crystallographic planes orientation (110).

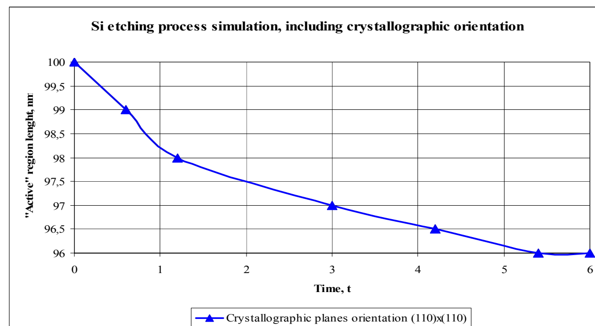

Fig. 10. Si etching process simulation – "active" region dependence on etching time including crystallographic plane orientation

For example, if hole must be formed with depth ~50 nm, we can use Si with crystallographic planes orientation (100) and process will take about 2 s time. The lateral encroachment rate of 17 nm/s and from result which we have got we make conclusion, that the length of the "active" region of photo mask must be 134 nm, otherwise it is possible to use Si ((110)x(110)) according to condition, that hole is formed with pitched side walls.

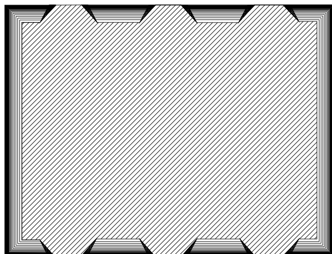

Fig. 11. Si etching process simulation, when surface crystallographic planes orientation – (111), edges – (110)

Conclusions

1. It is recommended to use wafers with crystallographic planes orientation (110) in semiconductor manufacturing using LOCOS and SOS technologies. In this way the lower lateral encroachment is reached only 1 nm/s on both sides together, when crystallographic planes orientation (100) lateral etching rate is 17 times greater (17nm/s);
2. Before wafers are chosen, lateral encroachment must be computed for IC fabrication;
3. The highest lateral etching is reached in silicon with crystallographic planes orientation (100), 17 nm/s on both sides together;
4. Si with crystallographic planes orientation (100) can be used for MOS formation, if "active" region of photo mask will be 134 nm;
5. Silicon wafers with crystallographic planes orientation (110) used for MOS formation with unchanged "active" region.

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Problems of etching process, related with MOS transistors separation in LOCOS and SOS technologies were researched. Wafer of Si selection depending on crystallographic planes orientation is the main task. The etching rate along direct direction and lateral encroachment depends on crystallographic planes orientation. Wet etching is simulated with program ACES. Test photo mask with 100 nm holes for wafer etching is used for etching process simulation. The highest etching rate reached in Si with crystallographic planes orientation (110) – 23 nm/s. The biggest lateral etching belongs to substance with crystallographic planes orientation (100), 17 nm/s on both sides together in wet etching process. Ill. 11, bibl. 6 (in English; summaries in English, Russian and Lithuanian).

Д. Андрюкайтис, Р. Анилёнис. Моделирование процесса травления в нано МОП структурах // Электроника и электротехника. – Каунас: Технология, 2006. - № 5(69). – С. 9–12.

Исследованы проблемы, связанные с изолированием МОП транзисторов в LOCOS и КНС технологиях. В выше упомянутых технологиях важно выбрать кристаллографическую ориентацию подложек, так как это определяет скорость травления кремния в прямом и боковом направлениях. Моделирование "мокрого" травления проведено используя программу ACES. При моделировании применена тестовая фоторезистивная маска с промежутками 100 нм. Максимальная скорость "мокрого" травления в прямом направлении (23 нм/с) достигается для кремниевых подложек кристаллографической ориентацией (110). При моделировании установлено, что максимальное боковое подтравливание со скоростью 17 нм/с получается для подложек с ориентацией (100). Ил. 11, библ. 6 (на английском языке; рефераты на английском, русском и литовском яз.).

D. Andriukaitis, R. Anilionis. Nanomatmenų MOP struktūrų ėsdinimo proceso modeliavimas // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2006. – Nr. 5(69). – P. 9–12.

Išnagrinėtos ėsdinimo problemos, susijusios su MOP tranzistorių atskyrimu LOCOS ir SAS technologijose. Pagrindinis veiksnys – Si pagrindo parinkimas pagal kristalografinių plokštumų orientaciją, nes nuo to priklauso Si ėsdinimo greitis tiesiogine kryptimi ir šoninis paėsdinimas. „Šlapiojo“ ėsdinimo modeliavimas atliktas programa ACES. Ėsdinimo procesui modeliuoti naudota testinė foto kaukė su ėsdinimui paliktomis 100 nm skersmens angomis. Didžiausias „šlapiojo“ ėsdinimo greitis 23 nm/s tiesiogine kryptimi pasiektas Si, kurio kristalografinių plokštumų orientacija (110). „Šlapiojo“ ėsdinimo proceso modeliavimo metu nustatyta, kad didžiausias šoninis paėsdinimas 17 nm/s gautas Si, kurio kristalografinių plokštumų orientacija (100). Il. 11, bibl. 6 (anglų kalba; santraukos anglų, rusų ir lietuvių k.).

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