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Calculation of Interpolation Parameters in the Comparator Analog Information Converters

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Introduction

One of the structures of comparator converters is analog–to–digital converters (ADC) with the signal interpolation at the input [1, 2]. When the applying the signal interpolation method the number of elements of the converter decreases and the lacking information is restored using the information of the remaining elements in outputs [3 – 5]. According to the way of the lacking information restoration, the interpolation can be passive and active. In the case of active interpolation the information in the strobing comparator input is restored using output signals of two consecutive pre–amplifiers. Then the number of amplifiers decreases twice. Using the passive interpolation, the lacking information is restored applying the divider of the interpolation resistors, which is switched in the outputs of pre–amplifiers. The passive interpolation allows reducing a larger number of amplifiers in the input than the active one. The application of folding and interpolating circuits decreases the requirements for the conversion accuracy because the ADC quantization step increases. The power consumption and the equivalent capacitance of the input also decrease. But the introduction of the inert circuit of interpolating resistors can reduce the speed of the analog information conversion when the interpolation level is chosen inadequately.

In this work dependences of the interpolation parameters on the number of bits of the converter, the band width of the analog signal frequencies and on the folding coefficient are considered. The analytic equations are derived and the modeling results are presented.

Calculation of the interpolation coefficient

A diagram of the parallel ADC with the folding amplifiers FA_1, FA_2 ... FA_k,, matrix of the interpolating resistors R_{11}, R_{12}, ..., R_{1k}; R_{21}, R_{22}, ..., R_{2k}, the strobing comparators C_1, C_2, C_3, ..., C_k and the decoding unit is presented in Fig. 1.

The interpolation level is called the interpolating coefficient K, which depends on the decrease of the number of amplifiers in the inputs of strobing comparators. This coefficient K is determined from these requirements.

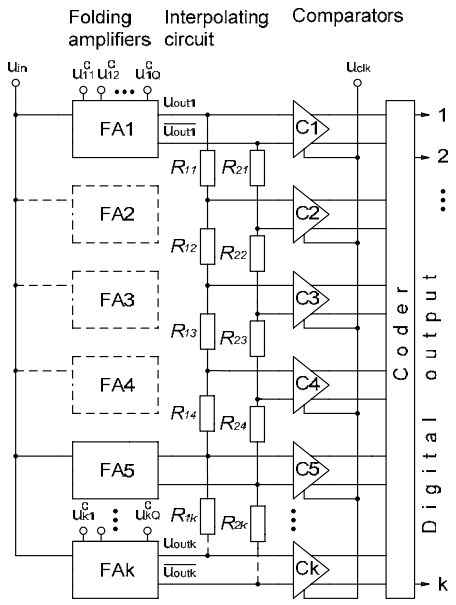

Fig. 1. Fragment of interpolating ADC: F_{A1}–F_{Ak} – differential (folding) amplifiers, C_1–C_k – strobing comparators, R_{11}...R_{2k} – circuit of interpolating resistors.

The first requirement is that the voltage difference Δu between remaining consequitive amplifiers should not exceed the limits of the transfer characteristic linear part of the differential amplifier, i.e.

$$\Delta u = u_{out(i+k)} - u_{outi} \le u_{lin}\,, \tag{1}$$

or

$$u_{lin} \ge K \cdot h_l\,, \tag{2}$$

where K is the number of unused amplifiers or the interpolation coefficient; h_l is the value of the lowest bit or the quantum size.

As for the N–bit parallel ADC

$$h_l = \frac{u_{in}}{2^N - 1}, \quad (3)$$

thus from equations (2) and (3) we obtain

$$K < \frac{u_{lin}(2^N - 1)}{u_{in}}. \quad (4)$$

The quantum size, when the signal transformation is used in the ADC input applying the folding circuit, is:

$$h_s = h_l \cdot Q; \quad (5)$$

where Q is the convolution coefficient [1].

The quantum size of the converter with the folding and interpolating circuits is:

$$h_{s-1} = \frac{h_s}{K}. \quad (6)$$

After evaluation of the transfer coefficient A_s of the folding amplifier, from equations (5) and (6) we obtain that

$$h_{s-i} = \frac{h_l \cdot Q}{K} = \frac{u_{in} Q A_S}{(2^N - 1)K}. \quad (7)$$

Equation (7) can be written as follows:

$$h_{sl} = \gamma \cdot h, \quad (8)$$

where $\gamma = \frac{Q \cdot A_S}{K}$ is the analog signal transformation coefficient. (9)

The second requirement is that the allowable aperture uncertainty time duration Δt_a must be longer than the interpolating circuit constant τ_I, i.e.

$$\Delta t_a \geq \tau_I. \quad (10)$$

The number of resistors in the interpolating circuit is determined by the number of unused amplifiers, which is evaluated by the interpolating coefficient K. The maximal time constant of the interpolating circuit formed of the resistor matrix $R_{1k} - R_{2k}$ can be calculated by an equation:

$$\tau_{I\max} \cong 0{,}5 R_{inekv} C_{ekv} K^2, \quad (11)$$

where R_{inekv} is the equivalent resistance of the resistor matrix circuit of the interpolating divider, which evaluates equivalent resistances of resistor R_i chains and metallization paths combining them; K – quantity of chains.

C_{ekv} is the equivalent capacitance of one RC chain is:

$$C_{ekv} = C_{KIn} + C_M + C_R, \quad (12)$$

C_{KIn} is the capacitance of the comparator input; C_M is the capacitance of the metallization path; C_R is the equivalent capacitance of the integrated interpolating resistor.

The maximal time constant τ_I of the interpolating circuit of the comparator most distant from two boundary folding amplifiers will be two times lower, i.e.

$$\tau_I \approx \frac{\tau_{I\max}}{2} = 0{,}25 R_{inekv} C_{ekv} K^2. \quad (13)$$

The aperture uncertainty time duration allowable for the converter for the sine form f frequency analog signal is expressed by equation:

$$\Delta t_a \leq \frac{h_{s-i}}{u_{in} 2\pi f}. \quad (14)$$

By inserting (7) into (14) for the folding – interpolating converter we obtain:

$$\Delta t_{s-i,a} \leq \frac{Q A_S}{2\pi f K (2^N - 1)}. \quad (15)$$

By inserting (9) into (15), the expression can be written as:

$$\Delta t_{s-i,a} \leq \frac{2\gamma}{2\pi f (2^N - 1)}. \quad (16)$$

From (10), (11) and (16) after some rearrangements we obtain such expression of the interpolation coefficient:

$$K_I = \sqrt[3]{\frac{4 Q A_S}{\pi f_{\max} (2^N - 1) \tau_{inekv}}}, \quad (17)$$

where: f_{max} is the maximum frequency of the analog signal spectrum;

$$\tau_{inekv} = R_{inekv} \cdot C_{ekv}. \quad (18)$$

Calculation of interpolation errors

The signal interpolation is possible in the linear part of transfer characteristics of the folding differential amplifiers [1].

We will consider the interpolation error due to nonlinearity of folding characteristics.

Output currents of the differential amplifier are expressed by known equations:

$$I_{a1} = \frac{I_0}{1 + \exp\left(-\frac{u_i - u_{0s}}{\varphi_T}\right)}, \quad (19)$$

$$I_{a2} = \frac{I_0}{1 + \exp\left(\frac{u_i - u_{0s}}{\varphi_T}\right)}, \quad (20)$$

where I_0 is the current of the source; $u_i = u_s - u_{i\,atr}$; u_{0s} is the offset voltage of the transistor pair; $\varphi_T = kT/q$.

Output voltage deviations of folding amplifiers due to nonidentity of parameters of differential transistor pairs can be expressed by an equation:

$$\Delta u = \frac{I_0 R_c}{2}\left[\frac{1}{1 + \exp\left(\frac{u_i - u_{0s1}}{\varphi_T}\right)} - \frac{1}{1 + \exp\left(-\frac{u_i - u_{0s2}}{\varphi_T}\right)}\right]. \quad (21)$$

The deviations of current due to the offset voltage deviation in boundary folding differential amplifiers A_1 and A_5 are written by equations:

$$\Delta I_{A1} = \frac{I_0}{2} th\left(\frac{\Delta u_{0sA1}}{2\varphi_T} \right), \quad (22)$$

$$\Delta I_{A5} = \frac{I_0}{2} th\left(\frac{\Delta u_{0sA5}}{2\varphi_T} \right). \quad (23)$$

The maximal deviation of output currents at „zero“ points for the boundary folding amplifiers is

$$\Delta I_{A1-A5} = \frac{I_0}{2}\left[th\left(\frac{\Delta u_{0sA1}}{2\varphi_T} \right) + th\left(\frac{\Delta u_{0sA5}}{2\varphi_T} \right) \right]. \quad (24)$$

The largest interpolation error according to the current ΔI_I will be due to the current deviations of the boundary folding amplifiers. This error will also depend on the folding and interpolating coefficients Q and K.

From equations (21), (22), (23) and (24) after evaluation of Q and K and after some rearrangements we can write the following equation:

$$\Delta I_L = \frac{I_0}{2}\left\{ \left[1 - th\left(\frac{K\Delta u_{ref\,A1}}{Q2\varphi_T} \right) \right] - \left[1 - th\left(\frac{K\Delta u_{ref\,A5}}{Q2\varphi_T} \right) \right] \right\}. \quad (25)$$

The interpolation current error ΔI_{0L} due to initial current deviations of differential amplifiers can be determined by an equation:

$$\Delta I_{0L} = -\left[1 - th\left(\frac{(Q-K)\cdot \Delta u_{ref}}{Q2\varphi_T} \right) \right]. \quad (26)$$

Due current deviations (24), (25) and (26) the total maximal interpolation error is as follows:

$$\Delta u_L = \frac{I_0 R_c}{2}\left\{ \left[th\left(\frac{\Delta u_{0\,A1}}{2\varphi_T} \right) + th\left(\frac{\Delta u_{0s}}{2\varphi_T} \right) \right] + \left[1 - th\left(\frac{K\Delta u_{ref\,A1}}{Q2\varphi_T} \right) \right] \right\} -$$

$$- \frac{I_0 R_c}{2}\left\{ \left[1 - th\left(\frac{K\Delta u_{ref\,A5}}{Q2\varphi_T} \right) \right] - \left[1 - th\left(\frac{(Q-K)\Delta u_{ref}}{Q2\varphi_T} \right) \right] \right\}. \quad (27)$$

The relative interpolation error from equation (27) can be written by an equation:

$$\delta_L = 0{,}5\left[th\left(\frac{\Delta u_{0s\,A1}}{2\varphi_T} \right) + th\left(\frac{\Delta u_{0s\,A5}}{2\varphi_T} \right) - th\left(\frac{K\Delta u_{ref\,A1}}{Q2\varphi_T} \right) \right] +$$

$$+ 0{,}5\left[th\left(\frac{K\Delta u_{ref\,A5}}{Q2\varphi_T} \right) + th\left(\frac{(Q-K)\cdot \Delta u_{ref}}{Q2\varphi_T} \right) - 1 \right]. \quad (28)$$

Assuming that voltage deviations in equation (28) differ little and the interpolation error depends on nonlinearity of transfer characteristics of folding differential amplifiers, the interpolation error equation (28) can be expressed by a simplified equation:

$$\delta_I \approx 1 - th\left(\frac{\Delta u_{lin}}{2\varphi_T} \right) + th\left(\frac{K\Delta u_{lin}}{Q\varphi_T} \right) -$$

$$- 0{,}5th\left(\frac{(Q-K)\Delta u_{lin}}{Q2\varphi_T} \right), \quad (29)$$

where Δu_{lin} is the linear part of the transfer characteristic of the folding amplifier, δ_I – error in LSB.

Modeling results

Modeling results of frequency characteristics of the ADC with folding and interpolating circuits are presented in Fig. 2.

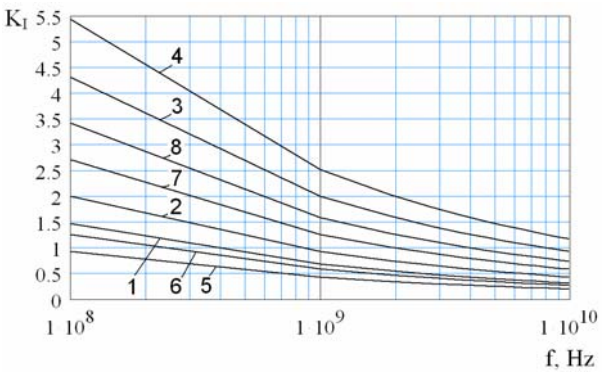

Fig. 2. Dependence of the interpolation coefficient K_I on the maximal frequency of the analog input signal spectrum. Calculation was made for: A_s = 2V; Q = 8. curve 1 – N = 8, τ = 250 ps; curve 2 – N = 8, τ = 100 ps; curve 3 – N = 8, τ = 10 ps; curve 4 – N = 8, τ = 5 ps; curve 5 – N = 10, τ = 250 ps; curve 6 – N = 10, τ = 100 ps; curve 7 – N = 10, τ = 10 ps; curve 8 – N = 10, τ = 5 ps.

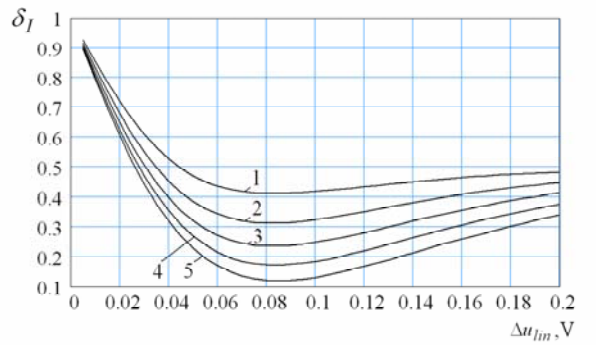

Fig. 3. Dependence of the interpolation error δ_I on the linear part Δu_{lin} length of the transfer characteristic of differential amplifiers with K = 3, and folding coefficients Q = 6 (curve 1), 7 (curve 2), 8 (curve 3), 9 (curve 4), 10 (curve 5).

We can see that the speed f_{max} of the interpolating ADC with the folding amplifiers depends on the inertness τ of the interpolating resistor divider circuit and the number N of converter bits. For example, the interpolation coefficient of one GHz ADC is K = 3, when N = 8 , Q = 8 and τ = 250 ps. In order to increase the number of converter bits at the same K, τ must be reduced. A higher

interpolation level can be achieved by reducing the converter speed.

Modeling results of interpolation errors are shown in Fig. 3. The error δ_I depends on the folding and interpolation coefficients. The lowest interpolation error (0.2–0.5 LSB) can be achieved by selecting a certain linear part length of transfer characteristics of folding amplifiers. When $\delta_I < 50$ mV, the error increases very fast.

Conclusions

1. Theoretical analysis of interpolation parameters evaluating the influence of folding circuits on the ADC speed and accuracy was made. Equations for the interpolation coefficient calculation with predetermined main parameters of the converter, the signal spectrum, the number of bits and the interpolation circuit inertness, were derived.
2. Equations for the interpolation error evaluation, depending on nonlinearity of transfer characteristics of the differential amplifiers, the folding and interpolation level, were derived.
3. Modeling characteristics of parameter dependence of folding and interpolating circuits are presented.

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The theoretical analysis of interpolation parameters evaluating the influence of folding circuits on the ADC speed and accuracy is made in the paper. The analytical equations are derived and dependences of interpolation parameters on the number of converter bits, the analog signal frequency band width, and the folding coefficient are considered. Equations of for the interpolation error evaluation, depending on the nonlinearity of transfer characteristics of differential amplifiers, folding and interpolation level, were derived. It has been determined that the speed of the interpolating ADC with folding amplifiers strongly depends on the inertness of the interpolating resistor divider circuit and the number of the converter bits. In order to increase the number of the converter bits with the same interpolation coefficient, the circuit inertness must be reduced. A higher interpolation level can be achieved by reducing the speed of the converter. The interpolation error depends on the folding and interpolation coefficients. The lowest interpolation error (0.2 – 0.5 LSB) can be achieved by selecting a certain linear part length of transfer characteristic of folding differential amplifiers. Ill. 3, bibl. 5 (in English; summaries in English, Russian and Lithuanian).

А. Марцинкявичюс, В. Ясонис. Расчёт параметров интерполяции компараторных АЦП // Электроника и электротехника. – Каунас: Технология, 2006. – №. 5(69). – С. 5–8.

Представлен теоретический анализ интерполяционных параметров свёрточных компараторных АЦП. Выводятся аналогические уравнения и исследуются зависимости интерполяционных параметров от разрядности, степени свёртки и максимальной частоты спектра входного аналогового сигнала. Получено уравнение для расчета погрешности интерполяции, в которой учитываются нелинейность передаточных характеристик дифференциальных усилителей и степень свёртки и интерполяции сигнала. Установлено, что быстродействие АЦП с интерполяцией на выходе сильно зависит от инерционности цепей интерполяции и разрядности. Для увеличения степени интерполяции необходимо уменьшать быстродействие АЦП. Погрешность интерполяции зависит от линейности характеристик и параметров цепей свёртки и интерполяции. Минимальная погрешность (0,2 – 0,5 МЗР) получается выбором ширины линейного участия передаточных характеристик свёрточных дифференциальных усилителей. Ил. 3, библ. 5 (на английском языке; рефераты на английском, русском и литовском яз.).

A. Marcinkevičius, V. Jasonis. Komparatorinių analoginės informacijos keitiklių interpoliacijos parametrų skaičiavimas // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2006. – Nr. 5(69). – P. 5–8.

Atlikta teorinė interpoliacijos parametrų analizė, įvertinanti sąsūkos grandinių įtaką ASK spartai ir tikslumui. Sudaromos analitinės lygtys ir nagrinėjamos interpoliacijos parametrų priklausomybės nuo keitiklio skilčių skaičiaus, analoginio signalo dažnių juostos pločio, ir sąsūkos koeficiento. Sudarytos lygtys interpoliacijos paklaidai įvertinti priklausomai nuo diferencinių stiprintuvų perdavimo charakteristikų netiesiškumo, sąsūkos ir interpoliacijos laipsnio. Nustatyta, kad interpoliacinio ASK su sąsūkos stiprintuvais sparta labai priklauso nuo interpoliacinių rezistorių daliklio grandinės inertiškumo ir keitiklio skilčių skaičiaus. Norint padidinti keitiklio skilčių skaičių, reikia mažinti grandies inertiškumą. Didesnį interpoliacijos laipsnį galima pasiekti mažinant keitiklio spartą. Interpoliacijos paklaida priklauso nuo sąsūkos ir interpoliacijos koeficientų. Mažiausią interpoliacijos paklaidą (0,2 – 0,5 LSB) galima pasiekti parinkus tam tikrą sąsūkos diferencinių stiprintuvų perdavimo charakteristikų tiesinės dalies atkarpos ilgį. Il. 3, bibl. 5 (anglų kalba; santraukos anglų, rusų ir lietuvių k.).