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A Transistor-Level Reconfigurable Circuit for Rapid Transconductor Design and Testing

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Introduction

Today's telecommunication and IT industry is mostly predominated by digital signal processing. There are however numerous applications which, by their nature, require analog processing. One of the most common applications specific for the analog domain is interfacing a digital processing unit with the "outside world". Information coming from a targeted environment is recorded with specific sensors, which by definition provide analog output signals. The resulting signal is then filtered and amplified before the analog-to-digital conversion takes place.

Another common analog processing application is the channel select filter in radio communication chipsets [1]. Although modern Software Defined Radio (SDR) and Cognitive Radio (CR) systems try to bring the ADC as close as possible to the antenna, there are technologically limiting factors which make digital signal processing in low-IF bands impractical, e.g. ADC sampling frequency, microcontroller/processor clock frequency, etc.

Bio-medical implantable electronics is another example which targets analog circuits. For example, recent trends in auditory prosthesis try to have the whole signal processing chain performed in an analog fashion [2, 3], due to its potential with respect to low power consumption and high processing speed.

Thus, the importance of the analog part in a mixed-signal system-on-a-chip (SoC) is obvious, although it only takes up a small percentage of the die area.

In the applications enumerated above, one central element is the analog filter. Implementation techniques for analog continuous-time filters are OpAMP-RC, MOSFET-RC and Gm-C [4].

OpAMP-RC and MOSFET-RC filters are operational amplifier (OpAMP) based circuits. They are usually limited to low-frequency applications because the open-loop gain of the active element is sufficiently high only at low frequencies [5]. Also, the passive component values increase with frequency, making integration more demanding in terms of area.

Transconductance-C (Gm-C) filters are a good alternative for intermediate frequency (IF) continuous-time filtering. The active element in Gm-C filters is the transconductor, or the operational transconductance amplifier (OTA). Transconductors are structurally built for high-frequency operation, namely a differential transistor pair with no additional internal nodes [5]. Among other advantages of the Gm-C filters is the possibility for electronic tuning [4]. Transconductors however have a weak performance with respect to linearity and distortion and therefore need additional circuitry for linearization.

Transconductor design specifications are given in terms of transconductance (Gm), bandwidth (BW), linearity – measured by total harmonic distortion (THD), dynamic range (DR) and power consumption (P). Although some design specs are correlated, e.g. higher linearity comes with a higher dynamic range, the design specifications are however conflicting. Transconductor linearity affects the transconductance and in some cases the power consumption, provided that additional bias current is needed.

Many linearization techniques have been proposed in literature. A review of linearization techniques can be found in [5, 6]. However, it is up to the experienced designer to choose a topology best suited to the satisfaction of a given set of design specifications.

To aid the task of circuit design and testing, solutions

for verification and rapid prototyping have been proposed. As an example, Stoica et. al. proposes a field programmable transistor array (FPTA) used for electronic circuit development at transistor level [7]. At a higher abstraction level, Becker proposes a field programmable analog array (FPAA) which allows reconfiguration at transconductor level [8]. Both examples exhibit a high granularity at the abstraction level they were designed for. However, it is often useful to eliminate certain degrees of freedom in favor of increased implemented circuit performance. For example, the FPAAs proposed in [1] used in multi-standard mobile terminals, have limited the implementable topologies to filtering applications in wireless communications.

In this article we propose a reconfigurable circuit to be used as a platform for the study, conception and testing of various transconductor linearization techniques. The proposed circuit has the ability to implement basic linearization techniques reported in literature, i.e. non-linear term cancelation and source degeneration, as well as combinations of these methods. Thus, given a set of design specifications, a high range of topologies can be implemented and tested, making it a powerful medium in integrated circuit development. In this respect, the proposed programmable analog array (PAA) exhibits a high level of generality for transconductor implementation. Compared to Stoica's FPTA however, certain degrees of freedom have been blocked.

This article is organized as follows. Section 2 presents a brief review of the basic linearization techniques reported in literature. The transistor-level reconfigurable circuit built around the basic linearization techniques is proposed in section 3. Simulation results are finally shown in section 4.

Transconductor linearization techniques

In this section, a brief overview of the basic linearization techniques is presented. Consider the transconductor from Fig. 1 implemented with a simple differential pair. No linearization is applied yet. The transconductance value is then equal to the transconductance of the input transistors

$$G_m = g_m = \frac{I_{bias}}{V_{od}}. \quad (1)$$

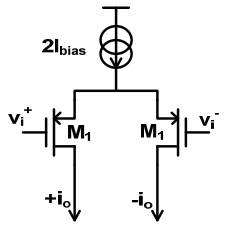

Fig. 1. The simple differential pair as transconductor

Further on, let the non-linearity of the transconductor be defined by the third harmonic distortion, HD3. With linearization, the target is to reduce HD3, as it has the greatest impact on the THD [5]. In the current work we target two main classes of linearization techniques: non-linear term cancellation and feedback.

Practical implementations of non-linear term cancellation translate to the interconnection of several transconductor stages [5]. A solution for the cancellation of second-order harmonics is shown in Fig. 2(a) [5, 6], and is implemented with the analog multiplier structure [9].

An alternative structure for non-linear term cancellation is the parallel transconductor deployment, as shown in [5], Fig. 2(b).

Non-linear term cancellation basically relies on signal multiplication and summation. Thus, the linearized transconductor design equation reduces to bias current and threshold voltage ratios [5], as stated in Table 1. The actual ratio values are subject to optimization.

Our tests reveal that, although an improvement in linearity is achieved, non-linear term cancellation does not perform well if employed alone. Yet, it leads to improved results if used in conjunction with other linearization techniques.

From the class of transconductor linearization via feedback, the main representative is source degeneration [6]. Resistive source degeneration, Fig. 3(a), consists of interconnecting the input transistor sources with a passive resistor Rs.

The transconductor linearity is dramatically improved by a factor n^2 [5, 6], where

$$n = 1 + g_m \cdot R_s . \quad (2)$$

Then, the trasconductance expression also changes, as shown in (3) [2], which approximates a decrease by factor n.

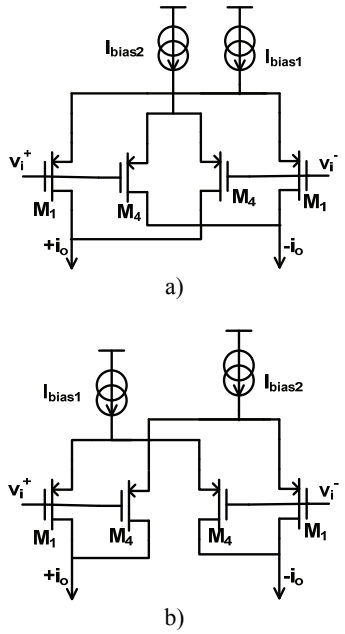

Fig. 2. Implementations of the non-linear term cancellation: (a) distortion cancellation [5, 6] and (b) parallel differential pairs [5]

$$G_m = \frac{g_m}{1 + g_m \cdot R_s}. \quad (3)$$

Equation (3) shows that there are two degrees of freedom to set the same performance parameter. However, provided the degeneration resistance is sufficiently high, the linearized transconductance can be approximated by:

$$G_m \approx \frac{1}{R_s}, \text{ if } R_s >> \frac{1}{g_m}. \quad (4)$$

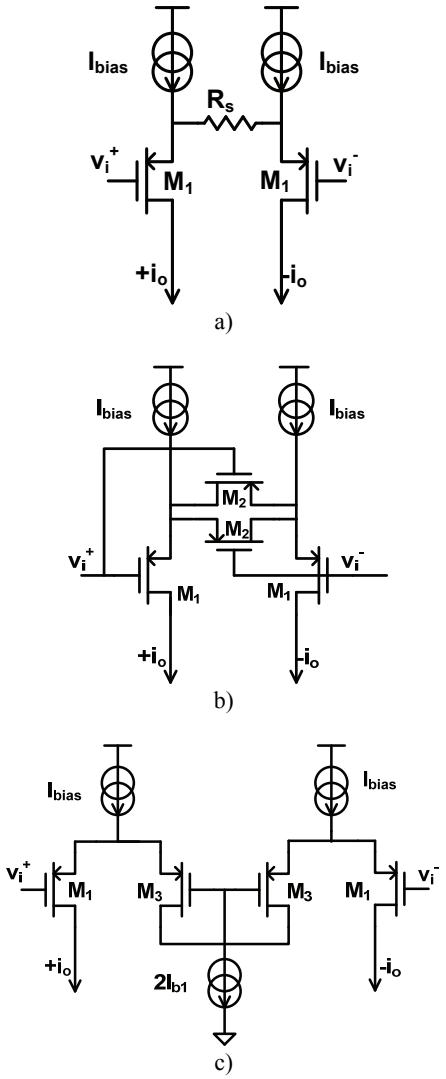

Fig. 3. Implementations of source degeneration with (a) passive resistance [5, 6], (b) triode transistors [10] and (c) saturated transistors [11]

Due to the considerably high resistance value, resistive source degeneration is not an integration friendly solution for silicon. Therefore, implementations of the degeneration resistor with MOS transistors have been proposed. Krummenacher and Joehl [10] proposed the use of transistors in the linear region, as shown in Fig. 3(b).

The use of transistors in saturation to implement the degeneration resistance has been proposed by Torrace et. al. [11], as shown in Fig. 3(c). Compared to [10], this solution needs an additional current source, namely 2Ib1, and consequently leads to increased power consumption for the same linearity. The benefit of this solution however is that it allows tunability via the additional current source, without changing the input transistors bias point, as is the case in [2].

The main design parameter for source degenerated transconductors is the linearization factor *n* defined in eq. (2). For MOS implementations, the linearization factor can again be defined by ratios, as shown in Table 1.

The basic lienarization techniques with the corresponding design equations and design parameters, i.e. degrees of freedom, are listed in Table 1 [5, 6]

It is shown in [12] that the basic techniques from Table 1 can be combined to achieve even better performance in terms of linearity, at the price of increased circuit complexity.

The reconfigurable Gm core

A collection of basic transconductor linearization techniques was presented in section 2, together with the corresponding performance measures. Literature shows that even better performance can be achieved, however with the price of increased circuit complexity. As a rule of thumb, higher linearity and dynamic range are achieved with the price of a smaller transconductance and in certain cases higher power consumption. Transconductor design is usually a matter of compromise in the satisfaction degree of various design specifications. It is then up to the circuit designer to chose, design and optimize the circuit topology which bests suits a particular application. This task is very difficult and involves designer experience.

The ultimate goal of electronic circuit design is to achieve the best possible performance with minimum costs in terms of circuit complexity and designer effort. This is however difficult in the presence of conflicting design specifications, which is common in the analog domain.

Table 1. Summary of the basic linearization technique design equations and performance measures

Fig.	Design Parameter	Design Equations	THD	Gm
2(a) [5, 6]	$\alpha = \frac{I_{bias2}}{I_{bias1}}$ $v = \frac{V_{od1}}{V_{od4}}$	$v = \alpha^{-\frac{1}{3}}$	HD3= 0	$g_m \cdot (1-\alpha^{\frac{2}{3}})$
2(b) [5]	$\alpha = \frac{I_{bias2}}{I_{bias1}}$ $v = \frac{V_{od1}}{V_{od4}}$	$\alpha \cdot v^2 = 5$	↑	↓
3(a) [5, 6]	R_s	$n = 1 + g_m \cdot R_s$	$\frac{HD_3}{n^2}$	$G_m \approx \frac{1}{R_s}$
3(b) [10]	$\beta_1 = \frac{\mu C_{ox}}{2} \cdot \left(\frac{W}{L}\right)_1$ $\beta_2 = \frac{\mu C_{ox}}{2} \cdot \left(\frac{W}{L}\right)_2$	$n = 1 + \frac{\beta_1}{4\beta_2}$	$\frac{HD_3}{n^2}$	$G_m = \frac{g_m}{n}$
3(c) [11]	$g_{m1} = \frac{I_{bias}}{V_{od1}}$ $g_{m2} = \frac{I_{b1}}{V_{od2}}$	$n = 1 + \frac{g_{m1}}{g_{m2}}$	$\frac{HD_3}{n^2}$	$G_m = \frac{g_m}{n}$

In this paper we propose a reconfigurable transistor array, namely a reconfigurable transconductor core (Gm core), which should serve as a platform employed in circuit development and design activities. The reconfigurable Gm core is based on the basic linearization techniques listed in Table 1. Thus, the proposed circuit is built around four

transistor pairs M1-M4, corresponding to the input and linearization transistors form Fig. 2 and Fig. 3 respectively. The resulting circuit is illustrated in Fig. 4. To be noted is that transistor pair M2 was doubled so that it can be used in conjunction with parallel deployed differential pairs [12].

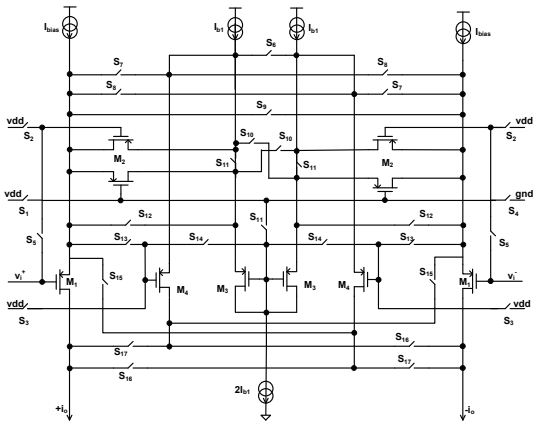

Fig. 4. The proposed reconfigurable transconductor core

PMOS switches S1-S3 implement the power-down circuits for the linearization transistors via connection to VDD. An exception is the diode-connected transistor pair M3 which achieves inherent power-down, provided that the stage is unbiased, $2I_{b1}=0$.

Switches S4-S17, implemented with digital transmission gates, are employed to interconnect targeted circuit nodes. The switch states to achieve the basic linearized topologies from Fig. 2 and Fig. 3 are listed in Table 2.

We have designed the reconfigurable Gm core to allow generality in the choice of a linearization topology. However, the allowable interconnections are limited in order to keep the downloaded/implemented circuits within some realistic ranges of complexity which pay off with respect to performance. Our configurable analog block (CAB) exhibits then a rather coarse granularity compared to the FPTA of Stoica et. al. [7].

The proposed reconfigurable Gm core is also provided with a programmability feature. The input transistors M1, linearization transistors M2-M4 and the current sources are implemented with arrays of parallel switched transistors.

Table 2. Switch states to implement the basic transconductor linearization techniques

Figure	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17
2(a) [5,6]	**on**	off	**on**	off	off	**on**	off	off	**on**	off	off	off	**on**	off	off	**on**	off
2(b) [5]	**on**	off	**on**	off	off	off	off	**on**	off	off	off	off	**on**	off	off	off	**on**
3(b) [10]	off	**on**	off	**on**	**on**	off	off	off	off	**on**	off	off	off	off	off	off	off
3(c) [11]	**on**	**on**	**on**	off	off	off	off	off	off	off	off	**on**	off	off	off	off	off

A generic switched transistor array of *m* parallel transistors is illustrated in Fig. 5, yielding an equivalent transistor aspect ratio equal to

$$\left(\frac{W}{L}\right)_{ech} = \sum_{k=0}^{m} a_k \cdot \frac{W}{L} \cdot 2^k \ . \qquad (5)$$

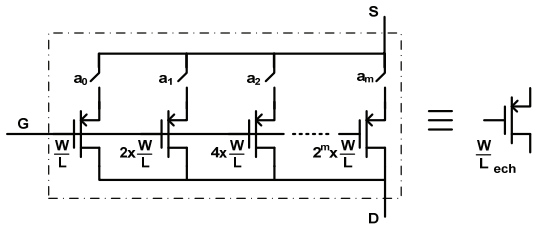

Fig. 5. Switched transistor array

With the switched transistor array shown in Fig. 5, the variation range of the transistor aspect ratios bias current values implemented for the reconfigurable circuit are listed in Table 3.

Table 3. Transistor aspect ratio and bias current variation range

	Step size	Variation range
M1 (W/L)	6.3µ/1µ	6.3µ/1µ → 25.2µ/1 µ
M2(W/L)	0.5µ/1µ	0.5µ/1µ →15.5µ/1µ
M3(W/L)	0.5µ/1µ	0.5µ/1µ →15.5µ/1µ
M4(W/L)	0.5µ/1µ	0.5µ/1µ →15.5µ/1µ
Ibias (A)	5µ	5µ → 50µ
Ib1 (A)	5µ	5µ → 50µ
2Ib1 (A)	1µ	1µ → 50µ

To be noted is that current sink 2Ib1 must be implemented with a smaller unity aspect ratio than the other transistors in order to provide a finer variation step for the generated bias current.

Simulation results

The proposed reconfigurable Gm core was implemented in Cadence using the AMS 0.35µm technology. The circuit was extensively simulated to prove its functionality and usefulness in testing various linearization topologies. For all examples presented in this section, the transconductor was designed to maximize linearity.

A first set of voltage-to-current (V-I) characteristics were simulated by configuring the CAB to successively implement the basic linearization techniques from Table 1.The simulation results are plotted in Fig. 6. The corresponding performance measures are then listed in Table 4.

Table 4 shows that the transconductance value is indeed decreased with linearity. The higher linearity was achieved for distortion cancellation, Fig. 2a, but for a very small dynamic range. The parallel differential stage topology exhibited the weakest performance. At this point, the circuits from Fig. 3 are the best compromise for Gm, THD and DR performance.

In the next scenario, combinations of the basic linearization techniques are subject to test. As an example,

the highly linear transconductor proposed in [12] was implemented. The CAB was set to simultaneously implement the solutions of Krummenacher and Joehl [10] and Torrace et al. [11] for source degeneration, together with distortion cancellation. The reconfigured Gm core is shown in Fig. 7. The simulated V-I transfer characteristic is plotted in Fig. 8 and the performance measures are listed in Table 5.

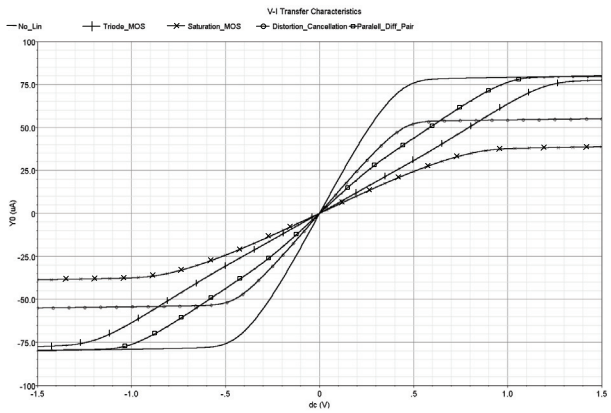

Fig. 6. The V-I transfer characteristics for the basic linearization techniques

Table 4. Performance measures for the basic linearization techniques

Figure	Gm [S]	THD [dB]	DR [V^{p-p}]	Power [W]
2(a) [5, 6]	115.5u	-56.9	1	1.015m
2(b) [5]	125.9u	-39.9	0.8	1.015m
3(b) [10]	64u	-44	2.2	948.5µ
3(c) [11]	48.3u	-45.3	1.4	949.1µ

Table 5. Performance measures for the transconductor linearized with combination of techniques from Section 2.

	Gm [S]	THD [dB]	DR [V^{p-p}]	Power [W]
Multiple linearization techniques [12]	53.5u	-54	2	1.05

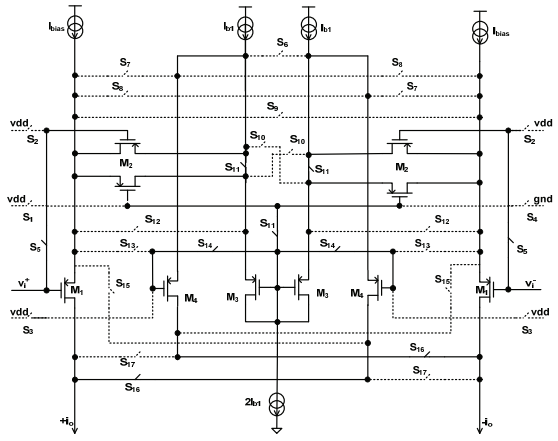

Fig. 7. Implementation of the linear transconductor from [12] on the proposed reconfigurable circuit

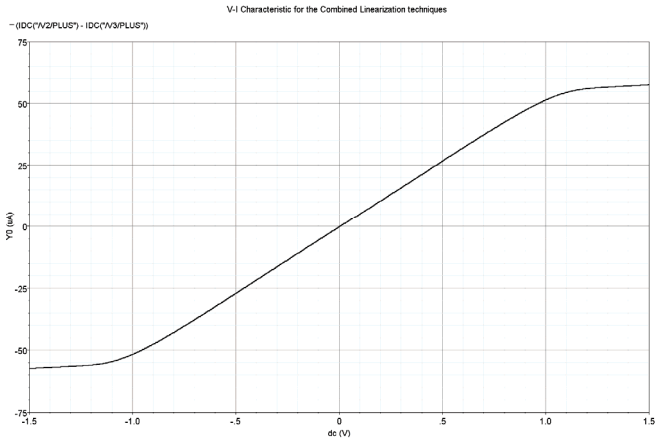

Fig. 8. The V-I transfer characteristics for the linear transconductor from [12], simulated with the proposed reconfigurable circuit

Conclusions

This article proposes a transistor-level reconfigurable circuit aimed to offer a platform for rapid conception, design and testing of linearized transconductor topologies. The reconfigurable circuit was built around the basic transconductor linearization techniques reported in literature. Transistor-level reconfigurability enables the simultaneous deployment of multiple linearization techniques. Thus, various topologies can be tested for the satisfaction of the multiple and often conflicting design specifications: transconductance, bandwidth, linearity, dynamic range and power consumption. On the other hand, switched transistor arrays enable programmability of the transistor aspect ratios and bias current values.

The reconfigurable transconductor was extensively simulated in a scenario that targeted the optimization of linearity. Simulation results prove the feasibility and usefulness of the proposed circuit in design and testing activities. Also, transistor level reconfigurability and programmability make the proposed circuit a good starting point for the development of auto-reconfigurable and auto-adaptive hardware.

Acknowledgements

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In modern mixed-signal systems-on-a-chip (SoC), a key role is played by the analog filter. For intermediate frequency (IF) bands, the filtering function is best performed with Gm-C structures. The active element of Gm-C circuits is the transconductor, the design of which is particularly difficult due to the multiple and conflicting design specifications. This article proposes a reconfigurable transconductor to aid the task of transconductor design. Transistor level reconfigurability enables rapid conception, design and testing of various transconductor topologies. Extensive simulation proves the feasibility and usefulness of the proposed reconfigurable circuit. Ill. 8, bibl. 12, tabl. 5 (in English; abstracts in English and Lithuanian).

P. Farago, L. Festila, S. Hintea, G. Csipkes, D. Csipkes, P. Soser. Tranzistorinė keičiamos konfigūracijos schema sparčiam transkonduktoriui projektuoti ir testuoti // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2012. – Nr. 1(117). – P. 99–104.

Šiuolaikinėse vienlustėse mišriųjų signalų sistemose pagrindinį vaidmenį vaidina analoginiai filtrai. Esant tarpinių dažnių juostai, filtravimo funkciją geriausiai atlieka Gm-C struktūros. Gm-C grandinių aktyvusis elementas yra transkonduktorius, kurį projektuoti ypač sunku dėl daugialypių ir konfliktuojančių projektavimo specifikacijų. Pasiūlytas keičiamos konfigūracijos transkonduktorius, padedantis spręsti projektavimo uždavinį. Tranzistorinis perkonfigūruojamumas leidžia greitai projektuoti ir testuoti įvairias transkonduktoriaus topologijas. Išplėstinė imitacija įrodo siūlomos keičiamos konfigūracijos schemos tinkamumą ir naudingumą. Il. 8, bibl. 12, lent. 5 (anglų kalba; santraukos anglų ir lietuvių k.).