

Operation Principles and Control Strategies of Cascaded H-bridge Multilevel Active Power Filter

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Introduction

In recent decades, electric power systems have suffered significant power quality problems caused by the proliferation of nonlinear loads, such as arc furnaces, lighting devices, adjustable ac drives, etc., which cause a large amount of characteristic harmonics, low power factor, and significantly deteriorates the power quality of the distribution systems [1-3]. The increasing restrictive regulations on power quality has significantly stimulated the development of power quality mitigation equipments, which are connected to the power system to improve the transmission capability and the quality of the voltage waveforms at the common coupling points (PCCs) for the customers. Among which the active power filters (APFs) are recognized as the most effective power quality compensating devices, adopted to recover balanced sinusoidal grid currents and enhance the voltage profiles [1].

For high-power medium-voltage APF applications, the classical two level or three-level converter topologies are insufficient due to the rating limitations imposed by the power semiconductors. Hence considerable attention has been focused on the multi-level inverter topologies, which significantly improve the output waveform spectrum of the inverter. Therefore, the bulky and expensive multi-pulse transformers can be avoided, resulting in reduced stress of the power semiconductor devices, substantially smaller filters and consequently, a cost reduction of the system [2].

With its modularity and flexibility, the cascaded H-bridge (CHB) multilevel inverter shows superiority among the multilevel converter topologies [3, 4]. A premium-quality output waveform with fast system response can be achieved by switching the power switches at relatively low switching frequency, while an equivalent high switching frequency can be obtained at the inverter output. However, the main disadvantage of the cascaded H-bridge converter is the voltage unbalance that could appear at the dc-link capacitors of the individual H-bridges [5]. In order to cope with this phenomenon, an adequate control strategy must

be employed to regulate the active power of each H-bridge, while the reactive power delivered by individual H-bridge must be equally distributed in order to ensure equal power sharing and heat dissipation of each H-bridge module.

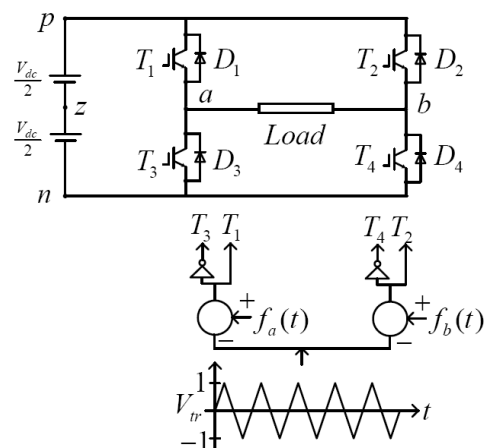


Fig.1. Schematic of single-phase H-bridge inverter

Operation principle of single-phase H-bridge inverter using three-level modulation

Fig.1 shows the schematic diagram of single-phase voltage source inverter, which consists of two single-phase legs connected to the common dc bus. The symbol 'p' and 'n' denote the positive and negative rail of the dc-link and 'z' denotes the fictitious ground. Each phase leg (indicated as 'a' and 'b') is modulated in a complementary manner by a carrier/reference waveform comparison circuit, which switches the phase leg to the upper DC rail when the reference waveform is greater than carrier, and to the lower DC rail when the reference waveform is lower than the carrier. The particular form of the carrier and reference waveforms depends on the PWM strategy that is implemented. As shown in Fig.1, the both legs 'a' and 'b' share a common carrier which is selected to be triangular. The two legs are modulated with 180 degree opposed reference waveforms, defined as:

$$\begin{cases} f_a(t) = V_{az}^* = \frac{V_{dc}}{2} M \cos(\omega_0 t); \\ f_b(t) = V_{bz}^* = \frac{V_{dc}}{2} M \cos(\omega_0 t - \pi), \end{cases} \quad (1)$$

where M represents modulation index ($0 < M < 1$) and ω_0 represents the angular frequency of the target output voltage. The line-to-line output reference voltage for the inverter is defined as:

$$V_{ab}^* = V_{az}^* - V_{bz}^* = V_{dc} M \cos(\omega_0 t). \quad (2)$$

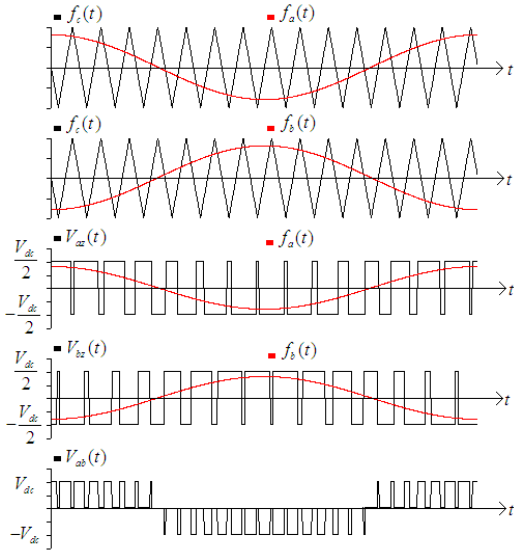


Fig. 2. Modulation signals, carriers and output waveforms of the single-phase H-bridge inverter

This arrangement achieves the three-level naturally sampled sine-triangular PWM, which shows significant harmonic advantages over most of the existing PWM schemes. The detailed waveforms regarding to this three-level PWM is shown in Fig.2. It can be seen how the each phase leg of the inverter switches between the upper and lower DC rails continuously over the fundamental cycle as the carrier waveform ramps above and below the reference waveform. The output voltage of a phase leg can be derived by using *double-edge naturally sampled PWM* technique, which is obtained as:

$$V_{az}^{pu} = \frac{V_{az}}{(V_{dc}/2)} = 1 + M \cos(\omega_0 t) + \frac{4}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{m} J_n \left(m \frac{\pi}{2} M \right) \sin[(m+n) \frac{\pi}{2}] \cos(m\omega_c t + n\omega_0 t) \quad (3)$$

and

$$V_{bz}^{pu} = \frac{V_{bz}}{(V_{dc}/2)} = 1 + M \cos(\omega_0 t - \pi) + \frac{4}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{m} J_n \left(m \frac{\pi}{2} M \right) \sin[(m+n) \frac{\pi}{2}] \times \cos[m\omega_c t + n(\omega_0 t - \pi)]. \quad (4)$$

Note that the output voltages are represented in per unit for the sake of brevity. Therefore, the output voltage harmonic components for the inverter can be derived as:

$$V_{ab}^{pu} = V_{az}^{pu} - V_{bz}^{pu} = 2M \cos(\omega_0 t) + \frac{8}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{2m} J_{2n-1}(m\pi M) \cos[(m+n-1)\pi] \times \cos[2m\omega_c t + (2n-1)\omega_0 t]. \quad (5)$$

Equation (5) shows that the odd carrier and associated sideband harmonics are completely cancelled from the output voltage, leaving only sideband harmonic $(2n-1)$ terms of the even $(2m)$ carrier groups.

A further harmonic cancellation can be obtained by appropriately phase shifting the remaining harmonics of several series-connected single-phase H-bridge modules. This modulation methodology, denoted as phase-shifted cascaded PWM (PSCPWM), is aiming to retain sinusoidal reference waveforms for two phase legs of each H-bridge inverter that are phase shifted by 180 degrees and then phase shift the carriers of each H-bridge to achieve additional harmonic sideband cancellation around the even carrier multiple groups.

Optimum harmonic cancellation is achieved by phase shifting each carrier by $(i-1)\pi/N$, where i is the i th converter, N is the number of series-connected single-phase inverters per phase leg. Then the output voltage of the cascaded H-bridge inverter can be expressed as:

$$V_{cas}^{pu} = 2M \cos(\omega_0 t) + \frac{8}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{2Nm} J_{2n-1}(Nm\pi M) \cos[(Nm+n-1)\pi] \times \cos[2Nm\omega_c t + (2n-1)\omega_0 t]. \quad (6)$$

A general description of the cascaded multilevel active power filter

Fig.3 shows the circuit diagram of the seven-level cascaded APF based on three H-bridge modules, where v_{ci} and v_{ai} ($i=1, 2, 3$) represents the dc-link capacitor voltage and output voltage of each H-bridge, respectively. Each H-bridge includes four switches with anti-parallel diodes and a dc-link capacitor. The output voltages of the cascaded H-bridge inverter can be derived as:

$$v_{aN} = v_{a1} + v_{a2} + v_{a3}. \quad (7)$$

Assuming $v_{c1}=v_{c2}=v_{c3}=V_{dc}$ in steady state conditions and three-level modulation is adopted for each module, i.e., each module produces three different voltage levels: $-V_{dc}$, 0 , V_{dc} . With reference to the upper bridge, it is possible to set $v_{a1}=+V_{dc}$ by turning on power switches S_{11} and S_{14} and $v_{a1}=-V_{dc}$ by turning on power switches S_{12} and S_{13} . Moreover, it is possible to set $v_{a1}=0$ by turning on either S_{11} and S_{12} or S_{13} and S_{14} , the lower bridge operates in a similar manner. Therefore, seven distinct voltage levels can be synthesized at the ac terminals. It should be noted that the switching states of S_{x1} , S_{x2} ($x=1, 2, 3$) must be complementary to those of S_{x3} , S_{x4} ($x=1, 2, 3$) in order to avoid short circuit of the H-bridge modules.

Defining the following switching functions

$$\begin{cases} f_1 = S_{11} \cdot S_{14} - S_{12} \cdot S_{13}; \\ f_2 = S_{21} \cdot S_{24} - S_{22} \cdot S_{23}; \\ f_3 = S_{31} \cdot S_{34} - S_{32} \cdot S_{33}. \end{cases} \quad (8)$$

The value of f_x ($x=1, 2, 3$) indicates the dynamic process of charging and discharging between the dc-link capacitors C_1 , C_2 and C_3 . Supposing the APF current i_{af} is positive, then the capacitor C_x ($x=1, 2, 3$) is charging if $f_x=1$, discharging if $f_x=-1$, and not undergoing any of these processes if $f_x=0$. Complementary phenomenon appears if the inverter current is negative.

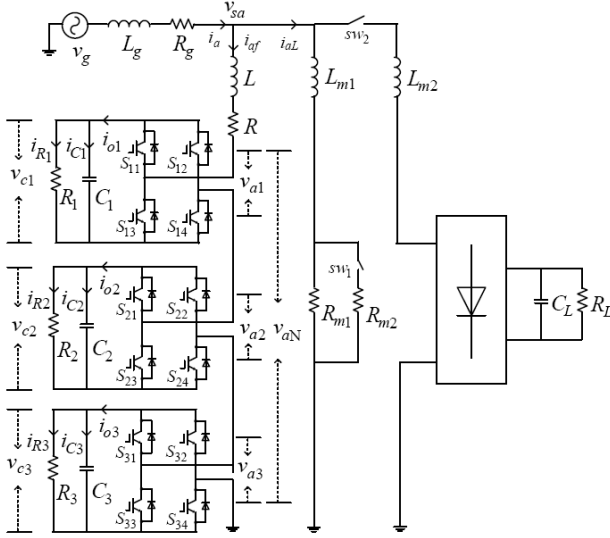


Fig. 3. Simplified single-phase schematic of cascaded multilevel active power filter

Mathematical modeling

The following assumptions are made for deriving the mathematical model of the cascaded H-bridge inverters.

(a) The grid is assumed to be AC current source,

(b) The power losses of the whole system are categorized as series loss and parallel loss. The series loss and interfacing inductor loss are represented as equivalent series resistance (ESR). Parallel losses are represented as shunt connected resistances across the dc-link capacitors, corresponding to the active power losses of the H-bridges, including blocking losses, capacitor losses and absorbing circuit losses, etc.

The differential equation describing the dynamics of the coupling inductor between the cascaded H-bridge inverter and the grid can be derived as:

$$v_{sa} = Ri_{af} + L \frac{di_{af}}{dt} + f_1 v_{c1} + f_2 v_{c2} + f_3 v_{c3}, \quad (9)$$

where the variable v_{sa} represents grid voltage, L represents the inductance of the coupling inductor and R represents the equivalent series resistance (ESR). The variables v_{c1} , v_{c2} and v_{c3} are actual voltages across the dc-link capacitors of the cascaded H-bridge inverter, which may not equal to the reference voltage V_{dc} during dynamic process.

According to kirchoff's law, the currents flowing into the dc-link capacitors C_1 , C_2 and C_3 can be expressed as:

$$\begin{cases} i_{c1} = C_1 \frac{dv_{c1}}{dt} = i_{o1} - i_{R1} = f_1 i_{af} - \frac{v_{c1}}{R_1}; \\ i_{c2} = C_2 \frac{dv_{c2}}{dt} = i_{o2} - i_{R2} = f_2 i_{af} - \frac{v_{c2}}{R_2}; \\ i_{c3} = C_3 \frac{dv_{c3}}{dt} = i_{o3} - i_{R3} = f_3 i_{af} - \frac{v_{c3}}{R_3}; \end{cases} \quad (10)$$

where R_1 , R_2 and R_3 are the equivalent resistance of each H-bridge representing parallel losses of H-bridges. The variables i_{o1} , i_{o2} and i_{o3} represent the total dc-link current and i_{R1} , i_{R2} and i_{R3} represent the current in the dc-link resistance of the individual H-bridge module.

The equations (9)-(10) can be rearranged as:

$$\begin{cases} \frac{di_{af}}{dt} = \frac{v_{sa}}{L} - \frac{R}{L} i_{af} - \frac{f_1 v_{c1}}{L} - \frac{f_2 v_{c2}}{L} - \frac{f_3 v_{c3}}{L}; \\ \frac{dv_{c1}}{dt} = \frac{f_1 i_{af}}{C_1} - \frac{v_{c1}}{R_1 C_1}; \\ \frac{dv_{c2}}{dt} = \frac{f_2 i_{af}}{C_2} - \frac{v_{c2}}{R_2 C_2}; \\ \frac{dv_{c3}}{dt} = \frac{f_3 i_{af}}{C_3} - \frac{v_{c3}}{R_3 C_3}. \end{cases} \quad (11)$$

Let the vector of state variables as $X_3 = [i_{af}, v_{c1}, v_{c2}, v_{c3}]^T$ and $U_3 = [v_{sa}, 0, 0, 0]^T$, as input vector, equation (11) can be expressed in compact matrix form:

$$\dot{X}_3 = \mathbf{A}_3 X_3 + \mathbf{B}_3 U_3. \quad (12)$$

The matrices \mathbf{A}_3 and \mathbf{B}_3 can be simply derived as:

$$\mathbf{A}_3 = \begin{bmatrix} -\frac{R}{L} & -\frac{f_1}{L} & -\frac{f_2}{L} & -\frac{f_3}{L} \\ \frac{f_1}{C_1} & -\frac{1}{R_1 C_1} & 0 & 0 \\ \frac{f_2}{C_2} & 0 & -\frac{1}{R_2 C_2} & 0 \\ \frac{f_3}{C_3} & 0 & 0 & -\frac{1}{R_3 C_3} \end{bmatrix},$$

$$\mathbf{B}_3 = \begin{bmatrix} \frac{1}{L} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}.$$

The proposed control strategies for the cascaded H-bridge multilevel APF

Fig.4 shows the control block diagram for the i th H-bridge module of the cascaded APF, including the average dc-link voltage controller, individual voltage controller and the current loop controller. The average voltage controller is responsible for regulating the active power flow between the cascaded H-bridges and the grid. The output of the

average voltage controller is multiplied by a unit sine signal which is synchronized with grid voltage by using a phase-locked loop (PLL), and the obtained signal is used as the active component of grid-side reference current. The individual voltage control is achieved by regulating the difference of the individual dc-link voltage and the average dc-link voltage (Fig.4). The output of the individual voltage regulator is multiplied by a unit cosine signal, and used to regulate the reactive power distribution among the all the H-bridge modules.

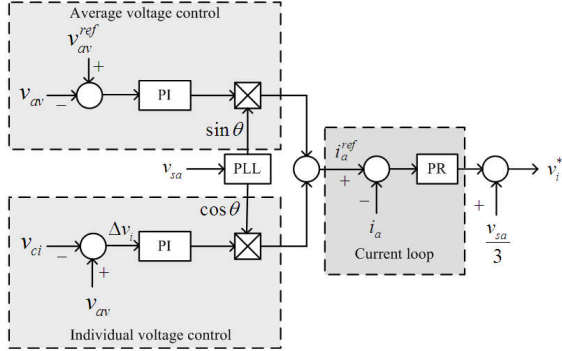


Fig. 4. Block diagram of the proposed control strategy for the i -th H-bridge module

Assuming v_{aN} is controlled such a manner that it lags v_{sa} by α_C rad, then active power absorbed by the APF is

$$P = \frac{v_{sa} v_{aN} \sin \alpha_C}{X}, \quad (13)$$

where X is the impedance of the interface inductor. Under ideal condition, the average charge to each dc capacitor over half cycle $[0, \pi]$ can be expressed as:

$$Q_i = \int_{\theta_i}^{\pi-\theta_i} \sqrt{2}I \cos \theta d\theta = 0, \quad (14)$$

where $\theta \in [\theta_i, \pi-\theta_i]$, represents the time interval when the dc capacitors are connected to the grid, and I is the RMS value of the inverter current. Theoretically, due to the symmetric power flow, all the dc-link capacitor voltages remain balanced. However, the H-bridge modules are not ideal due to unequal power loss and parameter differences, each dc-link voltage cannot be exactly balanced when only the average voltage control is used. When v_{ai} is shifted by $\Delta\alpha_{Ci}$, then the charge Q_i can be expressed as

$$Q_i = \int_{\theta_i-\Delta\alpha_{Ci}}^{\pi-\theta_i-\Delta\alpha_{Ci}} \sqrt{2}I \cos \theta d\theta = 2\sqrt{2}I \cos \theta_i \sin \Delta\alpha_{Ci}, \quad (15)$$

which is proportional to $\Delta\alpha_{Ci}$ when $\Delta\alpha_{Ci}$ is small. Usually this phase shift is much smaller than α_{Ci} , hence the individual voltage control block is included to balance power losses of the H-bridge so as to maintain a constant dc-link voltage.

The proportional-resonant controller is adopted in the current loop, which can be expressed as:

$$G_c(s) = k_p + \sum_{n=2N+1} \frac{k_{in}s}{s^2 + \omega_n^2}, \quad (16)$$

where k_p , k_{in} represents the proportional and integration gain, respectively. And n represents the harmonic orders to be attenuated, for the single-phase system, $n=2N+1$ (N is integer). For the present case, the 3rd, 5th, 7th and 9th order harmonics are considered. And k_p , k_{in} are selected to be 15 and 35, respectively.

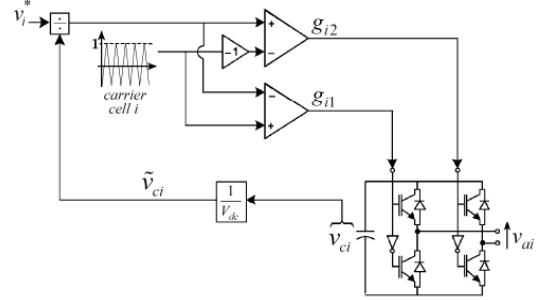


Fig. 5. Schematic of the gating signal generation mechanism for the i -th H-bridge module

The PWM mechanism for generating the switching patterns to the individual H-bridge modules is shown in Fig.5. The calculated modulation voltage is divided by the normalized dc-voltage of individual H-bridge module, then gating signals for each H-bridge module can be obtained by comparison with the phase shifted PWM carrier.

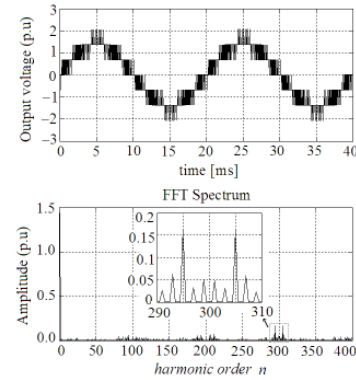


Fig. 6. Output voltage and its FFT spectrum of the cascaded APF based on three H-bridge modules

Simulation results and discussions

Fig. 7–12 show the simulation results of the proposed system under various scenarios. As shown in Fig. 3, the nominal system parameters are: $V_g=220\text{V}$ (RMS), $L_g=50\mu\text{H}$, $R_g=0.05\Omega$, $C_1=C_2=C_3=C_L=5000\mu\text{F}$, $L_f=500\mu\text{H}$, $L_{m1}=10\text{mH}$, $L_{m2}=1\text{mH}$, $R_1=R_2=R_3=1\text{k}\Omega$, $R_{m1}=R_{m2}=10\Omega$, $R_L=30\Omega$, and the dc-link reference voltage for each module is: $V_{dc}=150\text{V}$.

In order to investigate the robustness of the proposed control strategy, the non-homogenous H-bridge module situation is also considered, the circuit parameters under this situation are: $C_1=5000\mu\text{F}$, $C_2=5200\mu\text{F}$, $C_3=5400\mu\text{F}$, $R_1=1\text{k}\Omega$, $R_2=1.1\text{k}\Omega$, $R_3=0.9\text{k}\Omega$ and the other system parameters remain unchanged.

Note that, when $t<0.5\text{s}$, only the average voltage controller is enabled and the individual voltage controller is also enabled after $t=0.5\text{s}$. Besides, a sudden increase of load is applied at $t=1.0\text{s}$ by turning on the switch sw_1 to test the dynamic performance of the system. Fig. 7 shows the individual and average dc-link capacitor voltage under homogenous H-bridge module scenario. Fig. 8 shows the

differences between the individual dc-link voltage and the average dc-link voltage, Δv_i ($i=1, 2, 3$). It can be observed that the difference voltage Δv_i shows a trend of divergence before $t < 0.5s$. However, when the individual voltage control is applied at $t=0.5s$, Δv_i converges to zero, which implies that the whole system is stabilized after $t=0.5s$.

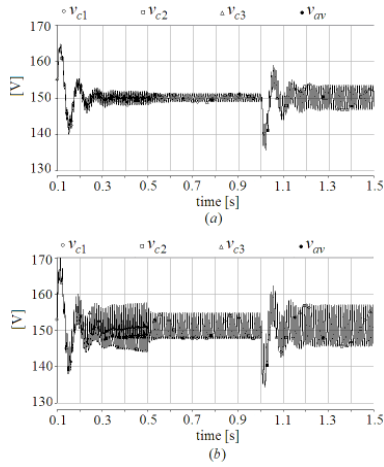


Fig. 7. Individual and the average dc-link capacitor voltage of the cascaded APF (a) reactive compensation mode, (b) reactive and harmonic compensation mode in case of homogeneous H-bridges

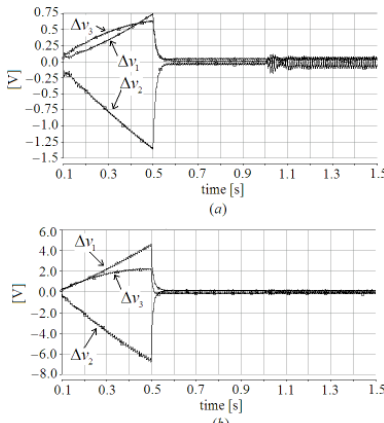


Fig. 8. Difference voltages of dc-link capacitors of the cascaded APF (a) reactive compensation mode, (b) reactive and harmonic compensation mode in case of homogeneous H-bridges

Fig. 9-10 show the corresponding simulation results under non-homogenous H-bridge module scenarios. The different parameters in the H-bridge modules imply the different switching losses in each module, which may be the worst case for the practical systems.

It is interesting to notice that Fig.9 resembles Fig.7 in the sense that the transient response almost has same dynamic behaviour and the difference of the dc-link voltage Δv_i converges to zero after $t=0.5s$ when the individual voltage controller is enabled. Further, sufficient stability under transient load disturbance is also observed in case of non-homogeneous H-bridge scenarios. Besides, it can also be noticed that the voltage ripple in case of reactive compensation mode is much smaller than that of reactive and harmonic compensation mode.

Fig.11 shows the simulation results of load current, APF current and grid current and voltage, corresponding to reactive power compensation mode, when the switch

denoted by sw_2 is turned off (Fig.3). It can be observed from Fig. 11 that the grid current and voltage are in phase under both steady state and transient load variations. Hence unity power factor at source side is achieved.

Note that, the currents under non-homogeneous H-bridge modules scenario are almost same as those under homogenous module scenario. Hence the waveforms of the non-homogenous H-bridge situation are omitted here.

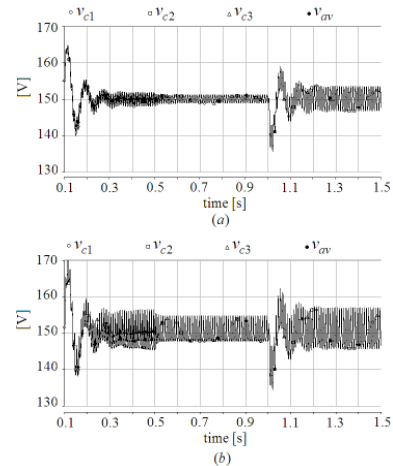


Fig. 9. Individual and the average dc-link capacitor voltage of the cascaded APF (a) reactive compensation mode, (b) reactive and harmonic compensation mode in case of non-homogeneous H-bridges

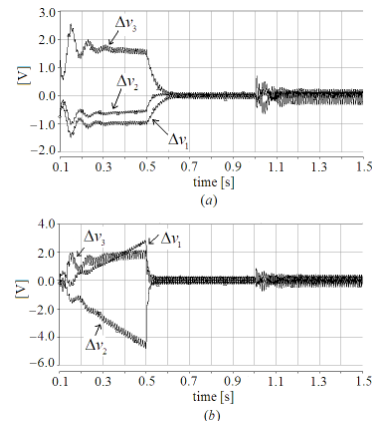


Fig. 10. Difference voltages of dc-link capacitors of the cascaded APF (a) reactive compensation mode, (b) reactive and harmonic compensation mode in case of non-homogeneous H-bridges

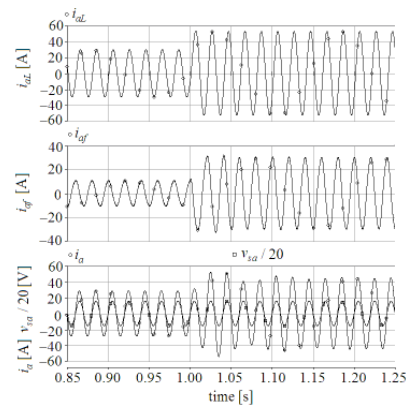


Fig. 11. Waveforms of load current, APF current, source-side current and voltage under reactive compensation mode.

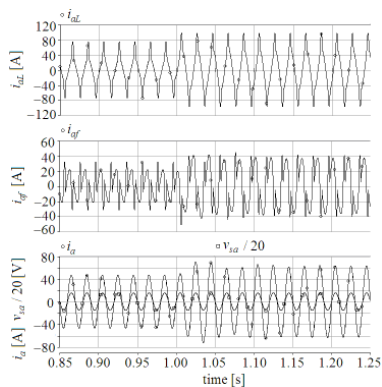


Fig. 12. Waveforms of load current, APF current and source-side current and voltage under reactive and harmonic compensation mode.

Fig. 12 shows the simulation results when the system is under reactive and harmonic compensation mode when the switch sw_2 is turned on, while the control parameters remain unchanged. It shows that the cascaded APF compensates both the reactive and harmonic current of the nonlinear load, and the grid-side current and voltage remain in phase hence unity power factor is also ensured. It can be concluded that the cascaded H-bridge APF provides flexible reactive and harmonic compensation capability, and the grid currents can be restored into pure sinusoidal wave shapes without harmonic contamination.

Conclusions

This paper reports the operation principles of the cascaded H-bridge multilevel active power filters (APFs). The phase shift cascaded PWM (PSCPMW) is adopted to generate the gating signals for each H-bridge module.

A novel dc-link capacitor voltage balancing strategy is proposed by regulating the average dc-link voltage and the difference of individual dc-link voltage with respect to the average dc-link voltage. The proportional and resonant (PR) controller is adopted in the current-loop for reference current tracking. Sufficient stability characteristic of the dc-link voltages is achieved under steady state conditions and transient load variations, which substantially confirms the validity and robustness of the proposed control scheme.

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The operation principles and control strategies of the cascaded H-bridge multilevel APF are reported. The phase shift cascaded pulse-width modulation (PSCPWM) is adopted to generate gating signals for each H-bridge module. A novel voltage balancing control of dc-link capacitors is proposed. The reference tracking is realized by the proportional and resonant controller in the current loop. The validity of the proposed control scheme is validated by the simulation results under both homogenous and non-homogenous H-bridge module scenarios. Il. 12, bibl. 5 (in English; summaries in English, Russian and Lithuanian).

Янг Хан, Лин Ху, Ганг Яо, Ли-Дан Зхоу, Мансур, Чен Чен. Принципы действия и методы управления H-моста многоступенчатого активного фильтра // *Электроника и электротехника*. – Каунас: Технология, 2009. – № 3(91). – С. 71–76.

Анализируются принципы действия H-моста ступенями соединенного многоступенчатого активного фильтра мощности и методы управления им. Для генерации затворных сигналов для каждого модуля H-моста использована ступенчатая модуляция ширины импульса фазного сдвига. Предложен новый способ управления балансом напряжений конденсаторов. Опорный сигнал фиксируется применяя в петле тока пропорциональное и резонансное управляющее устройство. Пригодность предложенной схемы управления подтверждено результатами моделирования. Ил. 12, библи. 5 (на английском языке; рефераты на английском, русском и литовском яз.).

Yang Han, Lin Xu, Gang Yao, Li-Dan Zhou, Mansoor, Chen Chen. Daugiapakopio aktyvaus galios filtro H tiltelio veikimo principai ir valdymo metodai // *Elektronika ir elektrotechnika*. – Kaunas: Technologija, 2009. – Nr. 3(91). – P. 71–76.

Analizuojami daugiapakopio aktyvaus galios filtro H tiltelio veikimo principai ir valdymo metodai. Kiekvieno H-tiltelio modulio užtvariniams signalams generuoti panaudota pakopinė fazės poslinkio impulso pločio moduliacija (PSCPWM). Pasiūlytas naujas kondensatorių įtampos balanso valdymo būdas. Atraminis signalas sekamas srovės kilpoje naudojant proporcinį ir rezonansinį valdiklį. Pasiūlytosios valdymo schemos tinkamumą patvirtina tiek homogeninio, tiek nehomogeninio H tiltelio modulio modeliavimo rezultatai. Il. 12, bibl. 5 (anglų kalba; santraukos anglų, rusų ir lietuvių k.).