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Testability Analysis Approach TADATPG for Deterministic Test Generation

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Introduction

Recent methods of the test pattern generation must be more intellectual. This idea lies in the basis of the SIGETEST system [1]. This system was developed by task group of Kharkov National University of Radio Electronics under the direction of ALDEC Inc. (USA). Such system should include testability analysis, which incorporates different aspect of testing methodology. One of the important tasks is testability analysis realization in the deterministic ATPG (Automatic Test Pattern Generation) systems. Such systems destined for test generation for asynchronous combinational and sequential logic circuits, unconditional of the DFT (Design for Test) methods. Also, that can not be tested pseudo-randomly in DFT-systems for combinational circuits or subcircuits.

When authors have tried to use classical methods of the testability analysis, they found some problems, which will be mentioned later in the article. That pushed to the development of a new method of the testability analysis.

Comparative analysis of existing methods

The pioneering work in this area was done by Rutman [2] and independently by Stephenson and Grason [3, 4]. This work relates primarily to deterministic ATPG. Rutman's work was refined and extended by Breuer [5]. These results were popularized then in the papers describing the Sandia Controllability/Observability Analysis Program (SCOAP) [6, 7]. This work, in turn, formed the basis of several other systems that compute deterministic controllability and observability values, such as TESTSCREEN [8, 9], CAMELOT (Computer-Aided Measure for Logic Testability) [10], and VICTOR (VLSI Identifier of Controllability, Testability, Observability, and Redundancy) [11], also [12, 13, 14].

These systems compute a set of values for each line in a circuit. There are two problems [15]. First, the correlation between testability values and test generation costs has not been well established. Second, it is not clear how to modify a circuit to improve the value of these testability measures. Naive rule-of-thumb procedures, such as add test points to lines having the worst observability values and control circuitry to lines having the worst controllability values, are usually not effective. In [12] more complex approach was offered, but its computational complexity is too high to be used in practice. Most of the present methods include complicated calculations and can be used only for simple circuits. It is hard to analyse them [15,16].

For comparative analysis three methods were selected here: Method1 [14], Method2 (CAMELOT) [10], Method3 (SCOAP) [7]. As investigations showed, in the method1 the values of the testability coincide with controllability values of the same nodes in the Method2. Hence, Method1 was mapped out. For comparison of Method3 to Method2 adjusted values were used. Authors detected the overflow of the bit plane in the Method3, when complex circuits were tested. Analysis of the circuit c6288 from ISCAS'85 Library has shown this. Hence it was impossible to make further analysis. In Method2 some values of the observability (about 16 percent of lines and more) are equal zero when calculation accuracy is 10^{-15}. It is not true and reduce adequacy of the analysis. Thus, mentioned methods are non-applicable even for relatively small circuits. Developed method, which is described further, does not contain mentioned disadvantages.

Calculation of the controllability

As above-listed methods, TADATPG is algorithmic method, which allows analyzing circuit on the gate level. Values of the testability are calculated for each node.

Controllability CY – the quantity of ability of the device to generate value 0 (CY^0) or 1(CY^1) on a set line which depends on a logic function of the device. It decreases with the increase of a distance of a line from external inputs of the circuit. Controllability can take the relative value, which belong to [0; 1] interval.

$CY = 1$ – has primary inputs of the device, where it is possible to set logic '0' and '1'. $CY = 0$ – has line, that can not be set to any of the logic values.

Practically, most values of the controllability are situated between the limits of range [0; 1]. In general case, controllability of inputs of the gates is not equal 100%. Therefore controllability must consider ability to transmit logic values from gate (Fig.1) and values of the controllability on its inputs:

$$CY^0(Y) = KCY^0 \cdot f^0, \quad (1)$$

$$CY^1(Y) = KCY^1 \cdot f^1, \quad (2)$$

where KCY – coefficient of the controllability transfer, that is defined by the logic function of the gate (KCY^1 – for setting of logic one on the output of the gate, KCY^0 – for setting of logic zero on the output of the gate).

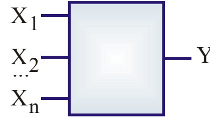

Fig. 1. Logic gate

Coefficients of the controllability transfer are defined by these expressions:

$$KCY^0 = \frac{N(0)}{N(1) + N(0)}, \quad (3)$$

$$KCY^1 = \frac{N(1)}{N(1) + N(0)}, \quad (4)$$

where $N(0)$ ($N(1)$) – number of all methods of setting of logic zero (one) on the primitive output line. f^0 – function, which is defined by formula:

$$f^0 = [\sum_{\forall z^0} \frac{CY^i(X_1) + CY^j(X_2) + \ldots + CY^k(X_n)}{n}] / m, \quad (5)$$

where n – number of gate's inputs; z^0 – input patterns ($X_1, X_2, \ldots, X_n$), which allow to obtain logic '0' on the output Y; m – number of patterns z^0; $i,j,\ldots,k \in \{0,1\}$ and equal to 0, if $X_1, X_2, \ldots, X_n$ on z^0 are equal to zero value; and equal to 1, if $X_1, X_2, \ldots, X_n$ on z^0 are equal to one value; f^1 – function, which defined by formula:

$$f^1 = [\sum_{\forall z^1} \frac{CY^i(X_1) + CY^j(X_2) + \ldots + CY^k(X_n)}{n}] / p, \quad (6)$$

where n – number of gate inputs; z^1 – input patterns ($X_1, X_2, \ldots, X_n$), which allow to obtain logic '1' on the output Y; p – number of patterns z^1; $i,j,\ldots,k \in \{0,1\}$ and equal to 0, if $X_1, X_2, \ldots, X_n$ on z^1 and take on '0' values, and, equal to 1, if $X_1, X_2, \ldots, X_n$ on z^1 take on '1' values. Sum of z^0 and z^1 patterns is equal to 2^n. For example, for two-port gate "NOT-AND":

z	X_1	X_2	i	k
$\forall z^0$	1	1	1	1
$\forall z^1$	0	0	0	0
	0	1	0	1
	1	0	1	0

And also $p = 3$, $m = 1$, $n = 2$, thus

$$f^0 = \frac{CY^1(X_1) + CY^1(X_2)}{2} / 1,$$

$$f^1 = [\frac{CY^0(X_1) + CY^0(X_2)}{2} + \frac{CY^0(X_1) + CY^1(X_2)}{2} + \frac{CY^1(X_1) + CY^0(X_2)}{2}] / 3.$$

Calculation of controllability is beginning from primary inputs to primary outputs.

It is not necessary to solve linear equations for sequential circuits, as in classical methods, because the fan-outs must be cut.

Calculation of the observability.

Observability OY – the quantity of ability of the device to transport a condition of considered line on external outputs of the circuit which depends on logic functionality of the device. Observability can take a relative value in [0; 1].

$OY = 1$ for primary output of the device. $OY = 0$, if it is impossible to change the logic value on the primary output by changing logic value in the node. Practically, most values of the observability are situated between the limits of range [0; 1].

In general case, transferring faults through primitive (logic gate) from inputs to output is depends on the ability to activate the appointed input. It depends on the ability to set the fixed values on the some/all inputs, which allows activating the path to appointed output of the device (the function of the controllability of these inputs).

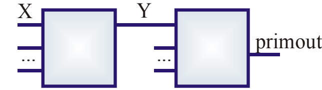

Fig. 2. Observability calculation

Therefore, observability is defined by the equation:

$$OY(X - primout) = OY(Y - primout) \cdot g, \quad (7)$$

where $primout$ – primary output of device; $X - Y - primout$ – activation path; g – arithmetic mean of values of the controllability (on the inputs), which ensures activation of the input X to output Y.

$$g = \frac{CY^i(X_1) + CY^j(X_2) + \ldots + CY^k(X_{n-1})}{n-1}, \quad (8)$$

where n – number of inputs of device; ($X_1, X_2, \ldots, X_{n-1}$) – input patterns ($z_a$), which provides the activation of $X_n - Y$ path; $i,j,\ldots,k \in \{0,1\}$ and equal to 0, if $X_1, X_2, \ldots, X_{n-1}$ on z_a take on '0' values, and, are equal to 1, if $X_1, X_2, \ldots, X_{n-1}$ on z_a take on '1' values.

For example, for three-input AND gate $OY(X_1 - primout) = OY(Y - primout) \cdot [CY^1(X_2) + CY^1(X_3)]/2$.

$CY^1(X_2)$ and $CY^1(X_3)$ are selected, because $X_2 = X_3 = 1$ provide path activation from input X_1 to output Y of gate. Inverter and repeater have one input and one output, observability of input is equal to observability of output. In case of fan-outs (Fig. 3) the observability is defined for each of the paths and the arithmetic mean of observability is taken by (9).

In this case the observability must be considered for each path, because some paths can not be locked.

$$OY(Y-U)=[\sum_{i=1}^{t} OY(Y_i-U)]/t. \quad (9)$$

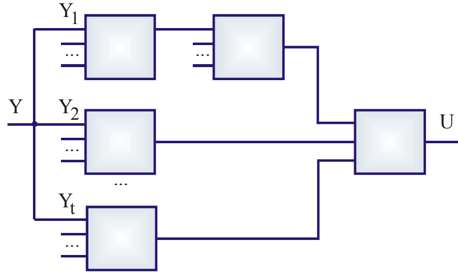

Fig. 3. Circuit with fan-outs

Fork can be present at the output (Fig 4). In this case node Y can be observed on primary output $primout1$ and on primary output $primout2$. Two values of observability can be obtained $-OY(Y-primout1)$ and $OY(Y-primout2)$.

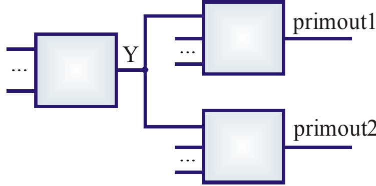

Fig. 4. Case of fork

In this case we have a problem of system reliability with parallel connection of elements.

In observability terminology, node state can be observed on the primary output when one of paths are activated. If more than one paths can be activated, then

$$OY(complex)=1-\prod[1-OY(primout_i)]. \quad (10)$$

For case which was presented on Fig. 4 observability of path Y - (primout1, primout2) can be obtained by (11).

$$OY(Y\text{-}(primout1,\ primout2)) = 1-([1-OY(Y-primout1)]\cdot[1-OY(Y-primout2)]), \quad (11)$$

Values of observability are calculated from primary outputs to primary inputs.

Calculation of the testability.

Testability of node can be calculated as multiplication of it controllability and observability.

$$TY^0(Y)=CY^0(Y)\cdot OY(Y), \quad (12)$$

$$TY^1(Y)=CY^1(Y)\cdot OY(Y), \quad (13)$$

$$TY(Y)=(TY^0(Y)+TY^1(Y))/2, \quad (14)$$

where $TY^0(Y)(TY^1(Y))$ – 0 – testability (1- testability) of node Y; $TY(Y)$ – testability of node Y.

General value of circuit's testability can be presented as measure of average laboriousness of test generation for circuit's node; therefore, this measure can be presented as an arithmetic mean of testabilities of all nodes in circuit, i.e.

$$TY_{circuit}=[\sum_{i=1}^{L} TY(Y_i)]/L, \quad (15)$$

here $TY_{circuit}$ - general testability of circuit; L – number of nodes in circuit.

For convenient interpretation of the results it is taken the 8-th root of the controllability, observability and testability values.

Method complexity (performance) is linear.

Example. Let's calculate values of the controllability, observability and testability of each lines of the given combinational circuit.

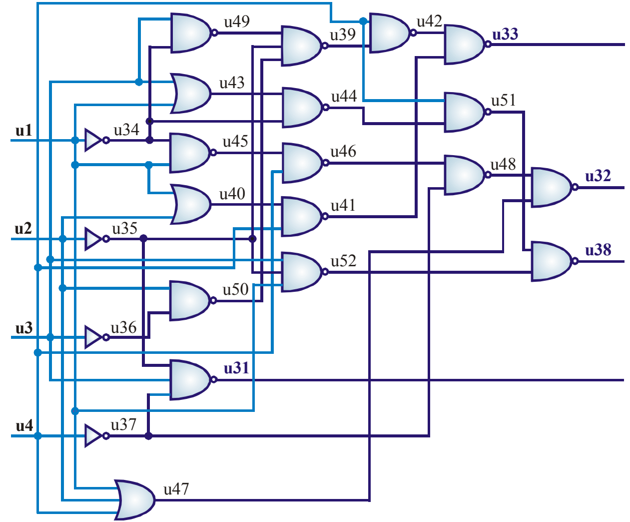

Fig. 5. Sample of combinational circuit

Fault coverage on deterministic test is Q=92,308%. In circuit: 4 inputs, 4 outputs, number of lines– 26, gates – 22.

Table 2. Testability measure before circuit's modification

CY^0	CY^1	OY	TY^0	TY^1	TY	Line
1.000	1.000	0.784	0.784	0.784	0.784	u2
1.000	1.000	0.861	0.861	0.861	0.861	u3
1.000	1.000	0.784	0.784	0.784	0.784	u4
1.000	1.000	0.761	0.761	0.761	0.761	u1
0.840	0.964	0.797	0.670	0.769	0.720	u40
1.000	1.000	0.361	0.361	0.361	0.361	u36
0.840	0.964	0.630	0.530	0.608	0.569	u43
1.000	1.000	0.591	0.591	0.591	0.591	u34
1.000	1.000	0.816	0.816	0.816	0.816	u37
1.000	1.000	0.783	0.783	0.783	0.783	u35
0.792	0.936	0.936	0.742	0.877	0.810	**u47**
0.964	0.840	**0.361**	0.349	0.304	0.326	**u49**
0.936	0.792	1.000	0.936	0.792	0.864	u31
0.923	0.826	0.653	0.603	0.540	0.572	u44
0.964	0.840	0.523	0.505	0.440	0.472	u45
0.923	0.826	0.826	0.764	0.683	0.724	u41
0.964	0.840	0.361	0.349	0.304	0.326	u50
0.936	0.792	0.792	0.742	0.628	0.685	u52
0.924	0.790	0.790	0.730	0.624	0.677	u51
0.936	0.792	0.622	0.583	0.493	0.538	u46
0.915	**0.776**	0.608	0.556	0.472	0.514	**u39**
0.867	0.665	1.000	0.867	0.665	0.766	u38
0.926	0.785	0.785	0.727	0.616	0.672	u48
0.920	0.783	0.783	0.720	0.613	0.667	u42
0.847	0.742	1.000	0.847	0.742	0.795	u32
0.862	0.678	1.000	0.862	0.678	0.770	u33

General value of testability $TY_{circuit}$ = 0,400464.

Strategy of modification for combinational circuits

As experiments showed, method allows executing simple procedure of bottlenecks selection for circuit's modification.

Strategy of points' selection for modification consists in following statements: 3% of lines with minimal values of CY^0 (with the exception of primary inputs and outputs) are selected. Lines with indexes, which are equal to maximal value from selected lines, are added to them. Generally, number of such lines is not large; it is challenge of developed method. The same procedure is applied to indexes of CY^1 and OY. Obtained sets are combined.

Way of circuit modification consists of following statements: scan cell, which must to provide best controllability and observability, is placed on selected line. Such cell must be transparent for circuit normal functioning and easy to test.

Cells are combined in shift register as scan path in structural DFT methods for decreasing of number additional pins.

Boundary register scan cell (IEEE 1149.1 Boundary-Scan Standard) meet requirements with the exception of problem of testing it independently in circuit under test.

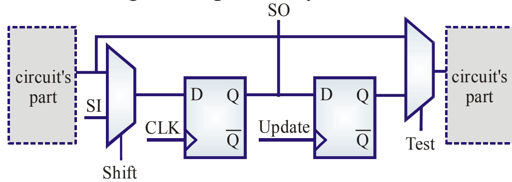

Fig. 6. Boundary scan cell

For decreasing area overhead and providing adequate testing of cell it is proposed to use the cell, presented on Fig. 7.

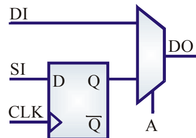

Fig. 7. Scan cell for combinational circuit

Cell consists of synchronous double-step D-trigger and multiplexer. DI – data input, DO – data output, SI – scan input, CLK – clock, A – address input. DI – DO – data transfer path on selected line.

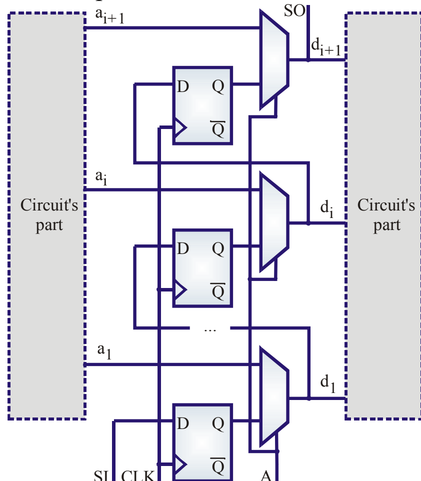

Fig. 8. Scan path

In Fig. 8: a_1, …, a_i, a_{i+1} – selected lines for circuit's modification, a_i replaced by path a_i – d_i, which pass through MUX. *SO* – scan output, which is also primary output. Testing of such circuit is executed by principle of scan path method. Standard tests are used for testing of shift register. After testing of address line, testing of CUT is executed. The cell of modified circuit can be completely tested independently. Proposed cell is absolutely transparent for normal functioning, therefore, test for combinational part of circuit is generated taking into account that selected lines must be cut.

Example. Let's consider way of modification of circuit presented in Fig. 5.

Set of additional scan lines {u47, u49, u39} are selected by using above mentioned strategy. Scan cells are placed on these lines for providing best controllability and observability. After that testability analysis is executed for modified circuit with opens (Table 3).

Table 3. Testability indexes after modification

CY^0	CY^1	OY	TY^0	TY^1	TY	Line
1.000	1.000	0.908	0.908	0.908	0.908	u2
1.000	1.000	1.000	1.000	1.000	1.000	u47.1
1.000	1.000	0.840	0.840	0.840	0.840	u39.1
1.000	1.000	0.839	0.839	0.839	0.839	u1
1.000	1.000	0.792	0.792	0.792	0.792	u49.1
1.000	1.000	0.801	0.801	0.801	0.801	u3
1.000	1.000	0.865	0.865	0.865	0.865	u4
0.840	0.964	0.630	0.530	0.608	0.569	u43
1.000	1.000	0.876	0.876	0.876	0.876	u34
0.840	0.964	0.797	0.670	0.769	0.720	u40
1.000	1.000	0.816	0.816	0.816	0.816	u37
1.000	1.000	0.666	0.666	0.666	0.666	u36
1.000	1.000	0.909	0.909	0.909	0.909	u35
0.792	0.936	1.000	0.792	0.936	0.864	u47
0.964	0.840	0.840	0.811	0.707	0.759	u42
0.964	0.840	0.666	0.643	0.560	0.601	u50
0.936	0.792	1.000	0.936	0.792	0.864	u31
0.964	0.840	0.523	0.505	0.440	0.472	u45
0.923	0.826	0.826	0.764	0.683	0.724	u41
0.964	0.840	1.000	0.964	0.840	0.902	u49
0.923	0.826	0.653	0.603	0.540	0.572	u44
0.936	0.792	0.792	0.742	0.628	0.685	u52
0.936	0.792	0.622	0.583	0.493	0.538	u46
0.924	0.790	0.790	0.730	0.624	0.677	u51
0.885	0.701	1.000	0.885	0.701	0.793	u33
0.926	0.785	1.000	0.926	0.785	0.855	u39
0.867	0.665	1.000	0.867	0.665	0.766	u38
0.926	0.785	0.785	0.727	0.616	0.672	u48
0.923	0.784	1.000	0.923	0.784	0.853	u32

General value of testability $TY_{circuit} = 0.482942$

After modification circuit model consists of 7 inputs, 7 outputs, 22 gates and 3 scan cells. Area overhead is equal 100%. Fault Coverage *FC* after modification is equal to 100%. Deterministic test generation and fault simulation is executed on model of circuit with opens.

Strategy of modification for sequential circuits

Strategy of synchronous sequential circuit's modification consists in following statements. All triggers in circuit are replaced by cell shown in Fig. 9. After that, indexes of testability are calculated for obtained

combinational circuit. Further circuit's modification is executed as for combinational circuit (Fig. 7, 8). It is organized as I type shift register (Fig. 8).

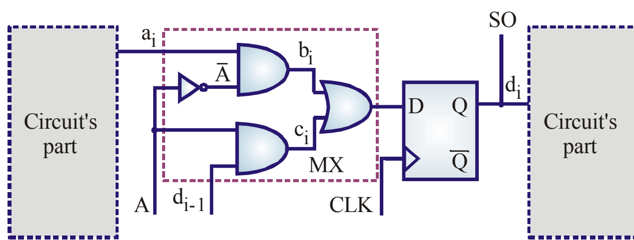

Fig. 9. Scan cell for sequential circuit

Obviously, some differences between cells for combinational and sequential circuits are present. A = 0 – normal functioning of circuit (mode of normal functioning of device - F). A = 1 – scan mode (SP). If number of cells is more than one, shift register is organized (Fig. 10).

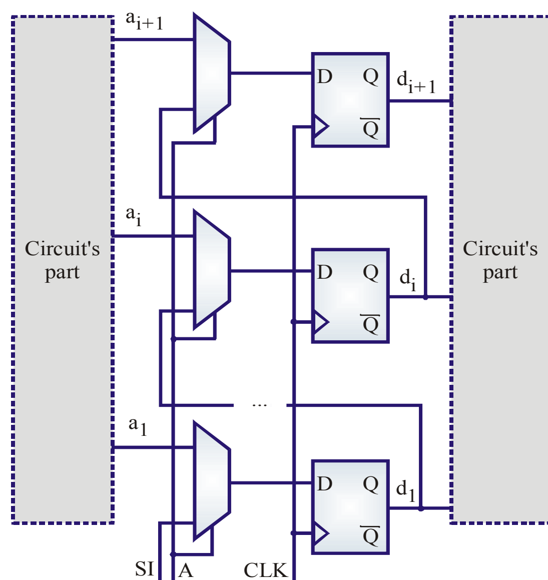

Fig. 10. Shift register of II type

Standard tests are used to test a shift register, (running zero (one), running pair zero (one)). Thus, two scan paths are organized, which can be combined into one.

Deterministic test for sequential circuit is generated taking into account that selected lines must be cut. Test procedure for sequential logic is executed as for combinational circuits.

Experimental results

Classical methods of the testability analysis, that were analyzed and a new method, proposed in our article, are implemented in SIGETEST system. VHDL-code is used as initial circuit schema. SIGETEST system converts the VHDL-code in internal circuit model. Mentioned methods use this model for testability analysis. Methods were approved on the circuits of different complexity, including circuits from ISCAS'85, '89, '99 library.

Experimental checks showed that developed method is more adequate in comparison with classical methods, taking into consideration problems described above. Indexes with zero values can be observed only in large circuits. For example, with calculation accuracy 10^{-31} in circuit c50000 ISCAS'85 2% from 49996 lines have indexes with zero values. However, correlation between indexes of testability and fault coverage does not always exist, therefore, minimization of area overhead by calculated values is impossible.

Table 4 shows the statistic for combinational circuits by use of proposed cell.

Table 4. Fault Coverage indexes for combinational circuits.

Circuit ISCAS'85	Scan Cells, %	Fault Coverage before modification	Fault Coverage after modification	Test
C432	7%	87,173%	100 %	Determ.
C499	6%	99,763%	100 %	Determ.
C880	9%	93,563%	100 %	Determ.
C3540	8%	97,798%	98,53 %	Random
C6288	6%	99,653%	99,81 %	Random
C20000	11%	72,094%	99,71%	Random

Table 5 shows the area overhead for combinational and sequential circuits from different ISCAS benchmarks based on different types of cell.

Table 5. Additional area overhead

ISCAS'85	BS Cell	New Cell	MUX		AND-OR	
	AAO, %	AAO, %	AAO, %	AP	AAO, %	AP
C432	111	88,9	25,9	59	14,8	87
C499	93,3	74,6	21,8	75	12,4	111
C880	143	114	33,3	115	19,1	171
C3540	135	107	31,4	315	17,9	471
C6288	90,3	72,3	21,1	569	12,1	852
C20000	331,2	132	77,3	4549	44,2	6822
ISCAS'99						
sb01	351	253	173	63	159	67
sb02	352	245	182	37	169	39
sb03	410	294	239	207	234	218
sb04	315	234	151	832	149	890
SCAS'89						
s208	269	201	122	160	108	170
s298	272	199,5	140	163	131	173
s344	366	274,9	175	234	158	255

In Table 5: AAO – additional area overhead (%), AP – number of additional pins. For BS Cell AP is equal to 6, for developed cell AP = 4. Table 6 shows statistics for sequential circuits from ISCAS'89, 99 with proposed cells.

Table 6. Fault Coverage for sequential circuits

ISCAS'99	Scan Cells, %		FC before modification, %	Test	FC after modification, %	Test
	Trigger +MUX	MUX				
sb01	10%	10%	96,667	Exh.	100	Rand.
sb02	8,8%	11%	92,308	Exh.	100	Rand.
sb03	6,7%	16%	98,077	Rand.	100	Rand.
sb04	8,3%	9,3%	91,969	Rand.	100	Rand.
ISCAS'89						
s208	8%	6%	99,537	Exh.	100	Rand.
s298	8%	10%	98,750	Exh.	100	Rand.
s344	11%	8%	99,123	Exh.	100	Rand.

Conclusions

Scientific novelty of the presented research results is determined by the following points:

1. More suitable method of testability analysis in comparison with classical methods was developed.
2. Strategy of bottlenecks selection and circuit's modification for improving it testability and obtaining best test quality was proposed.

Advantages: 1) simplicity of method when sequential circuits are analyzed; 2) simplicity of bottlenecks selection; 3) simplicity and regularity of circuit's modification; 4) complete test of scan cells independently of subcircuit; 5) ability to provide best fault coverage (minimum or zero number of undetected lines) before test generation;

The practical importance is defined by following points:

1. Offered approaches allow reducing area overhead about 20 – 30% for combinational circuits and about 100% for sequential circuits in comparison with Boundary Scan cell.
2. The mentioned strategies give an opportunity to use internal lines as external outputs of the device for significant increase of fault simulation speed.
3. Software implementation of method in SIGETEST system.

Method can be used when deterministic test generation is executed for combinational and sequential circuits, which are not constrained by DFT methods and in DFT-systems for combinational circuits or subcircuits, which can not be tested pseudorandomly. Also it can be used in SoC.

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E.N. Kulak, M.A. Kaminska, O.A. Guz, O.N. Parfentiy. Testability analysis approach TADATPG for deterministic test generation // Electronics and Electrical Engineering.– Kaunas: Technologija, 2006. – No. 2(66). – P. 5-10.

Method of testability analysis of digital circuits for deterministic test is offered. This approach is more suitable in comparison with existent classical methods. It is oriented to combinational and sequential circuits and based on topological analysis in gate level. The strategy of circuit's modification for improvement of fault coverage is proposed. Ill. 10, bibl. 16 (in English; summaries in English, Russian and Lithuanian).

Э.Н. Кулак, М.А. Каминская, О.А. Гузь, А.Н. Парфентий Метод анализа тестопригодности TADATPG для генерации детерминированного теста // Электроника и электротехника.– Каунас: Технология, 2006. – №2(66). – С. 5-10.

Предлагается метод анализа тестопригодности цифровых схем для детерминированного тестирования, более адекватный по сравнению с известными классическими методами. Он ориентирован на комбинационные и последовательностные схемы и основан на топологическом анализе их представления на вентильном уровне. Предлагается стратегия локализации точек схемы по просчитанным показателям для ее модификации, а также способ модификации схемы с целью сведения числа непроверяемых неисправностей к нулю. Ил. 10, библ. 16 (на английском языке; рефераты на английском, русском и литовском яз.).

E.N. Kulak, M.A. Kaminska, O.A. Guz, O.N. Parfentiy. Testuojamumo analizės metodas TADATPG determinuotiems testams generuoti // Electronics and Electrical Engineering.– Kaunas: Technologija, 2006. – No. 2(66). – P. 5-10.

Pasiūlytas skaitmeninių grandynų determinuoto testuojamumo analizės metodas. Šis metodas tinkamesnis palyginti su egzistuojančiais klasikiniais metodais. Jis yra skirtas kombinuotiems ir nuosekliesiems grandynams ir remiasi topologine analize ventilių lygmenyje. Siūloma taškų pagal apskaičiuotus modifikacijos rodiklius lokalizacijos strategija, taip pat grandynų modifikavimo būdas, leidžiantis pagerinti klaidų aptinkamumą. Il. 10, bibl. 16 (anglų kalba; santraukos anglų, rusų ir lietuvių k.).

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