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Thin Film Transistors Gas Sensors: Materials, Manufacturing Technologies and Test Results

M. C. Pereira, M. J. Martins, O. Bonnaud
Esc. Sec. de Gama Barros, Instituto Superior Técnico, Institut d'Electronic et Telecommunications de Rennes
e-mail: mcpereira_80@yahoo.com, mariajoaomartins@ist.utl.pt, olivier.bonnaud@univ-rennes1.fr

Introduction

Five of the most important performance specifications of a sensor are its sensitivity, linearity, frequency response, long-term stability and power consumption. Sensor sensitivity and linearity are important characteristics for high accuracy and high precision measuring systems. Environment, health, telecommunications and the automobile industries are driving research and development of further integrated multi-function and adaptive systems that feed on multi-frequency information provided by sensors with smaller power consumptions. And in some specific environment and health applications, long–term stability measurements is one the most important specifications.

Thin-film sensors are emerging as one of the most promising technologies for the manufacture of sensor blocks for those systems. These sensors are used in application-oriented systems, manufactured at smaller temperatures with reproductable and high-production techniques. Thin film sensors can also be integrated with post-signal processing CMOS technologies and consequently with low manufacturing and low maintenance cost systems.

In the next section, the authors analyse the evolution of large area electronics gas sensors and focus on the breakthroughs of thin-film transistors (TFTs) based technologies. The general characteristics of thin-film transistor (TFT) technologies are presented in the following sections: the structure of TFTs, the physical and electrical properties of the materials used in TFTs and how those properties are affected by the manufacturing processes parameters. A physics description and models overview of the thin film transistor (TFT) is discussed in the fifth section. The next section presents the structure, materials and manufacturing processes of air-gap thin-film transistors. Test and characterisation results are also discussed in this section. Air-gap thin-film transistors working as gas sensors present high sensitivity values in the presence of specific molecules, which could lead to new developments. Conclusions based on the five performance characteristics of a sensor, mentioned in the beginning of this introduction are presented in the last section of this paper.

Large Area Electronics Gas Sensors: the State-of-the-Art

The development of large area electronics at low temperatures is playing an ever-increasing role in medical, environment and automobile industries. The research over the last two decades in this area, namely on gas sensors, has led to:

- Time responses within tens of seconds to a few seconds for most examples with organic thin films [1-3] and semiconductor tellurium films[4], compared to a little more then a second for the tin oxide gas sensor [5, 6], due to carrier mobility differences. Recovery times vary from a few minutes [6], and tens of seconds for the PcPb films[1], and a few seconds for air-gap thin-film transistors[7].
- Sensitivity evolution within tens of vpm[1-2], 0.7 ng/ppm[3] for organic thin film sensors, and 50 V for 500 ppm for the tellurium sensor[4] varying with the gas concentration and operation temperature. Air-gap thin-film transistors present a linear variation of the drain current with humidity concentration of 10^6 between 20% to 60% humidity ratios [7]. Linear behaviour was also observed for the tellurium sensor from 0-100 ppm [4].
- Power consumption reduction from 1 W [1] to tens of mW [6], due to a reduction of size and mass of the heated membrane, thus allowing a pulse control of the temperature and reduction of switching times to milliseconds.

Several tests were also performed in deposition film methods, improving transistor stability and film conductivity. Thin-film transistor mobilities varied from tens of cm^2/V.s using a low pressure chemical vapour deposition method[8] to hundreds of cm^2/V.s with Metal Induced Lateral Crystallization (MILC)[9].

Some research for the development of organic film transistors arrangements in arrays for selective gas recognition will lead to the development of the e-nose [2]. Another trend is the pursuit of sensors compatible and integrated with the VLSI/CMOS processes.

Several technological challenges still remain and TFT sensors present several advantages over other technologies namely:

- Higher sensitivity than capacitive sensors and that it could surpass top sensitivity values of some organic thin film sensors [1-2] and some metallic oxide sensors [4-6], by using transistors instead of chemiresistors or other carrier mobility substrates [1].
- Higher carrier mobility in thin films of polycrystalline silicon will yield lower sensor switching times than in organic thin film sensors[9]. The time of recovery is also influenced by the carrier mobility [1-6], related also to the reversibility of the sensor (small hysteresis).
- Reproducibility at low cost and manufacture process compatibility with driven systems (silicon-on-insulator based process), allowing future integration of a hole signal processing system following the trend in gas sensors and bio sensors.
- Higher reliability, long-term stability and lower power than metallic oxide gas sensors[5-6] due to the non-existence of heaters.

The Structure and Manufacture poly-Si TFTs

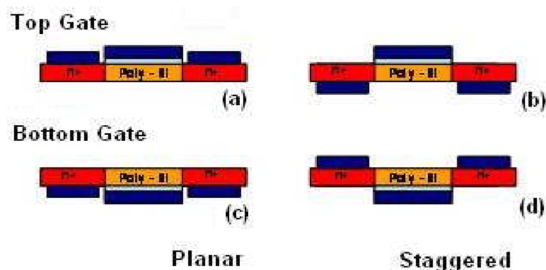

Fig. 1. Schematic diagrams of poly-Si TFTs: top-gate poly-Si TFT (a and b);down-gate poly-Si TFT (c and d) [8]

Unlike CMOS FETs, poly-Si TFTs are laid out on glass substrates at lower temperatures (smaller than 700ºC) and are used for large area applications (in the order of a few microns). As represented in figure 1, a TFT can be structured with the gate above or below the semiconductor layer. The drain and source contacts can also be positioned on the same side or in opposite sides as the gate contact to the poly-Si film.

The manufacture of thin film transistors follows an adapted sequence of mask definition, layer deposition and layer etching processes as the manufacture of CMOS circuits. The substrate is covered with an insulator, usually silicon nitride or silicon oxide, that isolates the device from the alkaline and water impurities contained in the glass. For the top gate planar structure (figure 1.a), the poly-Si film is deposited first, followed by the gate insulator film (silicon oxide). A metal film (aluminium) is deposited next to define the island of the gate contact. Next, ion-implantation of doping impurities and doping activation defines the source and drain regions not protected by the gate contact metal film (*in-situ* doping process). Another method uses the deposition of a doped Si layer for amorphous silicon TFTs (as-Si TFTs) of LCD screens. A new insulator layer is deposited and holes for the source and drain contacts are etched. A metal deposited layer defines those contacts. A thick silicon nitride or silicon oxide protective layer is deposited for mechanical, chemical and electrical protection of the device.

The deposition parameters of the poly-Si film, such as the temperature and the pressure determine the atoms arrangement of the film. For some intervals of pressure and temperature, the final result is a poly-Si film in the crystalline state, while for others the film remains in the amorphous state. For this latter situation crystallization and post-treatment processes are needed.

Materials and Process Parameters for the Manufacture of Poly-Si TFTs

For the manufacture of poly-Si thin film transistors (TFTs), two structural materials are mainly used: aluminium and polycrystalline silicon. Silicon oxide and silicon nitride are the insulator materials with the highest chemical compatibility with silicon, and therefore used as chemical, diffusion, thermal or mechanical barriers in the TFT structure.

The Polycrystalline Silicon Film. A high-quality polycrystalline silicon film is composed by grains or crystallites with longitudinal dimensions higher than the thickness of the film, without any internal defects and with small grain boundaries without any amorphous material. The generation of large grains in the film can be explained by the presence of few crystal seeds (low nucleation rate) that usually appear near the border between the base of the film and the insulator of the substrate. During crystallization, these seeds compete for amorphous material, rapidly growing in size. However, depending on the conditions of the crystallization process, this can lead to local areas of abrupt energy stabilization before all the amorphous material between the grains has been crystallized, forming a low quality film, with very small mobilities or even unusable TFTs. On the other hand, a high number of seeds (high nucleation rate) generate a large number of smaller grains without any or little internal defects and with very small borders. In these borders, the atoms of one grain usually connect directly to the atoms of the border grains. The bonds in the grain boundaries are weaker than the connections in the lattice. In silicon there are mainly tilted boundaries that have less structural disorder and smaller interfacial energies than the less common twisted boundaries [10]. The atoms arrangements are defined by their orientation in the <xyz> space axes and by Σn, where n is the number of atoms involved in periodic arrangements at those boundaries.

The size, orientation, distribution and quality of crystallites of the poly-Si film influences the electrical parameters of the TFT, like the mobility of free carriers. And as mentioned before, all of these physical characteristics are related with the film deposition method and its parameters (pressure and temperature). Silicon direct deposition techniques for thin film substrates are LPCVD (Low Pressure Chemical Vapour Deposition), PECVD (Plasma Enhanced Chemical Vapour Deposition) and the sputtering of silicon.

In Low Pressure Chemical Vapour Deposition (LPCVD) the deposited material is generated by thermal decomposition (pyrolysis) of precursor gases like silane

(SiH_4) or disilane (Si_2H_6) according to the chemical reactions: SiH_4 (g) → Si (s) + $2H_2$ (g) or Si_2H_6 (g) → 2Si (s) + $3H_2$ (g), respectively. Part of the generated hydrogen is captured in the grain boundaries, depending on the temperature (and on the pressure in a smaller degree) of the deposition process. A hydrogenation step or plasma exposure diffuses out part of the hydrogen, decreasing the number of dangling bonds in the grain boundaries, thus decreasing the reverse mode currents and increasing the threshold voltage in modulus[11]. So a little hydrogen is in fact, beneficial by improving the TFT electrical characteristics, but its presence in the film contributes to thermal instability [8]. A fine tuning in the temperature during deposition will assure adequate hydrogen "infiltration". The deposited film has crystalline properties for temperatures over 550ºC and pressures below 10^{-1} Torr and is in the amorphous state at temperatures from 500ºC to 550ºC, and pressures near 90 Pa [12]. Best results have been obtained for the latter, after additional crystallization and post-treatment processes [8].

In PECVD (Plasma Enhanced Chemical Vapour Deposition) the silicon film is generated through a chemical reaction by plasma at 200°C up to 450°C using precursor gases like silane (SiH_4) + fluoride (SiF_4) + hydrogen (H_2) or silane (SiH_4) + hydrogen (H_2) or silane (SiH_4) + dichlorosilane (DCS) (SiH_2Cl_2) + hydrogen (H_2) or other combinations of feed gases [8, 13, 14]. The substrate bias voltage controls the size of the crystallite. The size of the grain depends also on the substrate temperature, RF power and gas composition. The temperature controls the hydrogen content on the film like in the LPCVD process. For PECVD, better mobilities for top gate TFTs were obtained for 450 ºC with SiH_4 + SiF_4 + H_2 - 44 cm^2/V.s and for 230ºC with SiH_4 + SiH_2Cl_2 + H_2 - 20 cm^2/V.s [8, 14]. As a comparison with the previous deposition method, for LPCVD at 550º C and 100 Pa, it was measured a mobility of 53 cm^2/V.s [8]. Note that in this last TFT, the Silicon film was deposited in the amorphous state.

The other deposition method is sputtering, a physical process whereby atoms from a target material (doped or undoped) are ejected as a gas, due to bombardment by energetic ions or plasma, and deposited towards the substrate. The plasma may contain neutral species like SiH_2 and SiH_3, and other ionic species SiH_x with x varying from 0 to 4. The deposited material is in the amorphous state with grain sizes smaller than 10 nm [8].

If the film is deposited in the amorphous state, a crystallization step is needed. There are two main techniques:

1. Solid Phase Crystallization (SPC), that for best mobility results is used in a two-phase process: crystallization at low temperature (600ºC) for a low nucleation rate that will lead to the formation of large grains and a high temperature annealing (900ºC) to improve the grain quality by diffusing out the hydrogen content.

2. Laser crystallization used to obtain large grains by delaying the cooling process. The electrical field mobility reached 350 cm^2/Vs with a standard deviation of 5% [15].

The Aluminium Film. Aluminium is used as structural material in MEMS in spite of its smaller mechanical resistance to stress than polysilicon. A 150 nm thick film of polysilicon outstands up to 400 MPa of stress [16]. The deposition of aluminium is made in an air-tight chamber where a piece of solid aluminium with over 99,9% of purity is fused by Joule effect on a resistance. When the aluminium is in the liquid phase, the air is extracted from the chamber to create a vacuum that pulverizes homogenously the substrates attached to the top of the chamber. The film thickness is measured by spectrometry in nanometres.

Dielectric Materials.

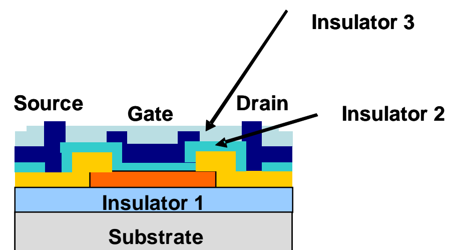

Fig. 2. Insulators for poly-Si TFT [8]

In the manufacture of thin film transistors, dielectric materials can have one or more functions according to the position in the TFT structure. Insulator one, the dielectric above the substrate is a thermal barrier during crystallization and a diffusion barrier to prevent contamination namely from water ions and alkaline ions of the glass substrate. Silicon nitride (Si_3N_4) films are better diffusion barriers than silicon oxide films.

The main requirement of the gate insulator is its electrical stability. The gate insulator influences several TFT electrical parameters, namely:

- The threshold voltage (V_T) that depends on the presence of charges in the insulator. This effect can be compensated by a higher doping level;
- The subthreshold slope (S) that depends on the fixed charges in the semiconductor and on the density of interface defects[8];
- The field effect mobility (μ_{FET}) that degrades due to the scattering of electrons caused by defects at the insulator-semiconductor interface. To lower the defect density at the gate insulator-semiconductor interface, the choice of a dielectric goes to the best chemically compatible material: silicon dioxide (SiO_2). Silicon nitride is a poor interface for poly-Si. To take advantage of its higher mechanical resistance a silicon nitride with silicon oxide dual gate TFT has been experimented in a TFT that showed a better $I_D(V_G)$ characteristic than an APCVD SiO_2 gate insulator regular TFT [17].

The dielectric above the device protects it from mechanical, chemical and electrical damages. A thick layer of silicon oxide is normally used.

The tetrahedral arrangements of silicon to oxygen atoms are formed by thermal oxidation of poly-Si or by the deposition of silicon oxide on silicon or glass substrates at low temperatures. The deposition of silicon oxide can be done by Physical Vapour Deposition (PVD) using RF sputtering or by Chemical Vapour Deposition (CVD) using LPCVD or PECVD. Silicon Nitride can be deposited by LPCVD for glass substrates or by PECVD. The latter

method is mainly used for the deposition of silicon nitride as gate insulator of hydrogenated as-Si TFTs.

Physics and Modelling of the poly-Si TFT

Physics Behaviour. The poly-crystalline structure of the TFT can be roughly described by internal defect free crystallites and their boundaries. The defect free crystallites have similar properties to those of monocrystalline silicon of VLSI FETs. The energy band diagram has a minimum conduction energy level and a maximum valence energy level with a gap of 1.12 eV (crystalline silicon), with no energy states between them.

Grain boundaries can be modelled as amorphous silicon. The difference between the minimum energy level of the conduction band and the maximum energy level of the valence band is 1.71 eV. Between those levels, there are several energy states with higher density of donor states near the valence level, and with higher density of acceptor states near the conduction level. These states are created due to distortions in the atomic bonds, unfilled or pending bonds with amphoteric behaviour and mainly due to the precipitation of doping atoms at the boundaries. The hydrogenation post-treatment passivates the dangling bonds, reducing the density of boundary states.

The difference in energy levels from crystallites to grain boundaries forms bends in the energy bands that behave as potential barriers from a crystallite to its neighbours. Assuming a columnar grain structure and a solid phase crystallization (SPC) method, these potential barriers are transversal to the current flow. For a n-type TFT, the grain boundary potential barriers decrease with increasing gate voltage and with increasing drain voltage (drain induced grain barrier lowering). The increase of the gate voltage frees carriers from the poly-Si to the channel region. In the thin film transistor, the drain current curve with the gate voltage changes from an exponential regime to a linear regime, as the gate voltage reaches the threshold value. The threshold voltage in TFT has a different meaning than the one used for MOSFET. The formation of the channel voltage is named "turn-on" voltage for the poly–Si n-type TFT. The threshold voltage is the gate voltage at which the relation $I_D(V_{GS})$ stops being exponential. The difference between these two values is typically 1 V [18]. The gate to source voltage and the drain to source voltage define the regions of operation of the TFT. Each region of operation is also characterized by a drain to source current resulting from the contribution of several conduction mechanisms.

Conduction Mechanisms. The conduction mechanisms in the crystallites are those of the MOSFET: drift of carriers mainly above the threshold region, and diffusion of carriers mainly at the subthreshold region. At the grain boundaries, in the conduction mode, there are two mechanisms [11]:

1. The carriers tunnel-through the grain boundary between the crystallites, when the extension of the space charge region is much smaller than the width of the crystallite, considering a cubic shape for all grains among other assumptions defined by the Seto's model[8]. The extension of the space charge region can be further minimized with higher doping concentrations.

2. When the extension of the space charge region is larger than the critical value defined by the Seto's model (the width of the crystallite), related with a higher height of the energy barrier, thermoionic emission causes electron scattering in the grain boundaries. The total scattering is given by:

$$\frac{1}{\mu} = \frac{1}{\mu_G} + \frac{1}{\mu_{eff}}. \quad (1)$$

In equation (1) the mobility in the film (μ) is related to the scattering in the grain (μ_G) and the scattering at the boundaries (μ_{eff}) in an analogy with two resistances in series. In the saturation, the mobility of free carriers is characterised by μ_G that decreases with the temperature. Before saturation, μ_{eff} is the main factor and it increases with the temperature. At low temperatures or with high trap concentration, or at low voltage μ_{eff} is the main scattering factor.

In the reverse mode, a reverse bias causes an electric field that occurs mainly at the grain boundaries. At the grain boundaries there are three possible conduction mechanisms:

1. The generation of free carriers on both sides of the grain boundary at the depletion region that is usually much wider than the grain boundary itself.

2. Trap-to-trap tunnelling at grain boundaries, that occurs when the density of traps is high especially at lower temperatures;

3. Fowler-Nordheim effect at the grain boundary or conduction generated by field enhanced thermal generation observed in poly-Si diodes.

Brief Notes on Models for poly-Si TFT. There are mainly three types of models: models based on the physics related to individual grain boundaries [19], models supported on current-voltage characteristics [20] and models built on empirical approaches to manufactured and tested devices [21].

Some models started with expressions for poly-Si characteristics like the height of the energy barrier at the grain boundaries and later incorporated in current-voltage equations. Several empirical results based on long-channel devices (above 6 µm) were added for accurate simulation values. Later versions include short-channel effects (like the Kink effect), the field-effect mobility in moderate inversion, and subthreshold currents. Most recent models for TFTs based on empirical measurements include equations for the reverse-bias leakage current of the drain junction and the subthreshold leakage current[22], drain induced barrier lowering, temperature effects[23] and mobility degradation at high voltage bias. To ensure SPICE convergence, most models use the same set of equations to describe all regimes (subthreshold, above threshold, saturation and kink regimes) [24]. For the drain current, the unified model can be obtained by:

$$\frac{1}{I_d} = \frac{1}{I_{sub}} + \frac{1}{I_a}. \quad (2)$$

In equation (2), the drain current is the combination of currents in the sub threshold and above threshold regions. As mentioned before, the drift of carriers occurs

mainly above the threshold region, and diffusion of carriers occurs mainly at the subthreshold region.

Air-Gap Thin Film Transistors (AGTFTs)

Manufacture of AGTFTs. Air-gap thin film transistors (AGTFT) or suspended gate thin film transistors[7], are thin film transistors with a gaseous gate dielectric. A glass substrate covered with an insulator film of Silicon Nitride (Si_3N_4) is used to deposit by LPCVD, a 350 nm poly-Si film. The film is then crystallized by SPC at 600º C for 12 hours. The gate insulator film is then deposited and etched for the definition of the active area. In some transistors a thin protective layer silicon nitride is deposited, in others the choice for protective material goes to silicon oxide and the rest of the transistors were fabricated without any protective film over the active area. A temporary support film is then deposited, before the aluminium structural film, which will define the gate and the contacts for the drain and the source. The excess material is removed by etching agents.

Characterization of AGTFTs. The air-gap thin film transistor is characterized by the analysis of its regions of operation, the $I_{ds} = f\ (V_{gs})$ transfer characteristic, the $I_{ds} = f\ (V_{ds})$ output characteristic, and the values of four standard parameters used to compare these types of transistors with thin film transistors with a silicon oxide insulator. These parameters are:

- Threshold voltage (V_T);
- Carrier mobility (μ);
- Voltage slope (S);
- I_{ON}/I_{OFF} ratio.

The operation regions for the air-gap thin film transistor are analogous to the operation regions of the field effect transistor. The basic working principle of the air-gap thin film transistor is not different from other field effect transistors, in spite of the different dielectric material. The threshold voltage is related to the charge density in the channel and with the interface channel-dielectric on the forbidden energy states and the capacitance between the gate and the channel per surface unit. The mobility depends on the TFT dimensions and also on the capacitance between the gate and the channel per surface unit.

Test Results for the AGTFTs. Three types of air-gap thin film transistors were studied in environment controlled conditions. The first type has no protection on the active area, while the other two have the channel protected by a layer of 50 nm of silicon oxide or by a layer of 15 nm of silicon nitride, respectively. Some of the results can be summarized in the following statements:

There was a degradation of the characterization parameters of the air-gap thin film transistor for neutral gases (such as nitrogen and oxygen). For those gases the threshold voltage and the voltage slope increased.

There was an improvement of the characterization parameters of the air-gap thin film transistor for increasing levels of humidity. The AGTFT presented a linear variation of the drain current with the humidity concentration of 10^6 between 20% of humidity ratio and 60% humidity ratio.

The transistors with protected active area presented smaller sensitivity, but higher precision. The return time of the air-gap thin film transistor is in the order of seconds, increasing with the temperature.

Conclusions

The main development vectors in large area electronics for gas sensors were presented by focusing on thin-film transistor sensors. The structure, materials and manufacturing methods and parameters, and how they influence the electrical parameters of the transistor and in turn the sensor specifications were analysed. Thin-film transistor breakthroughs reported mainly in sensitivity, linearity and dynamic response promise new fields of applications for the sensors developed with these technologies. There are also some challenges on the power consumption and stability specifications that needed to be addressed. Some questions on sensors based on air-gap thin-film transistors are still unanswered and hamper the effort to design a commercial usable device.

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The development of large area electronics gas sensors is reported, by focusing on the breakthroughs of thin-film transistor technologies. Thin-film transistors are analysed in terms of structure, their manufacturing materials and their properties. Deposition, crystallization and post-treatment methods and how the parameters of those methods affect the electrical properties of the thin-film transistor and in turn, the performance of the thin-film sensor, are also reported. A brief analysis on the structure, manufacture and test results of air-gap thin-film transistors, that showed high sensitivity values for certain gases, concludes this paper. Ill. 2, bibl. 24 (in English; summaries in English, Russian and Lithuanian).

М. С. Перейра, М. Е. Мартинс, О. Бонауд. Датчики газа на основе тонких пленок: материалы, технологии изготовления и результаты испытаний // Электроника и электротехника. – Каунас: Технология, 2009. – № 1(89). – С. 39–44.

Показано развитие крупноразмерных электронных датчиков газа. Большое внимание уделяется новейшим достижениям технологий транзисторов на основе тонких пленок. Транзисторы на основе тонких пленок анализируются с точки зрения их структуры, производственных материалов и их свойств. Анализируются: смещение, кристаллизация и методы постобработки, а также как особенности тех методов определяют электрические свойства транзисторов на основе тонких пленок. От этих особенностей зависят показатели датчиков указанного типа. Прведены: короткий анализ структуры, особенности изготовления и результаты испытаний транзисторов с воздушным диэлектриком. Результаты показали высокую чувствительность указанных датчиков к газам некоторых типов. Ил. 2, библ. 24 (на английском языке; рефераты на английском, русском и литовском яз.).

M. C. Pereira, M. J. Martins, O. Bonnaud. Plonų plėvelių tranzistoriniai dujų jutikliai: medžiagos, gamybos technologijos ir bandymų rezultatai // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2009. – Nr. 1(89). – P. 39–44.

Pristatomas didelio ploto elektroninių dujų jutiklių projektavimas. Daugiau dėmesio skiriama plonų plėvelių tranzistorių technologijoms. Analizuojama plonų plėvelių tranzistorių struktūra, gamybos metu naudojamos medžiagos ir jų savybės. Taip pat apžvelgiami nusodinimo, kristalizavimo ir pogamybinio apdorojimo metodai, taip pat šių metodų parametrai lemia elektrines plonų plėvelių tranzistorių savybes. Nuo šių savybių priklauso plonos plėvelės jutiklio efektyvumas. Trumpai analizuojama plonų plėvelių tranzistorių su dujiniu dielektriku struktūra, gamyba ir bandymų rezultatai. Parodyta, jog tokie tranzistoriai yra ypač jautrūs tam tikrų rūšių dujoms. Il. 2, bibl. 24 (anglų kalba; santraukos anglų, rusų ir lietuvių k.).