

## Interpolator in a Sigma-Delta Digital-to-Analog Converter

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### Introduction

Notwithstanding the fact that in special cases in Sigma-Delta ( $\Sigma\Delta$ ) digital-to-analog converters (DAC) it is possible to manage without an interpolator at all, yet they are necessary. That is also witnessed by the fact that interpolator often takes more chip space than the very  $\Sigma\Delta$  modulator [1, 2, 3]. Sometimes a question arises: „how important is this interpolator taking so much chip space or FPGA resources?“ The other, even a more important question follows: „when and where it is possible to save?“ This article is intended for the analysis of these questions.

The basis of this article consists of expanded experiments from [2] explaining in more detail. The more applicable interpolator structures were suggested and analyzed. The experimental research, was presented, ensures stopband attenuation  $> 66$  dB and  $> 99$  dB instead of the previous 49 dB.

### Interpolator's place in Sigma-Delta DACs

A Sigma-Delta DAC structure (Fig. 1) consists of an interpolation filter, a  $\Sigma\Delta$  modulator which, regarding a signal, works as a low frequency filter, whereas regarding quantization noise – as a high frequency filter, and a 1-bit (or n-bit) D/A converter (output key) whose output is being switched over between reference voltage (or current) magnitude. The signal received is being filtered by way of an output analog low frequency filter.

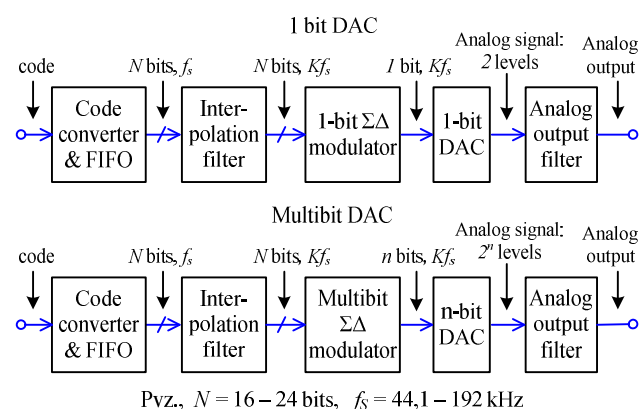


Fig. 1. Sigma-Delta D/A converter: one-bit and multibit

Interpolator is necessary in order to increase the sampling frequency and suppress all the additional images between the main band and  $OSR \cdot f_s$  (oversampling ratio multiplied by sampling frequency). This will improve the dynamic range of noise shaping loop (NSL) (in our case – of  $\Sigma\Delta$  modulator) and will reduce the requirements of the analog output filter.

On principle, it is possible to raise the sampling frequency up to  $OSR \cdot f_s$  at once and then carry out all the necessary filtrations. However in this case all the digital circuits must function at a high speed and will heat up more – will use more energy. Besides, digital activity will be active which will cause higher noise level; and finally, filters will have to be of higher order and more equipment resources will be necessary for this. So it is desirable to simultaneously raise the clock rate and filter, perform the major part of signal processing at low clock rates [3]. There are components in FPGA which can be time shared. The lower sampling speed is and the shorter the word is (length of sample in bits) comparing with the global clock rate, the more area resources the circuit needs. For this reason a consistent speed increase is more desirable.

### General structure of interpolator

The summarized most common structure of interpolator is provided in Fig. 2. Depending on the need, the number of stages can be larger or smaller.

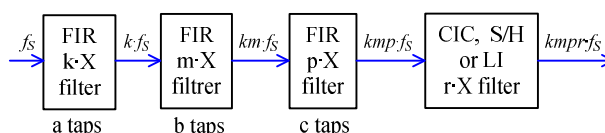


Fig. 2. Predominant structure of the interpolator

Every stage consists of interpolation low frequency filters. In the first steps the higher order traditional FIR filters dominate where an imparity  $a \geq b \geq c$  is valid. In the last step effective from the point of view of equipment resources, usually CIC (Cascaded Integrator-Comb), S/H (Sample and Hold) and LI (Linear interpolator) filters are used. Natural numbers  $k, m, p, r$  indicate interpolator factor of every step. Usually it is  $k \leq m \leq p \leq r$ . The general

interpolator factor is usually called oversampling ratio (OSR) and is equal to the product of interpolation factors of every step:  $OSR = k \cdot m \cdot p \cdot r$ .

#### 44 or even 43 non-zero taps

One of the possible interpolator realisations [2] consists of three stages where  $k = 2$ ,  $m = 4$ ,  $r = 8$  and  $OSR = 64$ ;  $a = 47$ ,  $b = 20$ , and in the last stage S/H circuit is used. Since in the above mentioned article interpolator transfer characteristic are given without the last S/H stage, talking about such structure, it will be called incomplete interpolator.

The authors of the above mentioned article tried quite well to reduce the resources used by interpolator. According to them, and what is proved by the repeated analysis of this article's authors, the characteristic of incomplete interpolator is as follows: stopband attenuation is 49 dB, passband ripple is 0,06 dB<sub>p-p</sub> (peak-to-peak, this is seen from the provided figure, and is not a amplitude value as written in the text – i.e. better that written), the cut-off frequency of passband is 19,4 kHz. In the first stage almost half of the filter coefficients are zeros and this means that only  $24 + 20 = 44$  coefficients not equal to zero are present in the interpolator. Having in mind that filters are symmetric, there are only 22 coefficients.

In order to reach such transfer characteristic synthesizing in MATLAB the multirate multistage filter by automatic regimen we get  $74 + 21 = 95$  (intermediate optimization) and  $70 + 11 = 81$  (advanced optimization) non-zero coefficient. These filters are also symmetric, so 48 and 41 different coefficients respectively will be received, what are almost twice more than authors from [2].

Not getting into more detail discussing if such transfer characteristic is sufficient, an inquisitive question arises „Is this a limit or it is possible to get even better results?“ The authors of this article succeeded in realizing an interpolator with four stages, where  $k = 2$ ,  $m = 2$ ,  $p = 2$ ,  $r = 8$  and  $OSR = 64$ ;  $a = 55$ ,  $b = 15$ ,  $c = 9$ , and in the last stage S/H circuit is also used.

In order to better compare, the main characteristic of incomplete interpolator is maintained not worse than the following [2]: passband ripple is  $< 0,06$  dB<sub>p-p</sub>, when the cut-off frequency of passband is 19,4 kHz, stopband attenuation is  $> 66$  dB (Fig. 3). The complete interpolator is built in the same way as [2] – after having used S/H circuit. However it is most amazing that more resources were not necessary for gaining 17 dB. Even contrarily – only  $29 + 9 + 5 = 43$  non-zero coefficients are present in the incomplete interpolator, i.e. even one less. The essence is an optimized structure where Halfband filters are used whose almost half of the coefficients are equal to zero. By the way, these filters are also symmetric, which means that there is almost half less of different coefficients.

Below comprehensive filter synthesizing parameters used in *Matlab fdatool* are provided.

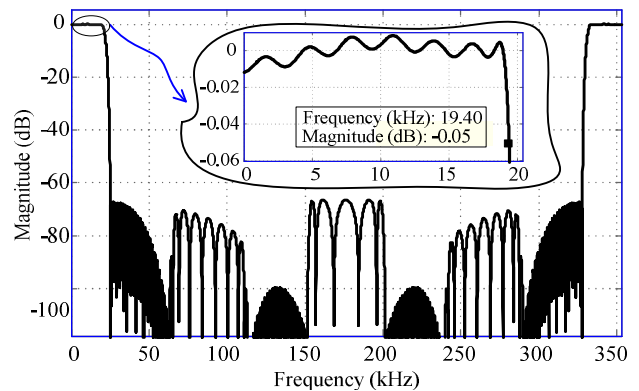
Common parameters: Structure: *Direct-Form FIR Polyphase Interpolator*; Responce Type: *Halfband*

*Lowpass*; Design Method: *Equiripple*; Density Factor: 500; Interpolation Factor: 2.

1<sup>st</sup>: Order: 54;  $F_s = 44,1 \cdot 2$  kHz ;  $F_{pass} = 19,03$  kHz .

2<sup>nd</sup>: Order: 14;  $F_s = 44,1 \cdot 4$  kHz ;  $F_{pass} = 23,5$  kHz .

3<sup>rd</sup>: Order: 8;  $F_s = 44,1 \cdot 8$  kHz ;  $F_{pass} = 21,0$  kHz .

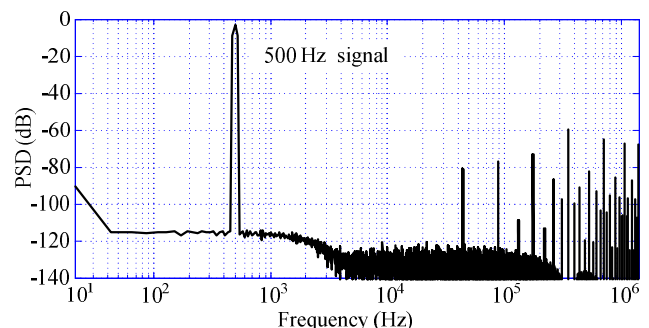


**Fig. 3.** Incomplete interpolator magnitude response

Two-channel interpolator was synthesized by Xilinx System Generator package, in Xilinx Spartan XC3S400 FPGA. Interpolator filters were realized using the structure of the distributed arithmetic (trying not to use Block RAM and dedicated equipment multipliers which can be useful for the remaining circuits). FPGA was clocked at 50 MHz frequency. The length of the input word was 18 bits. Interpolator was not optimized at low level what could reduce the used resources [4], because it already occupied quite less than [2]: 777 slices, 1312 slice Flip Flops, 894 4-input LUTs and 72 input/output blocks; 0 Block RAMs, 0 Embedded multipliers, 0 Tristate Buffers.

#### What more is important?

In the Fig. 7 [2] of the supporting article FFT spectrum of output at different input signals is provided. It is an important characteristic, however there was no use to stop 20 kHz: having extended it till  $F_s/2$ , what in our case is 1411,2 kHz, we would get more information. Such a characteristic when 500 Hz sine signal operates is provided in Fig. 4. FFT processed with  $2^{17}$  points, as in [2].



**Fig. 4.** Power spectrum density of complete interpolator output

The image in the frequency range up to 20 kHz is practically not changed, however at higher frequencies additional peaks are seen. The reason for this is explained by the amplitude transfer characteristic of complete interpolator (Fig. 5), which, most probably because of the

lack of space, is not provided in the above mentioned article. Their frequency response characteristic is practically identical to the given one, only suppressing between the „peaks“ appeared up to 17 dB or worse, because the last stages do not differ. In both cases the suppression of the complete interpolator pass band at 19,4 kHz does not exceed  $-0,1$  dB.

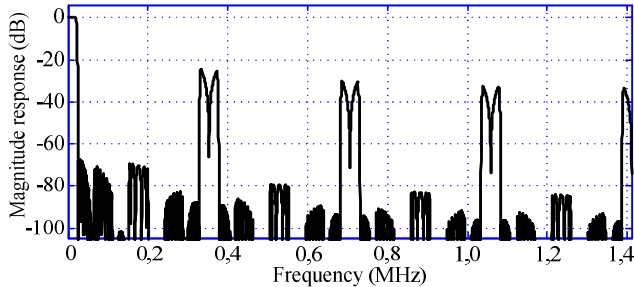


Fig. 5. Magnitude response of complete interpolator

### What interpolator is suitable as well?

A question arises looking at Fig. 5: „Where the designed interpolator may be suitable? To tell the truth, it depends for what purpose it is used, i.e. what circuits will follow it. If the characteristic of the following circuits is not precisely known, it is possible to design for the worst case as it was made in [4].

Let's take a certain situation when interpolator is used together with a Sigma-Delta modulator [4] whose signal and noise transfer functions (STF and NTF respectively) is such as indicated in Fig. 6.

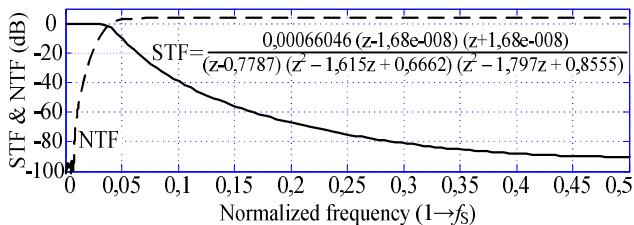


Fig. 6. Signal and noise transfer functions of  $\Sigma\Delta$  modulator

We assume that an analogue 3rd order Chebyshev filter is present in the modulator output (together with load [5]), passband edge frequency is 22 kHz with 0,5 dB of ripple in the passband. In this case not including the quantization noise by the modulator, we get such frequency characteristic of the whole system amplitude as indicated in Fig. 7. The power spectrum density (PSD) of system output when 500 Hz and 15 kHz sine signal is operating in the input is provided in Fig. 8. FFT processed with  $2^{17}$  points, as in [2].

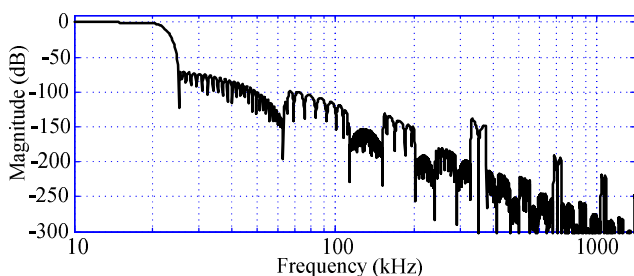


Fig. 7. Magnitude response of whole system

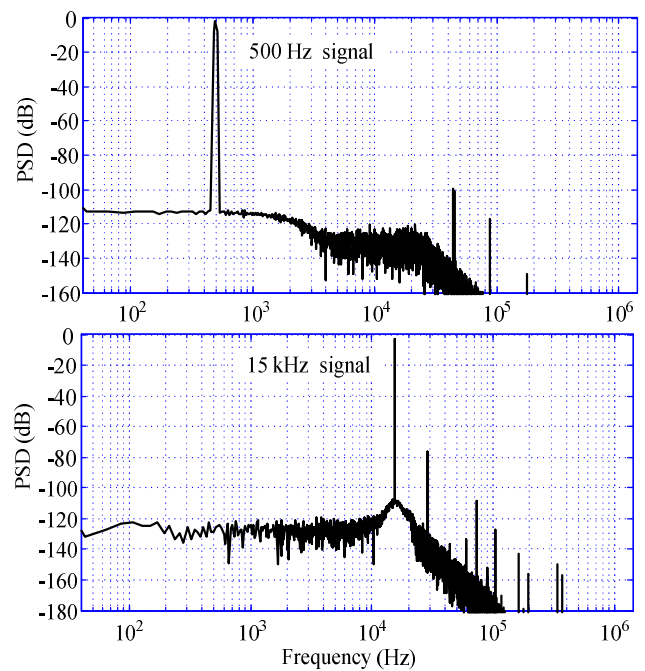


Fig. 8. PSD of whole system output without quantization noise

It can be seen from the latter figure that an output spectrum at 500 Hz sine signal is clean enough and interpolator's suitability does not cause any doubts. However after giving a 15 kHz signal, the suitability of the interpolator is questioned, because suppression level of frequency band 22 – 50 kHz is usually insufficient. Including the fact that so far not all Sigma-Delta modulators have such fast roll-off of STF, a conclusion can be made that the designed interpolator suits only a very limited circle of modulators. In this case the suitability of the reference interpolator, whose characteristic is 17 dB worse, for portable digital audio system (as written in [2]) is rather an exception than a rule.

Finally, knowing what follows after interpolator, it is possible to choose a very economic interpolator suiting only a certain system. One of the possible solutions for the mentioned system could be an interpolator with three stages, where  $k=2$ ,  $m=2$ ,  $r=16$  and  $OSR=64$ ;  $a=87$ ,  $b=15$  and CIC filter is used in the last stage (Differential delay = 1, Number of sections = 2). Only  $43+9=52$  non-zero coefficients are present in the incomplete interpolator. The output parameters of the first filter are identical to the previously designed only the filter order is increases and the second filter is left without changes. The amplitude frequency response of the system is provided in the Fig. 9.

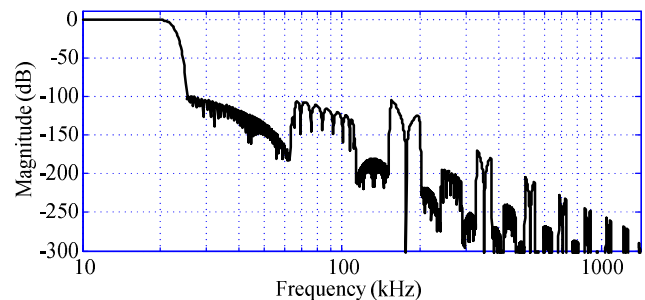


Fig. 9. Magnitude response of whole system with fitted filter

Synthesising the latter two channels filter in FPGA (at the same parameters as before), the filter requested: 761 slices, 1296 slice Flip Flops, 969 4-input LUTs and 72 input/output blocks; 0 Block RAMs, 0 Embedded multipliers, 0 Tristate Buffers. It means that it was needed even less resources than the previous filter!

Most probably the only drawback of the latter interpolator is that the pass band suppression at 19,4 kHz already reaches  $-0,35$  dB instead of the previous  $-0,1$  dB. However keeping in mind that the analogue output filter also impairs everything at 0,5 dB, it is really a worth "payment" for stopband attenuation  $> 99$  dB instead of the previous 66 dB (or 49 dB in the reference version of interpolator).

## Conclusions

1. Having changed the structure of incomplete interpolator and having optimized the stages, it was possible to improve the characteristic of amplitude frequency response even by 17 dB with less non-zero coefficients (43 instead of 44) and much less FPGA resources.

2. Having carried out the modelling of the full converter system (interpolator + modulator + output filter) it was defined that the amplitude transfer characteristic of the designed interpolator, with less non-zero coefficients and much less FPGA resources, unfortunately, suits only a very limited cycle of modulators.

3. One more economic version of 3-cascade with CIC filter interpolator was offered which suits better the above

mentioned system, ensures stopband attenuation  $> 99$  dB instead of the previous 66 dB or 49 dB.

4. It was shown, that modelling PSD of the full system, it is possible to identify places of the interpolator, where hardware resources could be saved, herewith reducing occupied chip area by converter. What is not always obviously analysing nodes separately.

## References

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## **V. Puidokas, A. J. Marcinkevičius. Interpolator in a Sigma-Delta Digital-to-Analog Converter // Electronics and Electrical Engineering. – Kaunas: Technologija, 2009. – No. 2(90). – P. 99–102.**

The place of interpolator in Sigma-Delta DACs was briefly discussed. The summarized structure of the most common interpolators was provided. The more applicable interpolators' structures were suggested and analyzed in comparison with [2]. Having changed the structure of incomplete interpolator and having optimized the stages, it was possible to improve the characteristic of amplitude frequency response even by 17 dB with less non-zero coefficients and much less FPGA resources. Experimental research of the full converter system (interpolator + modulator + output filter) it was defined that the designed interpolator (including 17 dB gaining) suits only a very limited cycle of modulators. Another version of interpolator was offered for the system, ensuring the suppression of the additional frequency band in the whole system above 99 dB instead of the previous 66 dB (or 49 dB in the supporting version of interpolator). Ill. 9, bibl. 5 (in English; summaries in English, Russian and Lithuanian).

## **V. Пуйдокас, А. Й. Марцинкявичюс. Интерполятор в Сигма – Делта ЦАП // Электроника и электротехника. – Каунас: Технология, 2009. – № 2(90). – С. 99–102.**

Обосновано место интерполятора в Сигма – Делта ЦАП. Предложена обобщенная структурная схема интерполятора. Приведены результаты исследования структур более совершенных интерполяторов, по сравнению с структурой [2]. Оптимизирована структура неполного интерполятора: с меньшим количеством ненулевых коэффициентов и на много меньшим ПЛИС ресурсов, позволило улучшить его амплитудную передаточную характеристику на 17 дБ. Однако, экспериментальное исследование полной системы преобразователя (интерполятор + модулятор + выходной фильтр) показало ограниченное применение интерполятора в Сигма – Делта ЦАП. Для системы разработана схема трехступенчатого интерполятора, которая обеспечивает подавление ненужной полосы частот более 99 дБ вместо предыдущих 66 дБ (или 49 дБ в начальной версии интерполятора). Ил. 9, библи. 5 (на английском языке; рефераты на английском, русском и литовском яз.).

## **V. Puidokas, A. J. Marcinkevičius. Interpoliatorius Sigma-Delta skaitmeniniame-analoginiame keitiklyje // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2009. – Nr. 2(90). – P. 99–102.**

Trumpai aptarta interpoliatoriaus vieta Sigma-Delta SAK'uose. Pateikta apibendrinta interpoliatoriaus struktūrinė schema. Pasiūlytos ir išanalizuotos tinkamesnės interpoliatorių struktūros, palyginti su [2]. Pakeitus nepilnojo interpoliatoriaus struktūrą ir optimizavus pakopas, sugebėta, naudojant mažiau nenulinių koeficientų ir gerokai mažiau LPL matricos išteklių, amplitudės perdavimo charakteristiką pagerinti net 17 dB. Visos keitiklio sistemos (interpoliatorius + moduliatorius + išėjimo filtras) eksperimentinis tyrimas parodė, jog suprojektuotas interpoliatorius (įskaitant 17 dB laimėjimą) tinka tik ribotam moduliatorių ratui. Sistemai pasiūlytas dar vienas interpoliatoriaus variantas, užtikrinantis visos sistemos pašalinės dažnių juostos slopinimą, viršijantį 99 dB, vietoj buvusių 66 dB (arba 49 dB atraminiam interpoliatoriaus variante). Il. 9, bibl. 5 (anglų kalba; santraukos anglų, rusų ir lietuvių k.).

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