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The Aspects of Non-standard CMOS Integrated Circuits Layout Design

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Introduction

Now the design process of integral circuits is divided essentially into two different trends. The first is when large computer producing companies design and provide the circuits of several millions transistors increasing the density of elements and reducing the width of the conjunctive line. Microsoft Company already presents processors with 0,18 μm width copper conjunctive lines. A lot of one-type circuits are produced [1].

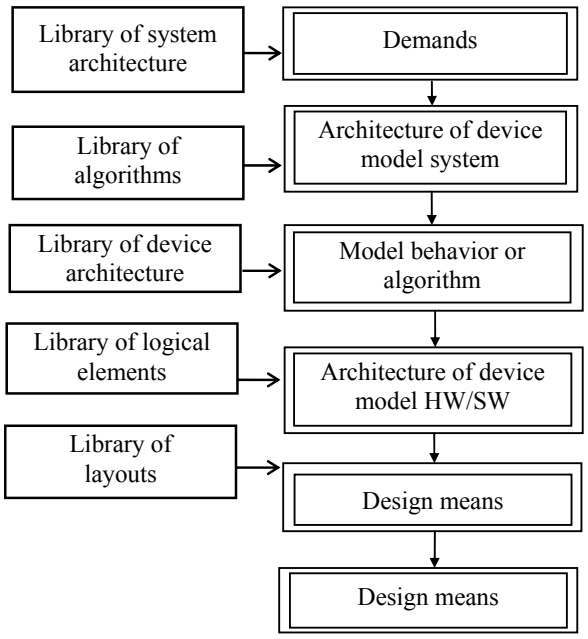

Fig.1. Methodic of IC design by new design systems

Design of nowadays circuits is reasoned by the application of standard library from the beginning to the end. The strategy of electronic design of structures using standard library elements is shown in Fig.1.[2].

All necessary information to the successful synthesis equipment operation is accumulated in libraries of technologies. Those libraries involve not only the descriptions of standard library logical function elements but also the area of those components, time parameters (signal front delay time), output ramification limitations and delay control processes. Symbolic standard element layouts are given in the libraries also.

In this case topology of library elements corresponding particular technological process and minimal in this technology used line width (minimal opening that permits to obtain by this technology) is established beforehand designing the element and stored in the library.

Symbols of those layouts are given composing general IC layouts. Symbolic cell layout has the area of real layout and the possible contact with the other cells and feeding and earth contact places are shown there [4].

The second trend is of comparatively small size, i.e. about 4 – 10 thousand transistors, the production of application specific integrated circuits (ASIC) according to the needs of the customer.

The design aspects of those specialized circuits would be analyzed in this paper. Specialized IC of small series are designed as synthesizing layout automatically as interactively.

Libraries of basic logical elements are made in the newest electronic circuits of design systems (Cadence, Synopsis). Usually the content of the library and its size reflects one of the possible technologies, such as Mietec 1,0 μm, ES2 1 μm, ES2n 0,7 μm, Matra MHS BICMOS 0,8 μm, CMOS 0,35 μm, UMC CMOS 0,25 μm; the minimal line width typical to particular library is given besides the name.

Components in the library are presented by symbolic or schematic picture and by layout symbol pictures. The pictures of all technological layers are designed for those components.

So, it is enough to make the layout of established circuit in the symbol level for the designers of complicated integrated circuits. The producers of integral circuits reproduce the entire layout and its segmentation by the layers using the same libraries.

Otherwise, using standard component libraries the area of cell layout is much more bigger than those of the same elements composing them interactively, besides, the parameters of those elements are average.

The task of the given work is to create and examine the aspects of non-standard cells design and connection into automatically generated logical circuit layout.

Non-standard cells are designed in the environment of Mietec 1,0 μm technology where layout is created separately forming the sphere of every transistor separately. So the non-standard structures of proper power and speed are designed.

The main problems in design process are [3-7]:
a) the introduction of non-standard cell layout into automatically synthesized general scheme layout;
b) the operation design of the circuit with analogue and digital elements.

The process of the non-standard transistor level cell design:

- To create the cell circuit in transistor level used for insertion;
- To design the corrective layout Compact image of the cell;
- To perform the control of geometric parameters (DRC analysis);
- To perform the search of electric errors of layout (ERC analysis);
- To design the detailed layout image Extract;
- To perform LVS analysis when the electric circuit and layout picture are compared;
- To verify the operation of the circuit by the programs cdsSpice or Spectre evaluating the parasitical parameters of layout;
- To load standard input, output, and feeding cells to the layout of designed cell;
- To compose the summarized cell-symbol of layout;
- To verify the operation of the circuit by the program Spectre-Verilog.

The non-standard cells with the different symbolic image and of bigger power and bigger resistance to the perturbations are introduced without any problems into the symbolic layout of c17_i89 of international example (Fig.2).

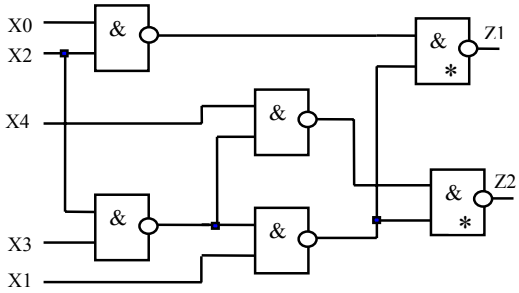

Fig.2. The logical circuit c17_i89 of standard international experimental example was chosen for the design, the star marks the changeable elements

As non-standard cell layout is designed in the level of transistors, in design system they are treated as circuits of analogue elements with the remained layout parts treated as digital circuit. The mixed simulation must be applied for verification of such combined circuit work. In this case, input signal collections are composed for the simulation of the part of logical circuit (STL files).

The capacity of conductive lines and isolation diodes are found from layout and given in the Table 1, whe "Inet" means the name of the line and the number shows its electrical capacity when the multiplier is 10^{-18} F.

The simulation of mixed analogical and digital circuits

The Analog Artist package including the modeling programs such as SpectreVerilog, cdsSpiceVerilog and SpectreSVerilog, HSpice are used for the simulation of mixed analogical and digital circuits. The complicated signal simulation environment Analog Artist allows to edit, simulate and analyze circuits composed from analogical and digital components. The environment of mixed signal simulation is very similar to the simulation and analysis.

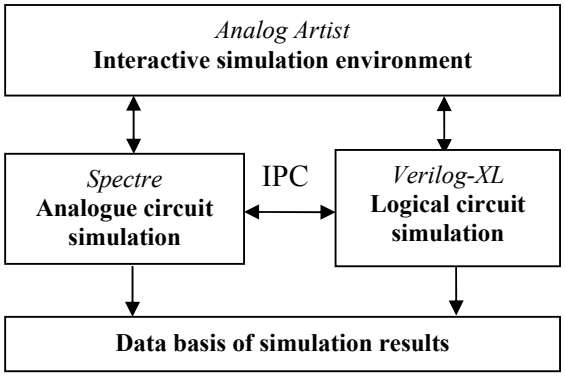

Fig.3. Modeling programs of mixed circuits

The biggest part of the work associated with the analysis of digital circuit parts is produced there. The same menu and the same sequence of procedures are used for the mixed (analogue and digital) circuits and for analogue circuits also. Most of mixed signal commands have extra materials for digital files, diagrams and so on.

Analog Artist mixed signal simulation environment uses such programs (Fig. 3):

- Spectre, cdsSpice, or HSpice program for the simulation of analogue circuits;
- Verilog-XL program for the simulation of digital circuits.

Interactive environment is used for the simulation. Both programs contacts the multiprocession system communication (IPC) working in Unix environment. This allows starting two programs in different work stations. IPC functions are controlled automatically. Programs sent calculated output signals to the data basis of simulation results.

The preparation to simulate mixed signals differs from the preparation to the analogue simulation in those parameters:

- Only analogue circuit simulation program works if the circuit is composed from analogue components;
- The circuit must be divided into analogue and digital parts before the simulation of the mixed signal circuit; the portrait of those parts allow to find the errors;
- It is very simple to change the simulation environment and to activate the process as simulating analogical as using mixed signal commands and materials;
- Program separately creates analogue and digital circuit lists (Netlist). The collections of input signals are given in the list of digital circuit (STL files). Those lists also include shift elements that are used for the connection of analogue and digital parts of the device.

This is analogue and digital (A2D), and digital and analogue (D2A) shift models (Fig. 4);

- Shift elements must have data stream direction.

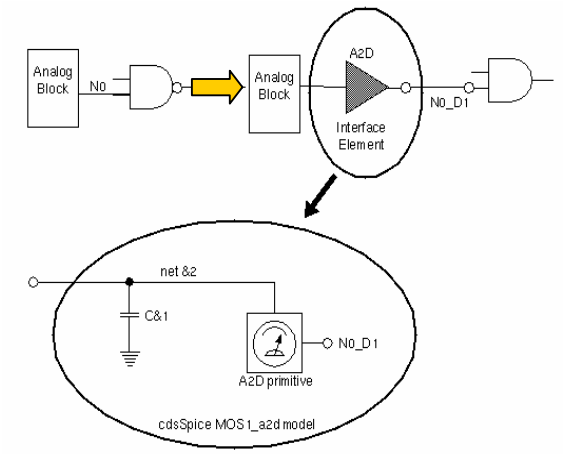

Fig. 4. The insertion and inner structure of shift element A2D [4]

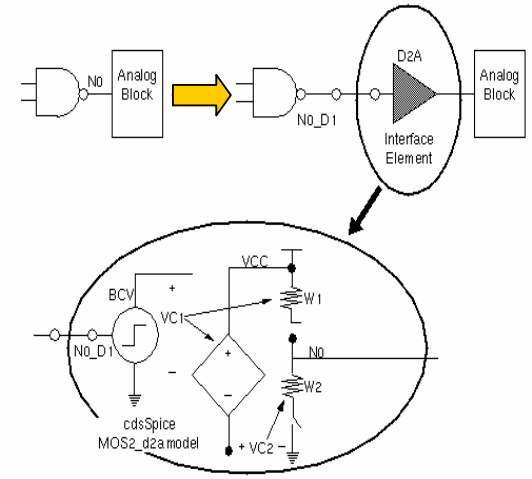

Fig. 5. D2A [2]

The description and insertion of D2A of shift element D2A is shown in Fig. 5. D2A model insertion into shift circuit is shown in the upper part. The model D2A used by the simulating program is shown in the upper part of the figure Fig. 6.

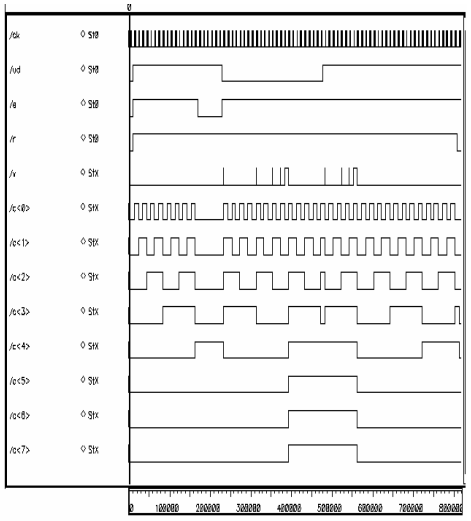

Fig. 6. The running time diagrams of circuit udc8

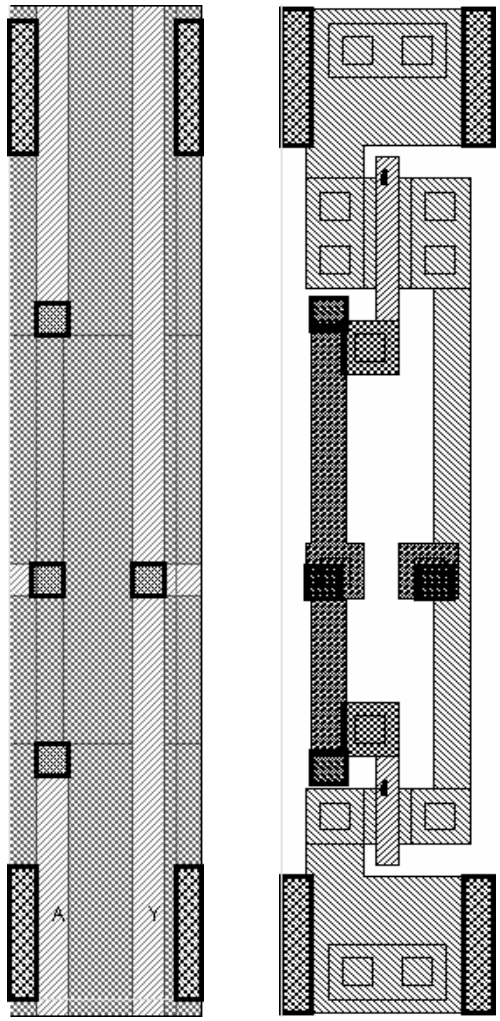

Fig. 7. Circuits layouts, NAND logical and transistor level layouts are given there.

Conclusions

1. The composed non-standard cell design process allowed the successful creation of original cells (NAND, D-trigger and Mux2) in the environment of Mietec technology (Fig. 7).
2. The created cell layouts of various sizes were successfully included into logical circuits (c17_i89, Udc8).
3. The simulation type of mixed analogue and digital layout parts was analyzed and simulation process succession was composed. The dynamical characteristics of designed IC layouts were analyzed using mixed SpectreVerilog simulation type.
4. The composed design methodic of non-standard integral circuits allows designing and verification of the desirable size analogue and logical circuits layouts.
5. The obtained results showed that original non-standard circuits could be included into layout of typical circuit. So, it can be expected in such a way to load any one's made original transistor level circuit that is not obtained in standard libraries.

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R. Benisevičiūtė. Nestandartinių KMOP integrinių schemų topologijos projektavimo aspektai // Elektronika ir elektrotechnika. - Kaunas: Technologija, 2005. – Nr .2 (58). – P.43–46.

Naujosios mikroschemų gamybos tendencijos sąlygojo ir naujų projektavimo metodikų atsiradimą. Viena iš galimų krypčių – technologijos, kurioms standartizuotas minimalus linijos plotis. Nagrinėjamos nestandartinių schemos ląstelių projektavimo ir įterpimo į bendrąją integrinės schemos topologiją galimybės ir metodika. Kadangi standartinių schemų topologijos pateikiamos simbolių lygiu, modeliavimo proceso metu šios ląstelės nagrinėjamos kaip loginės schemos. Nestandartinės schemos ląstelės projektuojamos tranzistorių lygiu, todėl jos traktuojamos kaip analoginės schemos. Integrinės schemos su įterptomis nestandartinėmis ląstelėmis modeliuojamos mišriuoju analoginiu ir skaitmeniniu būdu. Sudaryta nestandartinių ląstelių įterpimo į bendrąją simbolinę topologiją ir mišraus analoginių ir skaitmeninių schemų modeliavimo metodika. Il. 7, bibl. 7 (anglų kalba; santraukos lietuvių, anglų ir rusų k.).

R. Benisevičiūtė. The Aspects of Non-standard CMOS Integrated Circuits Layout Design // Electronics and Electrical Engineering. – Kaunas: Technologija, 2005. – No.2 (58). – P.43–46.

The new tendencies of circuit fabrication conditioned the investigation of new design methods. The technology with standardised minimal line width is one from such trends. The possibilities and methodics of design of non-standard cells are presented in the article. The possibilities of insert of non-standard cells layout into common integrated circuit layout are investigated also. The cell layouts from the standard library are interpreted as gates level circuit, because the layouts of those cells are given in the symbolic level. The non-standard cells are designed in transistor level, so they are interpreted as analogous circuits. The method of simulation of circuits layout with inserted non-standard cells on mixed analogue and logical level is researched. Ill. 7, bibl. 7 (in English; summaries in Lithuanian, English, Russian).

Р.Бенисявичюте. Аспекты проектирования топологии нестандартных КМОП схем // Электроника и электротехника – Каунас: Технология, 2005. – № 2(58). – С. 43–46.

Новые тенденции в производстве микросхем меняют методы проектирования и дальнейшего развития интегральных схем. Стандартизируется минимальная ширина линии. Рассматриваются возможности объединения топологических ячеек.

Создана методика внедрения нестандартных ячеек в логические схемы. Так как рассматриваются нестандартные ячейки топологии в симболном виде моделирование происходит на логическом уровне. Нестандартные ячейки схемы проектируются также на уровне транзисторных схем. Здесь они трактуются как аналоговые схемы. Интегральные схемы с внедренными нестандартными ячейками моделируются как чифровые и аналоговые в одно и тоже время. Ил. 7, библ. 7 (на английском языке; рефераты на литовском, английском и русском языке).