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Simulation of the Integrated Signal Folding Circuit with P–Spice

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Introduction

Modern analog–to–digital converters (ADC) have to meet numerous contradictory requirements. They are: high speed, precision, number of bits, small number of components, low power consumption, small area in the chip, low price and high reliability. To meet these requirements, the ADC architecture must be constantly improved.

In literature [1] the theory of folding circuits is analyzed but the simulation results of real circuits are not presented. In literature [2–5] there is no circuit quality quantitative evaluation how parameters depend on the delay time in the circuit.

Aim of the work

The first aim is: to show, that theory, created in [1], is working in practical cases.

The second aim is: to choose circuits and to refine them, then to choose models of transistors, the nominals of components, to make analysis of created circuits, and to verify theoretical conclusions that where made earlier [1], and to estimate the limitary parameters of the signal folding circuits.

Simulation of dynamic characteristics of the signal folding circuit (SFC)

In this paper we will perform simulation of the circuit dynamic characteristics of the signal folding according to voltages with the P–Spice package. For the circuit simulation we will use improved models of the 0,5 μm bipolar transistor technology. The structure of the simulated system is presented in Fig. 1.

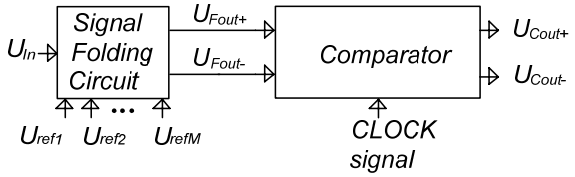

Fig. 1. Structure of the simulated system

In parallel converters the number K of comparators as well as the number of components in the chip depend on the number N of bipolar bits according to the equation $K = 2^N$. The use of the folding circuit allows significant reduction of the number of comparators in the converter [1, 2]. The main parameter of the folding circuit is the folding coefficient which is calculated by equation [1]:

$$M_{\max} = \left[4\pi f_{\max} \tau \ln\left(\frac{\pi f_{\max} \tau}{e} \cdot 2^N - 1 \right) \right]^{-1} - 1; \qquad (1)$$

where M_{max} is the highest possible folding coefficient;

f_{max} is the largest frequency of the analog input signal spectrum;

N is the number of ADC bits;

τ is the input signal delay time of ADC.

This equation (1) is correct when $2^N h = A$, where h is the value of the least significant bit (LSB), V, and A is the full scale value.

In literature [1] it is determined that the optimal folding coefficient M can be 4 – 8. Therefore, in designing precise ADC, part of comparators has to be used without the signal folding circuit.

For the simulation of characteristics of the SFC and the comparator we chose basic comparator and folding circuits referring to literature [2]. The simulated circuits are presented in Figs. 2 and 3.

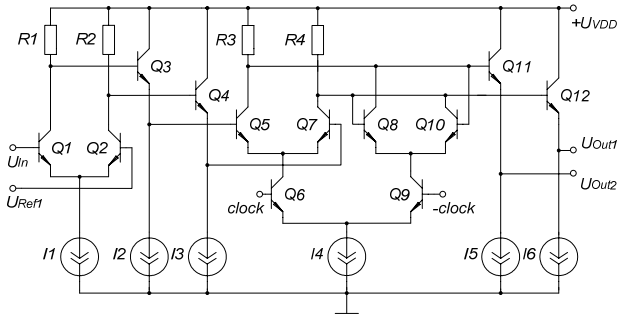

Fig. 2. Circuit of the simulated comparator

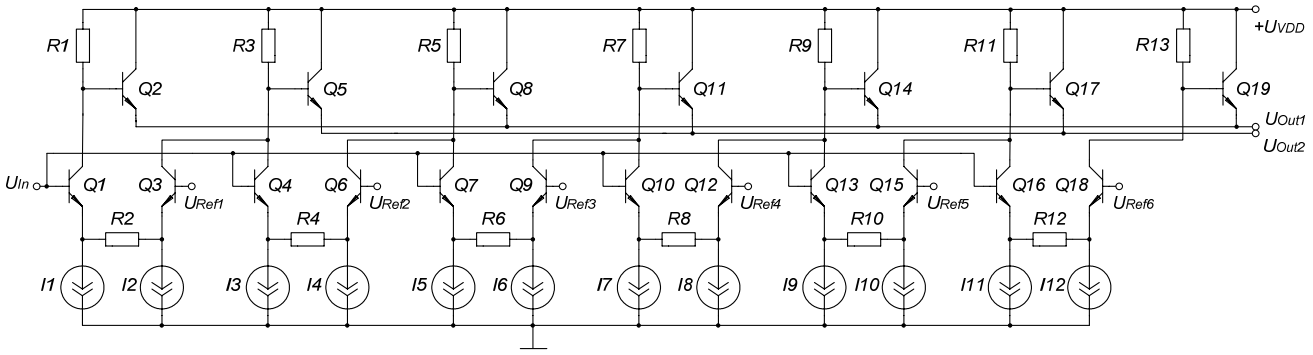

Fig. 3. Circuit implementing the signal folding when $M = 6$

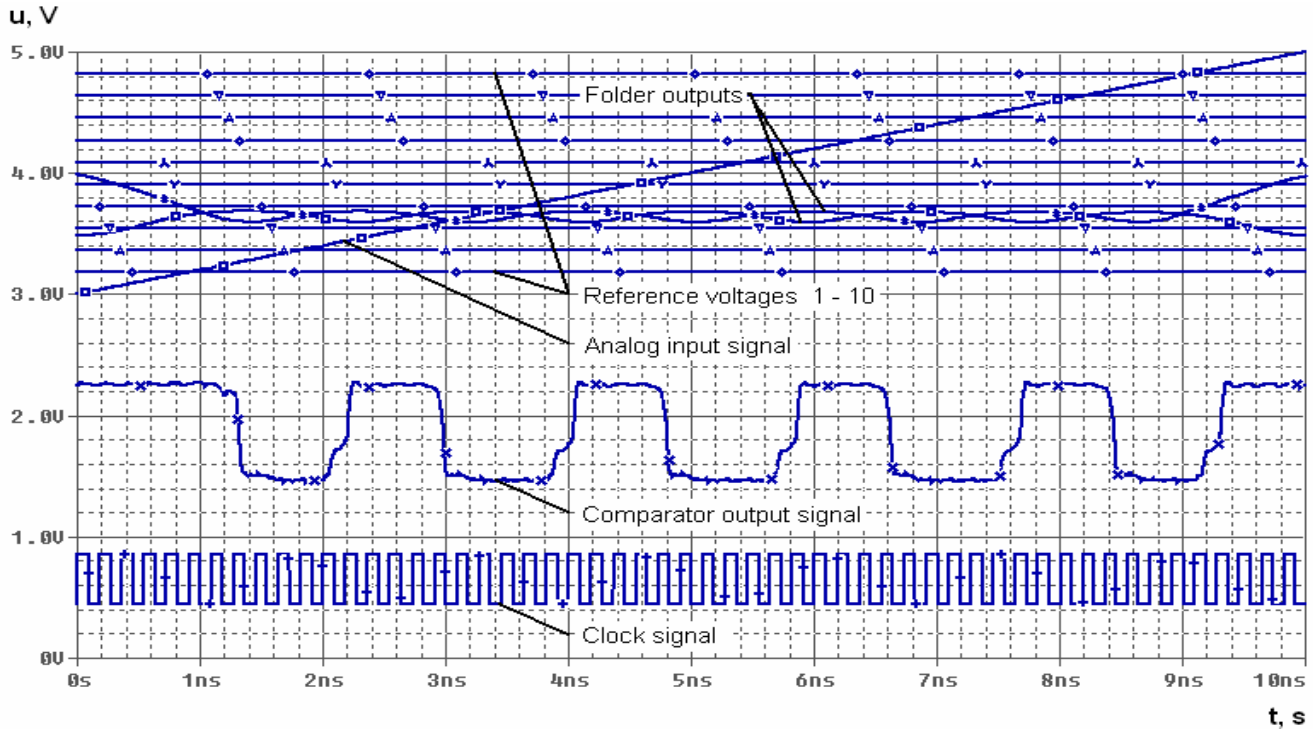

Fig. 4. Time diagrams of the circuit implementing the signal folding when $M = 10$

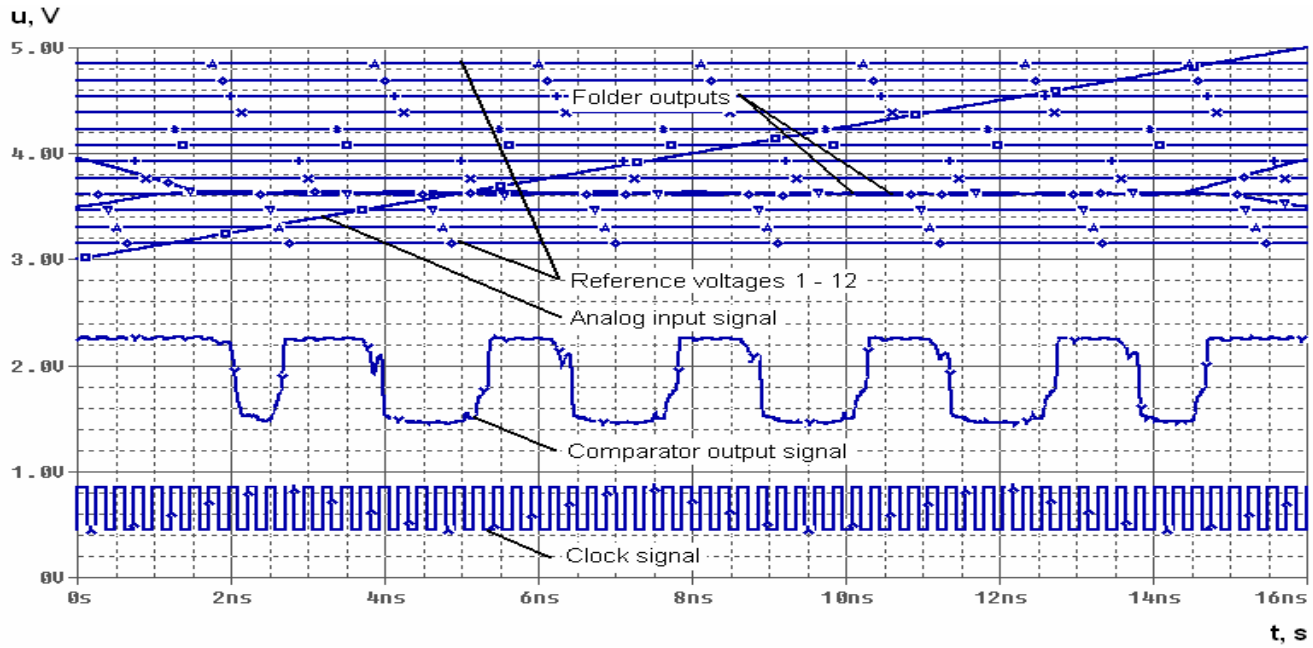

Fig. 5. Time diagrams of the circuit implementing the signal folding when $M = 12$

Analysis of simulation results

Signals obtained by simulating circuits when M = 10 and 12 are shown in Figs. 4 – 5. The following signals are shown: the analog input voltage, the folding circuit reference voltages, folding circuit output voltages, the comparator control signal and the comparator output signal. For clarity, the „Clock“ signal is presented of the reduced amplitude and shifted on the voltage axis.

Comparator output signal is without any intense distortions (Fig. 4). In Fig. 5, comparator output signal is quite worse, especially on the left and right sides. It means, that the SFC works well until the signal folding factor $M \leq$ 10.

From the Fig. 4, 5, and other simulations results, that are not presented in this paper, we measured some practical dependences of M, and presented them in figures 6 – 8.

From Fig. 6 we see that when M increases, the analog signal variation speed must be decreased in order to have still working circuitry. In Fig. 7 we see, that the required signal sensitivity Δu depends on M, and rapidly decreasing, what means, that it needs more sensitive comparators. In Fig. 8 we see, that the circuit driving speed f_{CLK} also decreases, but this is associated with input signal frequency, and signal variation speed.

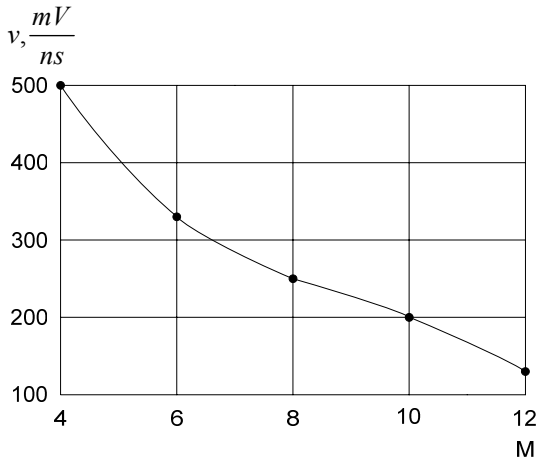

Fig. 6. Experimental dependence of the analog signal variation speed v, on the folding coefficient M

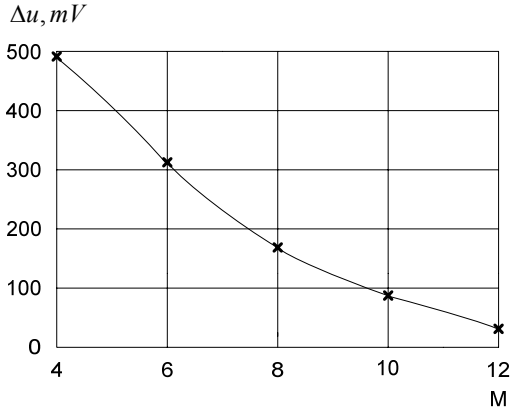

Fig. 7. Experimental dependence of the required comparator sensitivity Δu on the folding coefficient M

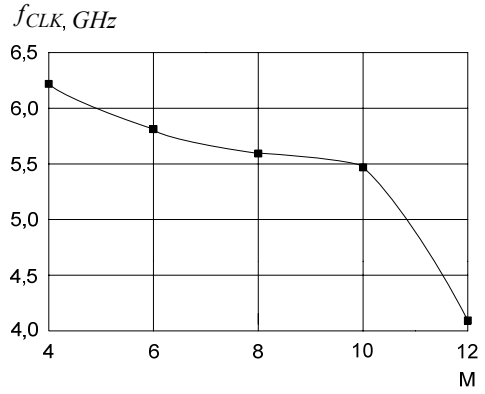

Fig. 8. Experimental dependence of the circuit driving speed f_{CLK} on the folding coefficient M

With the further attempt to increase M, the circuit missed the codes. It has been determined that codes were missed due to nonlinearity of the transistor volt–ampere characteristics on the edges of these characteristics.

It is seen that with the M increase the voltage difference Δu decreases. The highest allowable frequency of the analog input signal spectrum decreases also. The comparator driving speed f_{CLK} during simulation was related to the signal frequency. We also see that the parameters degenerate nonlinearly – a sudden worsening is observed between M = 10 and M = 12. Therefore, it is recommended not to use M > (8 – 10). And to use other circuitry solutions to minimize number of components.

In order to even more reduce the number of the circuit components, the signal interpolation, the theory of which is described in [6], can be applied. Another way is to use the cascade folding, i.e. using rather small M = 4, to restore the signal amplitude and to have several such cascades. In literature [3 – 5] up to 3 cascades can be found. Alongside with interpolation such solutions would allow reduction of the number of comparators in converters.

By increasing M, the output signal amplitude after folding decreases approximately M times. Since both positive and negative output signals are applied to the comparator after folding, this allows eliminating the influence of the irregular form folded signal and the amplitude. It is important that the amplitude difference should remain larger than the comparator sensitivity and the folded signals at their intersection points should be linear.

It has been determined, that created system operates properly only when M is in the range from 4 to 12. When M is large, system starts to miss codes and becomes unusable. It also has been observed that the best results for the circuit are when M = 4, 6, 8.

It has been determined that the optimal folding coefficient is 4 – 8. When M is larger, the requirements for the comparator sensitivity become more rigid and the signal processing speed becomes lower. E.g., when M = 8, the signal variation speed V can be 250 mV / ns, and the comparator sensitivity Δu of 175 mV is sufficient. When M = 12, V = 125 mV / ns, Δu must be not higher than 31,5 mV. By simulating the circuit when M > 12, it has been

determined that codes were missed. It is related to the nonlinearity of transistor volt–ampere characteristics on the edges of these characteristics. With the aim to increase $M > 12$, it is necessary to choose a sensitive comparator, to optimize the input signal dynamic range and to reduce the signal processing speed.

Other reasons which limit folding coefficient are:

- systems with larger folding coefficient require more attention for comparator sensitivity;
- input analog signal dynamical range;
- allowable clock frequency becomes lower.

Conclusions

The fast and precise ADCs, that consist of folding and comparator circuits, was simulated.

It has been determined, that created system operates properly only when M is in the range from 4 to 12. When $M > 12$, system starts to miss codes and becomes unusable.

It has been determined that the optimal folding coefficient is 4 – 8. When M is larger, the requirements for the comparator sensitivity become stricter and the signal processing speed becomes lower.

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The dynamical characteristics simulation results of the analog signal folding circuit for comparator ADCs were presented. The transient processes at differential folding and comparator stages switching points were simulated using improved models of real transistors and software P – Spice, when folding factor $M = 4, 6, 8, 10, 12$ and more, and when clock signal's frequencies are from 6,25 GHz to 4,1 GHz. It has been determined that the optimal folding coefficient is 4–8. When M is larger, the requirements for the comparator sensitivity become more rigid and the signal processing speed becomes lower. E.g., when $M = 8$, the signal variation speed v = 250 mV / ns, and the comparator sensitivity $\Delta u = 175$ mV. When $M = 12$, v = 125 mV / ns, $\Delta u \leq 31{,}5$ mV. By simulating the circuit when $M > 12$, it has been determined that codes were missed. It is related to the nonlinearity of transistor volt–ampere characteristics on the edges of these characteristics. With the aim to increase $M > 12$, it is necessary to improve sensitivity of comparator, to optimize the input signal dynamic range and to expand the linear part of folding amplifiers transistors volt–ampere characteristics. Ill. 8, bibl. 6 (in English; summaries in English, Russian and Lithuanian).

В. Ясонис, Д. Повиляускас, А. Марцинкявичюс. Моделирование интегральной схемы свёртки сигнала с помощью P–Spice // Электроника и электротехника. – Каунас: Технология, 2007. – № 1(73). – С. 37–40.

Приведены результаты моделирования динамических характеристик схемы свёртки аналогового сигнала применительно к компараторным АЦП. Используя усовершенствованные модели реальных транзисторов и пакет P – Spice, смоделированы переходные процессы в точках переключения дифференциальных каскадов свёртки и компаратора при коэффициенте свёртки $M = 4, 6, 8, 10, 12$ и больше, при частоте тактовых импульсов от 6,25 ГГц до 4,1 ГГц. Установлено, что оптимальный коэффициент свёртки равен 4–8. При большем M, значительно ужесточаются требования к чувствительности компаратора, уменьшается скорость дискретизации сигнала. При коэффициенте свёртки $M = 8$, скорость изменения сигнала v = 250 мВ / нс, а чувствительность компаратора $\Delta u = 175$ мВ. При $M = 12$, v = 125 мВ / нс, а $\Delta u \leq 31{,}5$ мВ. При моделировании схемы с $M > 12$ установлена нестабильность работы компаратора и потеря кодов. Это связано с нелинейностями вольтамперных характеристик транзисторов в краях этих характеристик. Желая увеличить $M > 12$, требуется улучшить чувствительность компаратора, оптимизировать динамический диапазон сигнала и расширить линейный участок волтамперных характеристик свёрточных усилителей. Ил. 8, библ. 6 (на английском языке; рефераты на английском, русском и литовском яз.).

V. Jasonis, D. Poviliauskas, A. Marcinkevičius. Signalo sąsūkos integrinės schemos modeliavimas naudojantis paketu P–Spice // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2007. – Nr. 1(73). – P. 37–40.

Pateikti analoginio signalo sąsūkos schemos, skirtos komparatoriniams ASK, dinaminių charakteristikų modeliavimo rezultatai. Pasinaudojant patobulintais realių tranzistorių modeliais ir paketu P – Spice, sumodeliuoti pereinamieji procesai diferencialinių sąsūkos ir komparatoriaus pakopų persijungimo taškuose, esant sąsūkos koeficientui $M = 4, 6, 8, 10, 12$ ir daugiau, kai taktinių impulsų dažniai yra nuo 6,25 GHz iki 4,1 GHz. Nustatyta, kad optimalus sąsūkos koeficientas yra 4–8. Didėjant M, smarkiai griežtėja reikalavimai komparatoriaus jautrumui, sumažėja signalo diskretizavimo greitis. Kai sąsūkos koeficientas $M = 8$, signalo kitimo greitis v = 250 mV/ns, o komparatoriaus jautris $\Delta u = 175$ mV. Kai $M = 12$, v = 125 mV / ns, o $\Delta u \leq 31{,}5$ mV. Modeliuojant schemą, kai $M > 12$ pastebėta, kad komparatorius veikia nestabiliai ir prarandami kodai. Tai susiję su tranzistorių voltamperinių charakteristikų netiesiškumu šių charakteristikų kraštuose. Siekiant padidinti $M > 12$, būtina pagerinti komparatoriaus jautrį, optimizuoti signalo dinaminį diapazoną ir išplėsti sąsūkos stiprintuvų voltamperinių charakteristikų tiesinę dalį. Il. 8., bibl. 6 (anglų kalba; santraukos anglų, rusų ir lietuvių k.).