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Broadband Optical Receiver IC on InP

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Introduction

On a worldwide basis, the means of information transmission is currently becoming more and more demanding. The amount of information to be transmitted through one channel is increasing rapidly to 10 Gbps (gigabits per second) and even 40 Gbps, which also increases information processing speed. The using of optical communication systems is probably the only solution for high-speed data transmission. Today's market requirements are mainly concentrated on 10 Gbps applications development. A great number of such devices have been designed recently. They differ in performance, technology and architecture in relation to technology, size, power dissipation, sensitivity and many more criteria. What is common, however, everyone seeks to design the perfect device, that is a tiny, very sensitive, highly-integrated device housing on the same chip (the so called 'die') all the circuits which are necessary for transmission and/or reception.

The device

The device studied in this work is Transimpedance Amplifier (hereafter TIA). It is the building block of optical communication system and lies at the receiver inception:

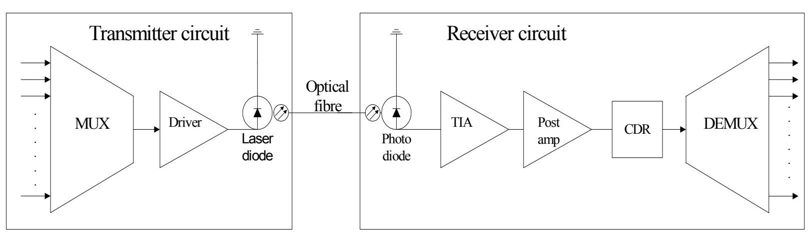


Fig. 1. Building blocks of optical communication system

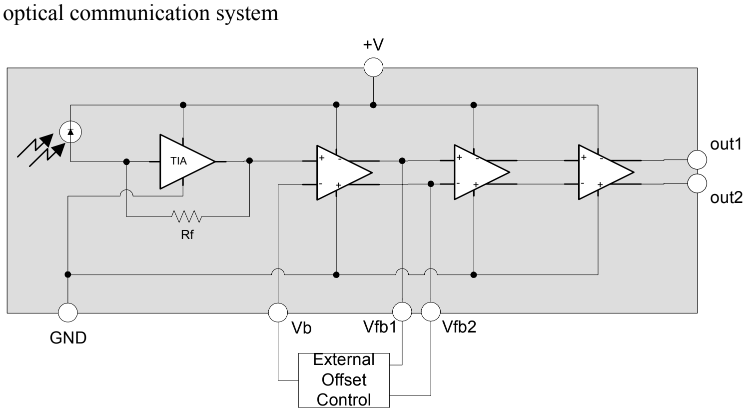


Fig. 2. Block diagram of TIA

Usually TIA has a single current input connected to photo-diode. Hence the main goal in the first stage of amplification is to correctly receive the signal, amplify it and feed it on to the next stage. This stage is generally called transimpedance amplifier, because as mentioned previously it converts the current signal to a voltage signal. An essential component of TIA is a feedback resistor, which enables to provide the necessary bias at the first transistor, to achieve required gain and reduce noise. As we can see from the review of similar devices one of the several feedback techniques could be chosen. However, a single TIA with two or three stages is incapable of providing the necessary gain. A so called post-amplifier is used to achieve the purpose.

A post-amplifier should preferably be differential. It provides the high gain and resistance to common-mode noise. But a serious problem at this stage is that TIA has only one single input and one output. This means that it is necessary to organize bias for both transistors (shoulders) of differential stage. One transistor is biased directly from TIA output. For the second one, several schematic solutions are possible.

For instance, the second exactly the same TIA stage could be arranged for biasing [1]. However, this approach has one drawback stemming from the imperfection of the technological process. Despite the fact that integrated circuit technology is a high-precision process it still cannot ensure an exact matching of components. This applies not only to developing technologies such as the one used in (InP) [2], but also to developed technologies like SiGe [3] or Si [1]. This mismatch amplifies by TIA. Thus even if two similar TIA's are used for differential amplifier biasing, it doesn't guarantee the exact bias voltage due to component mismatch.

Another way is to use the same signal for both two diff. stage inputs. The only difference here is that the voltage to the second input goes through RC-filter. In this case the average voltage of signal from TIA will be set at the second input. However, this solution requires high transistor Beta, or special schematic to compensate the impact of transistor Base current.

One more approach is to use a coupling capacitor between the TIA stage and the first differential stage. Bias can then be obtained simply by resistor divider or any other method. However, this way requires placing a high-value capacitor on the chip and that would be almost impossible to implement in InP technology - as well as in any other for that matter.

The simplest - but not the best - solution is to use the voltage divider on the chip and an external potentiometer [5, 6]. By adjusting external resistance we can achieve almost perfect bias matching for differential stage transistors. However, this approach is not efficient because in the event of change in the temperature or power supply voltage, the bias from the TIA stage changes too, and we would have to re-adjust the external resistances to achieve proper bias. This is highly undesirable in such type of devices.

A better solution in this case is to use feedback loop like in [6]. It is an integrated circuit set including an operational amplifier. This amplifier can be placed either on the chip or serve as an external component on printed circuit board. In this job an external Op Amp circuit for feedback loop is used.

There are several reasons to choose this approach. First, we are limited by the set of components in the design, i.e. only NPN transistors can be used (any PNP or CMOS are unavailable) and the number of transistors on the chip cannot be more than 40. This means that it is very hard to arrange the operational amplifier on the chip using only NPN transistors. Moreover, if we try to attempt this, the power dissipation of full circuit would increase rapidly due to the big current through transistors at operational amplifier which is necessary to get high gain at amplifier and better matching of bias at differential stage.

In conclusion of this discussion the authors would like to note that the first stage is actually TIA while the next three differential stages refer to the post-amplifier. TIA and the first two differential stages are used to obtain the necessary gain, and the third differential stage is used to match the output load of 50Ω.

The key advantage of this device is that it's fabricated using InP technology, which lets us integrate the photodiode on the same chip with TIA. That is a vital step forward to a highly integrated device. However, currently different processes are required to make the transistors and the photodiodes. Hence this solution requires a certain trade-off between the performance of TIA (bandwidth) and the optical characteristics of the photodiode.

Technology

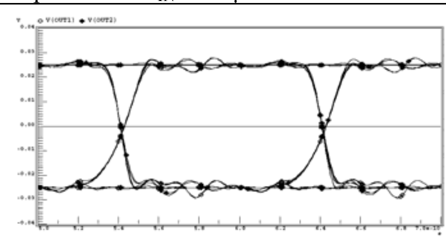
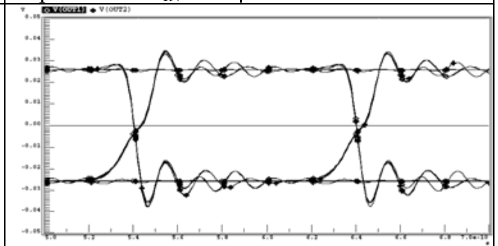
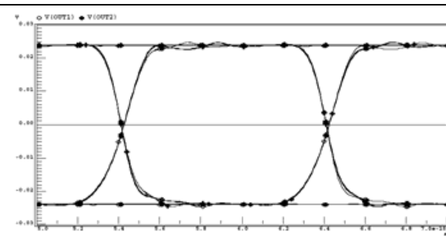
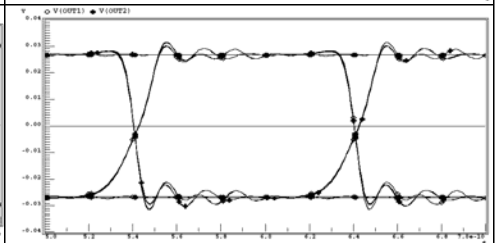
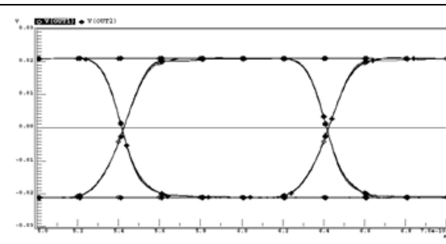
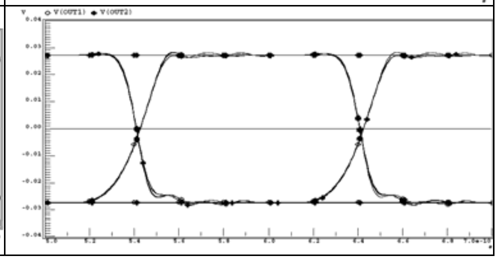
Initially epitaxial structure is grown by MOMBE (Metal Organic Molecular Beam Epitaxy). The layer structure is presented in [2]. The first process step is formation of the emitter by wet-etching of the emitter cap (InGaAs) and the InP emitter. Next step is base metal self-aligned deposition. The base metal is used then as an etching mask for the base. After base etching we have to isolate the emitter and base region for collector etching. Following passivation consists of a thick polyamide layer for good planarization. By unmasked dry-etching we can remove the polyamide until the emitter mesa break through the polyamide surface: self-aligned emitter contacts are created and only the less critical via holes for the base and the collector contacts remain to be generated by masked dry-etching.

Characteristics

The purpose of this work is to investigate the device performance in the temperature range -10^0C … $+130^0$C. Although these are only theoretical calculations the several important conclusions concerning the device performance can be reached.

One of the most informative characteristics of devices of such type is the eye diagram. The main amplifier characteristics such as gain, noise and power dissipation will be not discussed at this job. This job is focused on the eye diagrams because they represent the dynamic characteristics of an amplifier, such as rise and fall times, jitter, oscillations etc. Some eye diagrams are presented in the following table.

Table 1. Eye diagrams

	Input current I_{IN} = 25 μA	Input current I_{IN} = 50 μA
-10^0 C		
50^0 C		
130^0 C		

A current source with some parasitic elements approximating to real photodiode performance was used as a photodiode model in the simulation. The device performs conversion and amplification of current signal at the input to voltage signal at the output (hence the name TIA). Output peak-to-peak (swing) value is about 100 mVpp (for differential signal), which is enough for the CDR (clock and data recovery) circuit to separate high and low levels (logical 1 or 0). At higher input currents (50 μA in our case) the output peak-to-peak value is stable. However for smaller currents (25 μA) the output swing decreases at higher temperatures. This happens because at higher temperatures the gain is reduced by the lower currents at amplification stages. As for higher currents, we have a negative effect in the lower temperature ranges. You can see at the eye diagrams that there is a possibility of oscillations to occur, because at -10^0C and I_{IN}=50 μA the amplifier is overdriven. To avoid these issues, special schematic solutions should be made or the process should be improved.

Jitter is more observable at lower temperatures, but it is low enough and therefore not a critical parameter.

Transimpedance (the TIA gain) is measured in Ohms and equals 3600±400, depending on temperature and supply voltage (+V in FIG2).

The other important characteristic of amplifier is its noise performance. One of the ways to describe it is a characteristic called input equivalent noise density measured in $[pA/\sqrt{Hz}]$. It varies between $6\ldots7[pA/\sqrt{Hz}]$, which is quite small for this kind of devices.

This could be achieved because of advantage of InP technology process as we have mentioned earlier (at 1.2). The integration of the photodiode onto the amplifier chip enables us to avoid the bonding wires between the photodiode and TIA and therefore, to reduce input noise at TIA.

Conclusions

InP technology is undergoing an evolution and is promising. This process has two key advantages. These are high transistor bandwidth and the possibility of integrating the photodiode and TIA on the same chip. The present work is one of the trials in the perfection of InP technology. There is still much to do in the technology as well as in schematic areas to achieve good device parameters. One of the attempts of this was made by this study. The result is a TIA with good performance achieved at simulations.

References

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A. Aulas, B. Laurinavičius, M. Chusnutdinov. Integrinis plačiajuostis optinis InP imtuvas // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2005. – Nr. 1(57). – P. 67–70.

Pateikiami 10 Gbps optinio ryšio sistemų veikimo principai. Buvo koncentruojamasi į pagrindinę imtuvo grandinės dalį – pereinamosios varžos stiprintuvą (transimpedance amplifier, TIA). Jame integruotas fotodiodas priima šviesą iš optinio kabelio, optinį signalą keičia į srovę, ją sustiprina ir išėjime sukuria parafazinę įtampą. Šią funkciją galima atlikti keliais būdais. Tinkamiausias sprendimas šiuo atveju – naudoti išorinį grįžtamąjį ryšį su išoriniu operaciniu stiprintuvu. Simuliacijos metu buvo gautos geros charakteristikos naudojant „Cadence“ programų paketą. Šis TIA yra perspektyvus, nes taikoma InP technologija, kurios svarbiausi pranašumai yra greitaveikiai heterostruktūriniai tranzistoriai ir mikroschemoje integruotas fotodiodas. Tai leidžia sumažinti triukšmų lygį ir iškraipymus, kadangi nėra išorinio fotodiodo. Taikant InP ir kitas šiuolaikines puslaidininkines technologijas, tikimasi pasiekti 40 Gbps ir didesnę informacijos perdavimo spartą. Il. 2, bibl. 5 (anglų kalba; santraukos lietuvių, anglų ir rusų k.).

A. Aulas, B. Laurinavicius, M. Chusnutdinov. Broadband Optical Receiver IC on InP // Electronics and Electrical Engineering. – Kaunas: Technologija, 2005. – No. 1(57). – P. 67–70.

The principals of optical communication systems operating at 10 Gbps and more are presented at this paper. A Transimpedance Amplifier (TIA) is the main part here. The Photo Diode current is a single input signal for TIA, and the differential voltage is the TIA output signal. A several ways to provide a reference voltage (biasing) to the second input of differential stage are inspected. The mostly suitable solution in case of 10 Gbps TIA designed on InP process is the using of a feedback loop with external operation amplifier. The good performance of such TIA was demonstrated using simulations with cadence tool. TIA ICs designed on InP process look promising due to advantages, which goes to be important with the growth of communication speed. These are high transistor bandwidth and the possibility of integrating the photodiode and TIA on the same chip, what reduces noises and signal distortions. This lets to foretell the optical receiver IC on InP process will be used at 10…40 Gbps area. Ill. 2, bibl. 5 (in English; summaries in Lithuanian, English and Russian).

А. Аулас, Б. Лауринавичюс, М. Хуснутдинов. Интегральный широкополосный оптический приемник на InP // Электроника и электротехника.– Каунас: Технология, 2005. – № 1(57). – С. 67–70.

Представлены принципы оптической связи со скоростью передачи информации 10 Гигабит/сек. и более, где основным узлом обработки информации является трансимпедансный усилитель (TIA). Входным сигналом для TIA служит ток фотодиода, а сигнал на выходе – парафазное напряжение. Рассмотрены различные способы организации опорного напряжения для второго входа дифференциального каскада TIA. Наиболее подходящим для 10 Гб/с TIA, выполненного на InP-технологии, представляется подача опорного напряжения с выхода внешнего операционного усилителя, сравнивающего средние значения напряжений сигнала на обоих выходах TIA. Приведены расчетные данные (так называемые EYE Diagrams, уровень шумов и др.), показывающие возможность получения необходимых параметров TIA при применении выбранного способа смещения второго плеча дифф. каскада. Расчеты выполнены на симуляторе Cadence. TIA на основе InP-технологии представляет большой интерес с увеличением скорости передачи информации. InP-технология имеет важные преимущества – она позволяет формировать фотодиод и TIA на одном кристалле, что уменьшает уровень шумов и искажений, кроме того транзисторы на InP имеют большую полосу усиления. Это позволяет прогнозировать все более широкое применение InP-технологии в производстве оптических приемников с быстродействием 10...40 и более Гб/с. Ил. 2, библ. 5 (на английском языке; рефераты на литовском, английском и русском яз.).