Promising Method of IC Operation Speed Testing at the Production based on 3-rd Harmonic Measurement

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Introduction

The ability of high-speed communication ICs to operate at max defined speed (more than several gigabits NRZ) is often characterizes by Rise/Fall time parameter (pulse edge speed). This parameter values stated at specification have to be proved and guaranteed by production test. However, direct rise/fall time measurement is usually enough complicated, time and cost spending. This can show stopper at achieving the smallest cost which is absolutely critical both for components and whole devices such as USB 3.0, or others.

The relevant IC-test deliverers mainly utilize the most popular "Catalyst GIGADIG"-instrument for RF-test at high volume and low cost production. It's not enough convenient for time-domain measurements at more than several gigabits, but able to ensure the productive frequency-domain test up to 6GHz of sine signal [1].

The objective of this work is the investigation and bringing of the prompt result on ability of non-direct frequency-domain test to provide the sorting of communication ICs in terms of operation at max speed, such as 10Gbps. It's intended to help customer at achieving the low cost and required accuracy at high volume production test.

Essentials of the method

Periodic waveforms such as the sine curve of alternating current can be represented as a *Fourier series*. A Fourier series is an infinite sum of sine and cosine terms, which are themselves periodic, and therefore useful in representing a periodic function. Other periodic functions include sawtooth waves, square waves, and rectified half-waves. Given a function $f(x)$ of period 2π, a Fourier series for that function is of the form [2]:

$$f(x) = \frac{1}{2}a_0 + a_1\cos x + a_2\cos 2x + a_3\cos 3x + ...$$
$$+ b_1\sin x + b_2\sin 2x + b_3\sin 3x + ... \quad (1)$$

where the Fourier coefficients a_n and b_n are given by the following equations

$$a_n = \frac{1}{\pi}\int_{-\pi}^{\pi} f(x)\cos(nx)dx, \quad (2)$$

$$b_n = \frac{1}{\pi}\int_{-\pi}^{\pi} f(x)\sin(nx)dx. \quad (3)$$

Consider the square wave (see Fig.1), This appears to be a difficult case - the rather angular square wave does not look as if it will be readily expanded in terms of sine and cosine functions.
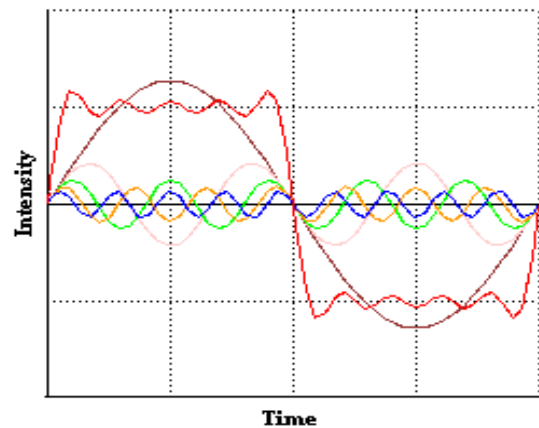

Fig 1. Square wave harmonics

The coefficients in the expansion can be determined from the formulae given previous, just draw $\cos(x)$ to see that its integral from $0 \to \pi$ is zero, so $a_n = 0$ *(for all n).*

For the b coefficients we have,

$$b_n = \frac{1}{\pi}\int_0^{+\pi}\sin(nx) = \frac{1}{\pi}\left[\frac{-\cos(nx)}{n}\right]_0^{\pi} = \frac{1}{n\pi}(1-\cos(n\pi)) \quad (4)$$

But,

$$\cos(n\pi) = +1, \quad n-\text{even} \quad (5)$$
$$= -1, \quad n-\text{odd}$$

so,

$$b_n = 0, \qquad n - even \qquad (6)$$
$$2/n\,\pi, \qquad n - odd$$

having determined all of the coefficients we can write the series for f(x) as [2]:

$$f(x) = \frac{1}{2} + \frac{2}{\pi}\left(\sin(x) + \frac{\sin(3x)}{3} + \frac{\sin(5x)}{5}...\right). \qquad (7)$$

The sum continues to an infinite number of terms. From formulae 7, we can see that square signal is determined by odd harmonics'.

In the following we are going to consider only 3rd harmonic behavior

Test setup

The key device is spectrum analyzer which displays a power spectrum over a given frequency range, changing the display as the properties of the signal change (Fig. 2).
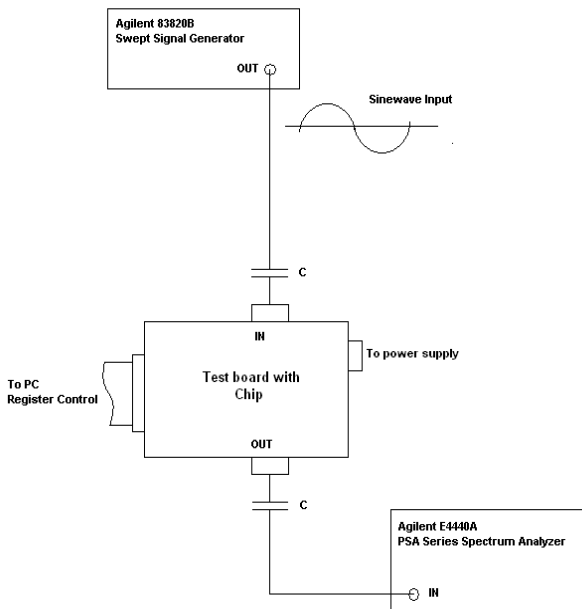

Fig. 2. Test set up block schematic

There is a trade-off between how quickly the display can be updated and the frequency resolution, which is for example relevant for distinguishing frequency components that are close together. With a digital spectrum analyzer, the frequency resolution is $\Delta\nu = 1 / T$, the inverse of the time T over which the waveform is measured and Fourier transformed. With an analog spectrum analyzer, it is dependent on the bandwidth setting of the bandpass filter. However, an analog spectrum analyzer will not produce meaningful results if the filter bandwidth (in Hz) is smaller than the square root of the sweep speed (in Hz/s), which means that an analog spectrum analyzer can never beat a digital one in terms of frequency resolution for a given acquisition time. Choosing a wider bandpass filter will improve the signal-to-noise ratio at the expense of a decreased frequency resolution.

The spectrum analyzer does not need to be specified at very wide frequency range. If there is IC with speed of 10Gbit/s, used for communications, the spectrum analyzer enough to measure to 6 GHz to fulfill all time-domain measurements. So the test equipment can be used more cheaply.

Test results.

The correlation between time-domain parameter values (Rise/Fall time) and frequency- domain test results (3rd harmonic data) was used as criteria of frequency-domain method availability.
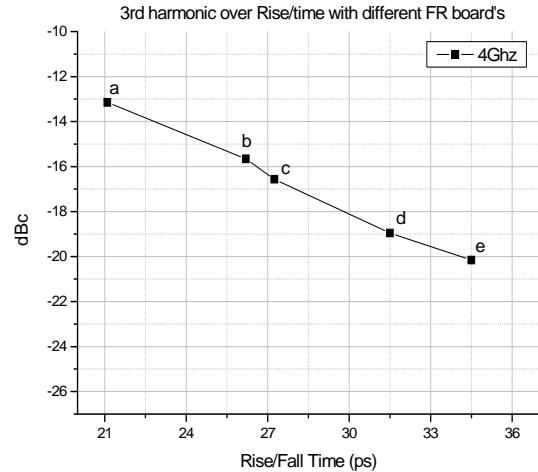

Fig. 3. Measurements with different PCBoards made. PCBoard trace length respectively: a:0 mm, b:52 mm, c:102mm, d:152mm, e:202mm
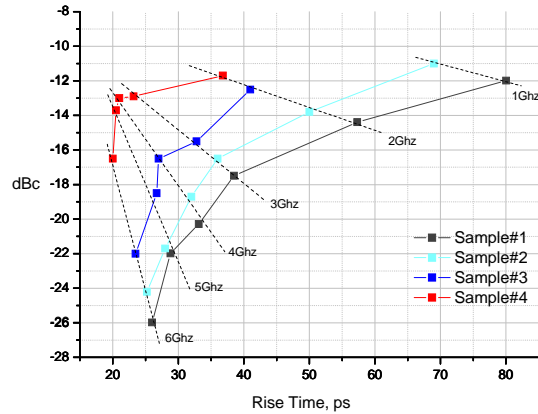

Fig. 4. 3-rd Harmonic vs Rise time over the $f_{in}=1...6$GHz. Test provided on four samples having the different Rise time@11.3Gpbs

At the beginning five PCBoards with different signal trace lengths (a: 0 mm, b:52 mm, c:102mm, d:152mm, e:202mm) [3] were prepared and tested on both Rise/Fall time at 10Gbps and 3rd harmonic at 4 GHz input sinewave. Test results shown at Fig. 3 demonstrate the clear correlation between Rise/Fall time and 3rd harmonic distortion.

Whereat the four communication IC-samples with different Rise/ Fall time in the range 19…50ps at 11.3Gbps were prepared. Frequency-domain measurements were provided over the different frequency range 1…6GHz. The good correlation between Rise/Fall time and 3rd harmonic distortion was provided in this case too (see Fig. 4).

Conclusion

The Promising Method of IC Operation Speed Testing based on 3-rd Harmonic measurement have been investigated both by using the different samples of PCBoards and communication ICs.

This method is designed for production test of communication ICs in terms of operation at max speed, such as 10Gbps. It is able to replace the enough complicated, time and cost spending time-domain measurements and intended to help customer at achieving the low cost and required accuracy at high volume production.

The investigation had been provided with limited time and resources, and was successfully integrated to manufacturing process This method is efficient for large variety of High speed ICs at the Production test (sorting).

References

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2. **Tolstov G. P.** Fourier Series. Courier Dover Publications, 1976 , ISBN 0486633179.
3. **Johnson H., Graham M.** High–Speed Digital Design. A Handbook Of Black Magic, Prentice Hall PTR, 1993. ISBN 0–13–395724–1.

Acknowledgments

A. Aulas, R. Vadoklis, V. Dangelas, A. Kiseliov, M. Chusnutdinov, I. Mazurkevič. Promising Method of IC Operation Speed Testing at the Production based on 3-rd Harmonic Measurement // Electronics and Electrical Engineering. – Kaunas: Technologija, 2009. – No. 6(94). – P. 106–108.

The production test and sorting of high speed communication ICs up to 10 Gb/s, is currently complicated technical task for manufacturer. The relevant IC-test deliverers often utilize the "Catalyst GIGADIG"-instrument for RF-test at high volume and low cost production. However, it's not applicable for Rise/Fall time measurements at more than several gigabits per second, but able to ensure the productive frequency-domain test up to 6GHz of sine signal. The objective of this work is the investigation and bringing of the prompt solution on ability of non-direct frequency-domain test instead of direct Rise/Fall time measurement for sorting of communication ICs in terms of operation at max speed, such as 8-10Gbps. The intention is to help IC-manufacturers at achieving the low cost and required quality at high volume production test. Ill. 4, bibl. 3 (in English; abstracts in English, Russian and Lithuanian).

А. Аулас, Р. Вадоклис, В. Дангялас, А. Киселев, М. Хуснутдинов, И. Мазуркевич. Многообещающий метод высокоскоростного тестирования ИС в массовом производстве, основанный на измерении 3-ей гармоники // Электроника и электротехника. – Каунас: Технология, 2009. – № 6(94). – С. 106–108.

Производственные измерения и разбраковка высокоскоростных (вплоть до 10Гб/с) интегральных микросхем для телекоммуникаций является сегодня сложной технической задачей для производителя. Стремясь снизить цену при массовом производстве, компании часто используют оборудование "Catalyst GIGADIG" при оценке работы микросхем на максимальной скорости. Это оборудование не обеспечивает качественного измерения длительности фронта импульсного сигнала при скорости передачи данных близкой к 8-10 Гб/с, однако может обеспечить частотные измерения вплоть до 6ГГц синусоидального сигнала. Целью этой работы является исследование и нахождение быстрого решения, основанного на частотных измерениях взамен измерения длительности фронта импульсного сигнала для оценки работы интегральных микросхем на максимальной скорости, такой как к 8-10 Гб/с. Ожидается, что это поможет производителям уменьшить цену и обеспечить качество разбраковки интегральных микросхем при массовом производстве. Ил. 6, библ. 11 (на английском языке; рефераты на английском, русском и литовском яз.).

A. Aulas, R. Vadoklis, V. Dangelas, A. Kiseliov, M. Chusnutdinov, I. Mazurkevič. Trečiosios harmonikos matavimo metodo taikymas greitaveikėms integrinėms schemoms testuoti // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2009. – Nr. 6(94). – P. 106–108.

Greitaeigių (apie 10Gb/s) telekomunikacinių integrinių schemų testavimas ir atrinkimas gamybos procese šiandien yra sudėtinga techninė užduotis gamintojui. Siekdamos kiek galima atpiginti masinę gamybą pasaulio kompanijos dažnai naudoja "Catalyst GIGADIG" įrangą integrinių schemų veikimui, esant maksimaliam greičiui, įvertinti. Šia įranga negalima kokybiškai išmatuoti impulso fronto trukmės, kai duomenų perdavimo greitis didesnis kaip keletas gigabitų per sekundę, tačiau galima atlikti iki 6 GHz sinusinio signalo dažnio matavimus. Šio darbo tikslas – atlikti tyrimus ir rasti greitą sprendimą, pagrįstą dažnio matavimais, kurie pakeistų impulsinio signalo fronto ilgio matavimus siekiant nustatyti, kaip veikia integrinės schemos esant maksimaliam greičiui, pavyzdžiui, 8–10Gb/s. Tai gali padėti integrinių schemų gamintojams sumažinti kainą ir pagerinti integrinių schemų atrinkimo kokybę masinėje gamyboje. Il. 4, bibl. 3 (anglų kalba; santraukos anglų, rusų ir lietuvių k.).