Advanced Design of DSP-based High Precision Event Timer

V. Vedin

Institute of Electronics and Computer Science
Dzerbenes st. 14, LV-1006 Riga, Latvia, phone: +371 7554500; e-mail: vedinv@edi.lv

Introduction

A good many various techniques associated with time measurements have been developed over years. In most of applications it is time intervals that have to be measured. Traditionally they are measured by employing time interval measurement techniques. However, during last years, a new approach to time measurements, which is based on event timing, has become popular. Timing the events means that their position with respect to a time axis is measured. In general case this gives more information about events including time intervals between them, which can be extracted from the primary timing information.

Event timers are characterized by a number of specific parameters of performance. Depending on particular targeted tasks and applications these parameters may have different degree of importance. In many applications such parameters as RMS resolution, "dead time", and measurement range are regarded as the most important ones. There are tasks that require both high speed and high precision or, in other words, high productivity of event timers.

Let us introduce the productivity factor (P) as a joined parameter for highly-productive event timers, which would be useful to compare them:

$$P = 1/(D \cdot R), \qquad (1)$$

where D − "dead time", ns; R – RMS resolution, ns. It is easy to see that event timers with different D and R are able to "produce" the same amount of valuable data during some particular time if their productivity factors P are equal. Of course, such simple joined parameter does not lay claim to be fully exhaustive, but at least it can give a good estimation criterion for a particular event timer or an event timing method.

There are two distinctive subclasses of high-productivity event timers. The event timers of the first one are usually based on tapped delay lines and have typically very short "dead time" (units of ns). Their RMS resolution, however, is rather limited (from around a hundred of ps to units of ns).

The subject of the paper is related to the second subclass that is characterized by high RMS resolution (about dozens of ps or less) and acceptable "dead time"

within the range from hundreds of ns down to dozens of nanoseconds. For example, the technology cutting edge event timer HTSI made in Honeywell Technology Solutions Lab [1] provides RMS resolution of 4 ps and the "dead time" of 100 ns which results in productivity factor of 2.5 ns^{-2}.

The timers based on Enhanced Event Timing (EET) method fall into the second category. In particular, the event timer A032-ET [2] has 7 ps RMS resolution and 60 ns "dead tome". The productivity factor (P_1) is as follows:

$$P_1 = 2.38 \ (ns^{-2}). \qquad (2)$$

The principle of the EET method [3] is that a primary input measured pulse signal (event) is converted into a secondary analog signal by generation of such signal at the time instant of input event arrival. Then this secondary analog signal is digitized using an A/D converter and digitally processed by a specific algorithm to estimate its position relative to the periodic sampling pulse sequence (or, in other words, relative to the discrete uniform time scale).

The possibilities of EET method are not yet fully realized and leave room to substantially improve the productivity of EET-based timers. Techniques for doing that are considered in this paper.

Generation of the secondary signal

Generation of the secondary signal is a key function in realization of the EET method. It is obvious that the length of the secondary signal has to be as short as possible for reducing the "dead time". The recovery time, after the process is over, has to be as short as possible as well. On the other hand, it is desirable to get as many highly informative samples as possible from single realization of the signal.

A single piece of a symmetrical saw tooth signal ("triangular" signal) is well suited for the purpose and was chosen for the implementation of EET-based event timers. Additional samples or at least one sample can be taken on the falling slope of such signal. The symmetrical secondary signal of this kind can be realized in electronics much easier than the asymmetrical one with very sharp falling

slope. A simple principle based on charging and discharging a capacitor with dynamic diode stabilization of initial base ("zero") level was applied for the design of a "triangular" signal shaper (Fig. 1).
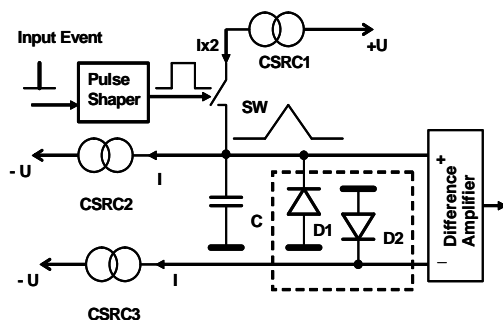

Fig. 1. Principle of operation of "triangle" signal shaper

In the initial state the switch SW is OFF, the current I from the current source CSRC2 flows via the diode D1. The voltage of p-n junction of the diode D1 determines the voltage across the capacitor C. When an input event pulse arrives the Pulse Shaper produces a pulse that switches ON the switch SW. The width of this pulse is equal to To. During this time the capacitor C is charged by the difference between two currents, which is I. It happens this way because, after a short transition time, the diode D1 gets reverse biased and becomes non-conductive. After the trailing edge of the pulse from the pulse shaper the switch SW is OFF again and the capacitor is discharged by the current I from the source CSRC2. At some point the diode becomes forward biased and the output voltage reaches the initial level. This initial "zero" level tends to change with the temperature. The second diode D2 sitting on the same substrate is used for compensating the temperature drift of the initial level.

In reality the obtained shape of the "triangle" signal is not an ideal triangle. Transition processes take place in the beginning, at the apex, and at the end of the signal. These processes are placed outside the dynamic range of the ADC as shown in Fig. 2, which actually results in "trapezoidal" secondary signal with unused top.
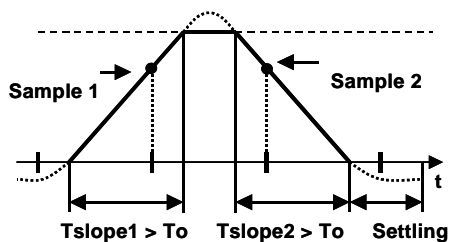

Fig. 2. "Trapezoidal" secondary signal

For achieving a minimum length of such signal and surely obtaining at least one sample on each slope of the signal the duration of slopes (*Tslope*) has to be more than *To*. Such shape is optimal [3] for achieving best precision with minimum duration of the signal.

The transitions cause a certain increasing of the signal duration. The most critical transition is the final one because the voltage across the capacitor C has to return to its initial value with required accuracy. The final transition

is determined by the exponential process of discharging the capacitor C via the differential resistance of the forward biased diode D (approximately at the barrier potential voltage). For instance, a typical differential resistance of a Schottky diode is less than 2 Ω. For a capacitor of, say, 150 pF it results in time constant $\tau = 0.3$ ns. Hence, within 3 ns (10τ) the voltage across the capacitor C is settled with 0.0045% error with respect to the initial value (0.4 V approximately), which is negligibly small.

In reality the shape of the secondary signal is not ideally trapezoidal. The actual shape of the signal is derived by applying a specific calibration procedure [2] that is adapted for the employed DSP. As a result of the calibration, one may say that a specific transfer function is obtained to translate the digitized values into a time-stamp.

A newly designed "triangle" signal shaper is one of most important components for the new version of EET-based event timers (model A033-ET). The use of up-to-date high-speed electronic components, including an RF Schottky diodes, resulted in certain reduction of the duration of the secondary signal and, correspondingly, in shortening the "dead time" – down to 50 ns (from 60 ns for A032-ET). The employing of the diode temperature compensation caused significant improvement of the temperature stability of the secondary signal shape. As in the A032-ET a cable delay transmission line maintains the stability of the Pulse Shaper (see Fig. 1).

Possibilities for increasing the precision

The timing error of EET-based event timers mainly is caused by A/D quantization errors, intrinsic noise of electronic hardware, and errors of the transfer function evaluation (integral non-linearity).

The latter errors are, strictly speaking, systematic ones. Normally the input measured events are not synchronized with the periodic sampling pulse sequence of an event timer. They are rather random and, hence, errors of the transfer function can be regarded as being such. In most cases all main error components can be regarded as normally distributed and characterized by RMS values. In particular, the A032-ET precision is characterized typically by the following approximate RMS values of error components: A/D quantization errors - 3.5 ps, integral non-linearity errors - 2.6 ps, internal noises - 2.0 ps. Considering that these error components as statistically independent, the RMS resolution of the A032-ET can be estimated as 7 ps. These estimates well conform to the RMS resolution (6-8 ps) experimentally evaluated for a number of A032-ET event timers.

Evidently, an increase of the precision can be done by using a higher resolution A/D converter (to decrease quantization errors) and by more qualitative implementation of hardware (to reduce integral non-linearity errors and internal noises).

Design of advanced EET-based event timer and experimental results

In the process of redesign the new above described "triangle" signal shaper was incorporated, the 10-bit A/D

converter has been replaced by more advanced 12-bit converter AD9432 from Analog Devices. Additionally, obsolete high-speed logical NECL chips have been replaced by the modern LVPECL chips, an FPGA chip (Altera CycloneII) has been employed instead of an outdated CPLD chip for real-time digital operations. PCB conductors between the most sensitive hardware components have been revised and more careful board design has been carried out to minimize internal noises. The ground plane of the noise-sensitive front end components as well as the ground plane of the "triangle" signal shaper was separated from the "digital" ground. The necessary inter-connections between these parts of the device were realized by differential transmission lines. As a result a fully new board of the timer hardware has been built.

The hardware means are housed in a standard plastic enclosure (EUROCASE; dimension: 367x250x76 mm), the new event timer will be available on a customer request as the model A033-ET.

Test results show, that, as a result of the mentioned modifications, the A033-ET error components can be characterized by the following approximate figures: AD quantization errors – 1.1 ps, integral non-linearity errors – 1.7 ps, internal noises – 1.1 ps.

The integral non-linearity errors have been experimentally evaluated directly after device calibration (Fig.3).
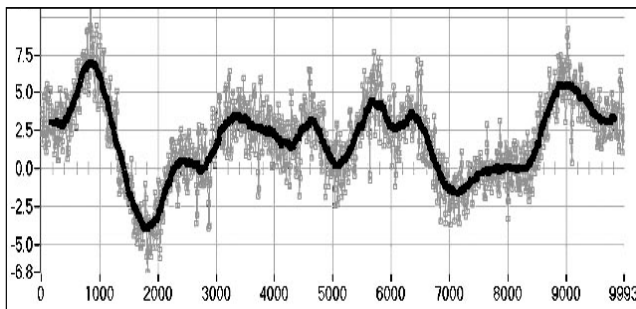

Fig. 3. A033-ET integral non-linearity errors (in ps) over interpolation interval

These estimates conform to the calculated RMS resolution about 3.3 ps. In other words, precision of the A033-ET is two times better than that of the A032-ET. Such conclusion is confirmed by the test results of the A033-ET. Temperature stability tests (Fig.4) show that the best resolution (about 3.4 ps) is supported if the ambient temperature is in the range $T_{CAL} \pm 1\ ^0$C, where T_{CAL} is the ambient temperature when the device has been calibrated. However, sufficiently good resolution is supported without re-calibration in much wider range of ambient temperature variation.

As a result, having the "dead time" 50 ns and the RMS resolution less than 3.5 ps, the following productivity factor has been obtained:

$$P_2 = 5.71\ (\text{ns}^{-2}). \qquad (3)$$

As one can see, the obtained figure is practically 2.5 times better than that of the previous model A032-ET and more than 2 times better then the model HTSI ET.
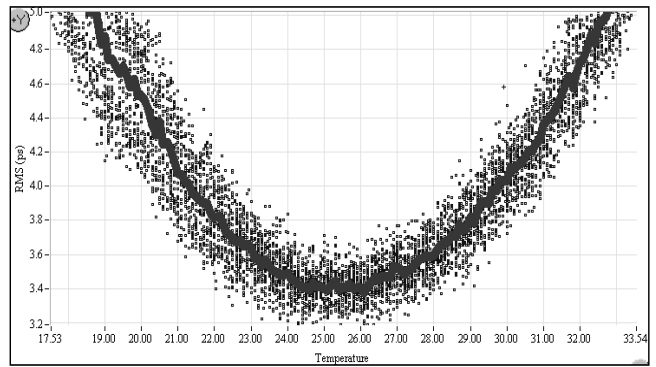

Fig. 4. A033-ET RMS resolution vs. ambient temperature variation (T_{CAL}= 25 ^{0}C)

Event Timer Module

The Event Timer Module (ETM) is being developed as a semi-customized product intended for incorporating into various customized timing systems. The design covers a certain degree of flexibility to ease the adaptation of the ETM to specific customer requirements.

Principles of the ETM operation are almost the same as for the A033-ET but emphasis in its implementation is made on achievement of hardware compactness. For this purpose the "triangular" signal shaper was modified to get rid of the bulky cable delay line, PLL-based clock signal synthesizer is incorporated into the module board. An FPGA is used to provide customized modifications of the ETM operation to meet particular requirements of application.

The exclusion of the cable delay line was done by using a different Pulse Shaper (see Fig. 5). When an input event pulse comes the Flip-flop is set. The generated secondary signal is compared with some constant threshold and, as soon as it reaches the threshold, the Comparator resets the Flip-flop.
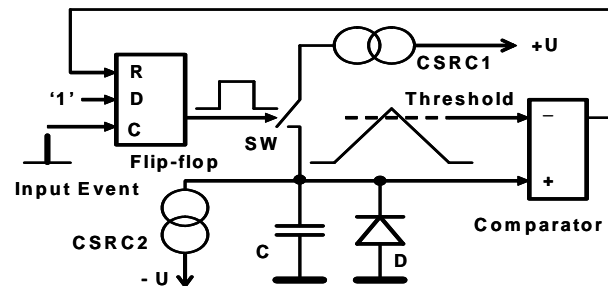

Fig. 5. "Triangle" signal shaper with a comparator-based Pulse Shaper

Due to all these modifications relatively small size of ETM card (130x210 mm) and power consumption less than 6W have been achieved.

The ETM precision parameters are pretty close to those of the A033-ET, the preliminary tests confirm that. The experimentally estimated RMS resolution of the ETM pilot version was about 3.5 ps. The "dead time" is the same as for the A033-ET – 50 ns, and so is the productivity factor – 5.71 (ns^{-2}).

Conclusions

The taken measures allowed to better realize the potential of the EET method. The introduced composite parameter of productivity served well for estimating the degree of improvement of EET-based event timers and for comparing them with similar products.

Enhancement of the shaper of the secondary signal as well as other technical solutions made it possible to significantly elevate the precision (2 times) and, to some extent, the "dead time". That resulted in obtaining substantially better productivity factor – 2.5 times better in comparison with the previous model A032-ET.

References

1. **McClure D., Steggerda C., Wetzel S.** High–Speed Enhancement to HTSI Event Timer System. 15th International Workshop on Laser Ranging, Canberra, Australia. – 2006. http://cddis.gsfc.nasa.gov/lw15/index.html
2. **Bespal'ko V., Boole E., Vedin V.** The Model A032–ET of Riga Event Timers. Proceedings of the 15th International Workshop on Laser Ranging, Canberra, Australia. – 2006. http://cddis.gsfc.nasa.gov/lw15/index.html
3. **Artyukh Yu.** High–resolution Event Timing Based on Analog Signal Digitizing. Proceedings of the 8th Biennal Electronics Conference. – Tallinn, Estonia. – 2002. – P. 237–238.

V. Vedin. Advanced Design of DSP-based High-Precision Event Timer // Electronics and Electrical Engineering. – Kaunas: Technologija, 2009. – No. 6(94). – P. 35–38.

Techniques for considerable advancing the precision and operational speed of event timers, based on the Enhanced Event Timing (EET) method, are considered. The method employs digital processing of analog signals that reflect the event positions. Emphasis is made on improving the generation of such signals, which, along with other technical enhancements of design, resulted in RMS resolution 3.5 ps and "dead time" 50 ns. In comparison with the previous event timer model based on the same method, the performance improvement is 2.5 times in terms of productivity factor characterizing the precision/speed ratio in a generalized form. Ill. 5, bibl. 3 (in English; summaries in English, Russian and Lithuanian).

В. Ведин. Усовершенствование прецизионного таймера событий, основанного на цифровой обработке сигналов // Электроника и электротехника. – Каунас: Технология, 2009. – № 6(94). – С. 35–38.

Рассмотрены методические и технические решения, направленные на значительное повышение точности и быстродействие таймера событий, основанного на одном особом методе таймирования. В методе используется цифровая обработка сигналов, которые отражают временное положение таймируемых событий. Акцент сделан на усовершенствование генерации таких сигналов, что, наряду с другими техническими мерами, позволило получить среднеквадратическую погрешность 3,5 пс и "мертвое время" 50 нс. По сравнению с предыдущей моделью таймера событий, реализующего тот же метод таймирования, качество устройства, выраженное как обобщенный показатель его производительности, улучшилось в 2,5 раза. Ил. 5, библ. 3 (на английском языке; рефераты на английском, русском и литовском яз.).

V. Vedin. Tikslaus laikmačio savybių gerinimas skaitmeninių signalų apdorojimo metodu // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2009. – Nr. 6(94). – P. 35–38.

Išanalizuotos metodinės ir techninės priemonės, leidžiančios gerokai padidinti laikmačio tikslumą ir greitį taikant metodą, pagrįstą skaitmeninių signalų apdorojimu. Šis metodas atspindi laikines įvykių savybes. Pagrindinė idėja remiasi signalų generacija taikant įvairias technines priemones. Buvo gauta 3,5 ps paklaida ir 50 ns „neveikos trukmė". Palyginti su ankstesniu įvykių modeliu, našumas padidėja 2,5 karto. Il. 5, bibl. 3 (anglų kalba; santraukos anglų, rusų ir lietuvių k.).