

## Hysteretic-controlled Voltage Regulator using Integrated Circuit LM723

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### Introduction

Linear power regulators, whose principle of operation is based on a voltage or current divider, are inefficient. This is because they are limited to output voltages smaller than the input voltage, and, at the same time, their power density is low because they require low frequency (50Hz) line transformers and filters. Electronic devices in linear regulators operate in their active (linear) modes, but at higher power levels switching regulators are used [1, 2].

A dc-dc converter must provide a regulated dc output voltage under varying load and input voltage conditions. The converter component values are also changing with time, temperature, pressure, and so forth. Hence, the control of the output voltage should be performed in a closed-loop manner, using principles of negative feedback. The two most common closed-loop control methods for PWM dc-dc converters are, namely, the voltage-mode control and the current-mode control.

Among other control methods of dc-dc converters, a hysteretic (or bang-bang) control is very simple for hardware implementation. However, the hysteretic control results in variable frequency operation of semiconductor switches. Generally, a constant switching frequency is preferred in power electronic circuits for easier elimination of electromagnetic interference and better utilization of magnetic components [3, 4].

### Operational Principle

Hysteretic control, also known as bang-bang control or ripple regulator control, maintains the converter output voltage within the hysteretic band centered about the reference voltage. The hysteretic-controlled regulator is popular because of its inexpensive, simple and easy-to-use architecture. The greatest benefits of hysteretic control are that it offers fast load transient response and eliminates the need for feedback-loop compensation. The other well-known characteristic is the varying operating frequency [5, 6, 7]. However, the regulation inaccuracy issue of the hysteretic-controlled converter is almost unknown to engineers. Until now, research on hysteretic regulators has

mainly focused on transient analysis and transient modeling [7, 8].

The first analysis of accuracy was performed on a current-mode hysteretic regulator specifically designed to power microprocessors [6]. However, the regulation accuracy of the more widely used voltage-mode hysteretic-controlled regulators is still unknown.

This analysis also reveals how operating conditions (input voltage  $[V_1]$ ; output voltage  $[V_0]$ ; component sizes (inductor L, output capacitor  $C_S$ ) and parasitic parameters (ESR, ESL, DCR, etc.) affect the accuracy of dc regulation [9]. Most importantly, this analysis influences the design process for hysteretic-controlled dc-dc converters and enables practical design tradeoffs to be made.

Fig. 1 shows a simplified hysteretic-controlled voltage regulator and its ideal operating waveforms.

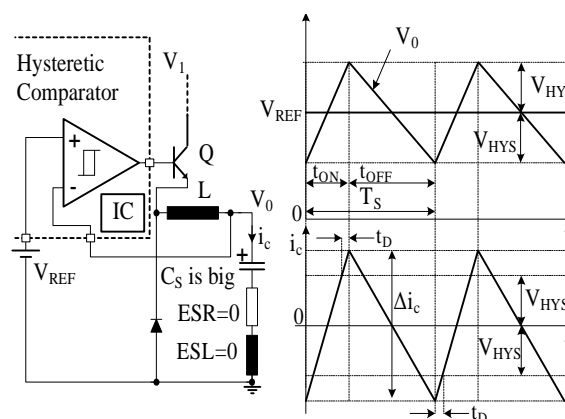


Fig. 1. Simplified hysteretic control voltage regulator and operating waveforms

If output voltage  $V_0(t)$  is at or below the level of the reference  $V_{REF}$  minus the hysteresis  $V_{HYS}$ , output of the hysteretic comparator is high and Q is turned on. This is the power stage on-state and it causes the output voltage to increase. When the output voltage  $V_0(t)$  reaches or exceeds the reference  $V_{REF}$  plus the hysteresis  $V_{HYS}$ , the output of the hysteretic comparator turns low and then Q is turned

off. This is the power stage off-state, and it causes the output voltage to decrease. This hysteretic method of control keeps output voltage within the hysteresis band around the reference voltage, which leads the dc value of output voltage to be the reference voltage, namely  $V_O = V_{REF}$ , without any dc offset.

Let's consider that the output capacitor  $C_S$  has a high value, which leads to a low output voltage ripple, as shown in Fig.1. The output voltage's peak ripple above  $V_{REF}$  is equal to  $V_{HYS}$ , and the output voltage's valley ripple below  $V_{REF}$  is equal to  $V_{HYS}$ , too. So, the dc value of the output voltage is still regulated at  $V_{REF}$  without any offset [8].

Applying this hysteretic control method, we propose below a dc-dc converter circuit using the LM723 integrated circuit. This IC is specially designed to perform the linear regulation function, but it can also be used, as we shall see, in applications of dc-dc power conversion.

The dc-dc converters with voltage-mode control to propose in Fig.2 consists of a LM-723 integrated circuit. The LM723 works with input DC voltages from 9.5 - 40V and the IC itself can source 150mA maximally. However it can be used with external transistor to handle load currents up to 10A. The shows a simplified circuit of LM-723 [9], which contains a temperature-compensated voltage reference, differential amplifier, series pass transistor Q, and current-limiting protection circuit. It has to connect with external circuits to work as a regulator. The voltage reference circuit  $V_{REF}$ , provides a reference voltage, typical 7.15V for LM723. The voltage from the non-inverting input of the Operational Amplifier (+NI) within the integrated circuit, is obtained by dividing the reference voltage of 7.15V, using  $R_1$  and  $R_4$  resistors. The circuit made up of  $R_1$  and  $R_3$  resistors and  $C_3$  capacitor provides the "soft start" functioning of the circuit, namely the slow increase of the initial voltage. Because of this, the output capacitor  $C_S$  is charged with a low current when the power supply is connected, which avoids the current protection circuit to disable the control in these transient moments. By using  $R_8$  and  $R_9$  resistors, the output voltage is applied to the inverting input (-IN) of the operational amplifier.

As long as the inverting input voltage (from the operational amplifier) is lower than the non-inverting input voltage, the output voltage of the error amplifier (error amplifier working as hysteretic comparator) will determine the transistor Q (within the Integrated Circuit) to enter in ON state, as well as transistors  $Q_1$  and  $Q_2$ . In this functioning state diode D is OFF and the voltage across inductance L is

$$v_L = V_1 - V_0. \quad (1)$$

The  $i_L$  current starts to increase, compensates the  $I_S$  load current, and when the value surpasses  $I_S$ , it charges the capacitor  $C_S$ . Considering this, the voltage across  $C_S$  capacitor increases and when this value surpasses the reference voltage applied to the non-inverting input of the error amplifier, the output voltage of the error amplifier will turn OFF the Q transistor, as well as  $Q_1$  and  $Q_2$  transistors. If the  $Q_2$  transistor is OFF, across the L inductance an electromotive voltage will appear. The energy stored in the electromagnetic field of the L

inductance is transferred through the D diode to the output resistor  $R_S$ . When it is ON, the diode D insures a closed loop of the  $I_S$  current in the same direction as when  $Q_1$  and  $Q_2$  were in saturation modes. In this case, the voltage across the L inductance is

$$v_L = -V_0 - V_D. \quad (2)$$

The voltage from the capacitor  $C_S$  starts to decrease, and when this value is below that of the non-inverting input voltage, the output voltage of the error amplifier will determine again the transistors Q,  $Q_1$  and  $Q_2$  to enter in ON state modes, and the function cycle will continue this way. Because the output current of LM723 is lower than 150mA and the gain of  $Q_2$  is small, it is necessary to use an amplifier stage with  $Q_1$  and  $R_{12}$ . Zener diode  $D_Z$  is used to prevent the voltage from the output transistor to surpass, in any circumstances, the value of 40V. Resistance  $R_{10}$  is used to limit the current through the output stage of LM723, protecting this stage from over-current, and  $R_{11}$  resistor allows the evacuation of the charges from the base of the  $Q_2$  transistor when it is turned ON, leading to reduced commutation time and low power dissipation on the transistor. To increase the efficiency of the circuit, it is important to have low voltage across D diode, and the working frequency to be as high as possible; in this case, it is necessary to use a commutation diode. The circuit is completely stabilized even at the extremes of its output range and is fully protected against short-circuits and overloading.

In the current-limiting circuit, the voltage drop cross the terminal CL and CS should be less than 0.65[V] (a voltage drop cross a diode) [10].

Voltage limita for the curent  $I_S$

$$V_{R_0} = I_{S\lim} \times R_0, \quad (3)$$

$$V_{R_0} = V_{BE(CL-CS)} + V_{R_7} = 0,65 + (V_1 - V_0) \frac{R_7}{R_7 + R_6}. \quad (4)$$

Considering (3) and (4)

$$I_{S\lim} = \frac{V_{R_0}}{R_0} = \frac{0,65}{R_0} + \frac{V_1 - V_0}{R_0} \frac{R_7}{R_7 + R_6}. \quad (5)$$

$R_6$  and  $R_7$  resistances are used for feeding the positive reaction, thus maintaining the commutation action, even if there is a short circuit at the output. This prevents the increase of the power dissipation over the  $Q_2$  transistor, situation which could occur if the converter functioned as a linear power regulator.

The  $R_5$  resistor insures the hysteresis of a sure source functioning. When the  $Q_2$  transistor is saturated, the voltage of its emitter is  $V_1$ , and the voltage at the non-inverting input (+NI) is

$$V_{+NI} = V_{REF} \frac{R_4}{R_4 + R_1} + V_1 \frac{R_2}{R_2 + R_5}. \quad (6)$$

When the voltage at the inverting input (-NI) reaches the voltage value at the non-inverting input (+NI), the  $Q_1$  and  $Q_2$  transistors are blocked and voltage at non-inverting input drops to the following value:

$$V_{+NI} = V_{REF} \frac{R_4}{R_4 + R_1} + V_D \frac{R_2}{R_2 + R_5} \approx V_{REF} \frac{R_4}{R_4 + R_1} \quad (7)$$

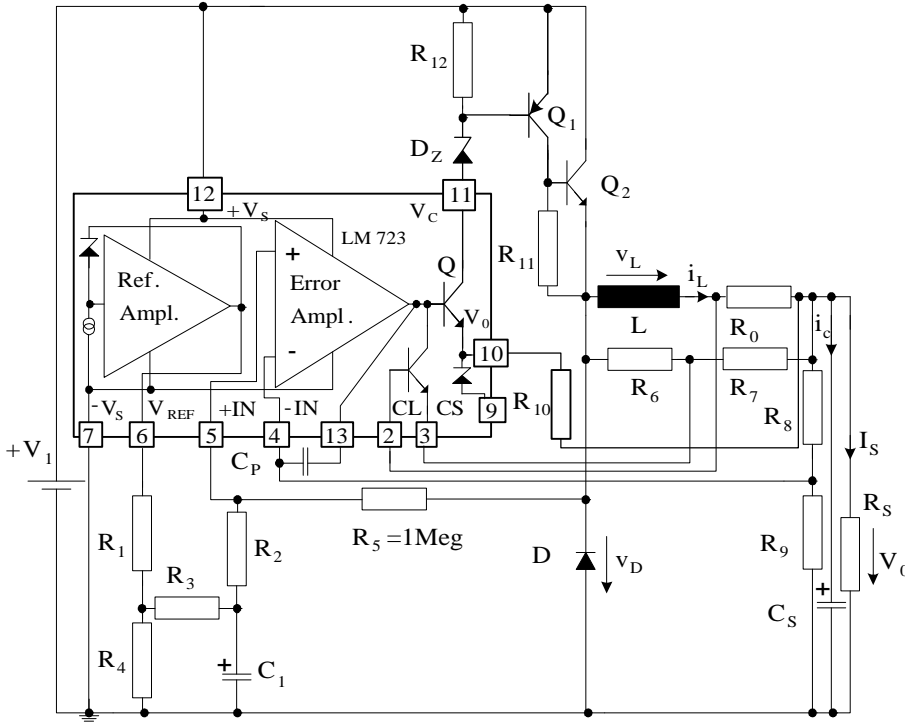


Table I. Specification

DC Voltage ( $V_1$ )	25~32[V]
$C_1$	10[uF]
$C_P$	10[nF]
$C_S$	470[uF]
$L$	300[uH]
$D$	MUR 1560
$D_Z$	1N4740
$Q_1$	BD140
$Q_2$	BUX47A
$R_1$	2.1[k $\Omega$ ]
$R_2$	1[k $\Omega$ ]
$R_3 = R_4$	5.1[k $\Omega$ ]
$R_5$	1[Meg $\Omega$ ]
$R_6 = R_8$	3.3[k $\Omega$ ]
$R_7$	33[ $\Omega$ ]
$R_9$	39[k $\Omega$ ]
$R_{10}$	220[ $\Omega$ ]
$R_{11}$	100[ $\Omega$ ]
$R_{12}$	1[k $\Omega$ ]
$R_0$	0.3[ $\Omega$ ]/5[W]
$R_S$	2~25[ $\Omega$ ]
Integrated Circuit	LM 723

Fig. 2. Hysteretic control voltage regulator using integrated circuit LM 723

From equations (6) and (7) we can notice that the load voltage ripple changes according to the following equation

$$V_{0ripple} = V_1 \frac{R_2}{R_2 + R_5} \quad (8)$$

Given that the value of the  $R_5$  resistance is much higher than the value of the  $R_2$  resistance, the value of the voltage ripple at the converter output is therefore dictated mostly by the  $R_5$  resistor.

### Simulation Results

The functioning of the circuit presented in Fig. 2 was studied by simulation, using programs designed for the analysis of power electronic circuits. The nominal values of the power sources and of the circuit components used for simulation, as well as for the experimental check, are presented in Table I.

Within these simulations, circuit elements were chosen from the simulation program libraries in accordance with the values indicated in Table I. For the simulation of transistors and diodes, we used circuit models instead of simplified controlled source models, with a view to obtaining a functioning behavior as close as possible to the real one.

The designed dc-dc converter insures a constant output voltage of  $V_0 = 5.3V$  and a maximum load current  $I_{Slim} \approx 3A$ , for an input voltage  $V_1$  varying between 25 and 32V. According to the data in Table I and to equation (7)

$$I_{Slim} = \frac{V_{R_0}}{R_0} = \frac{0.65}{R_0} + \frac{V_1 - V_0}{R_0} \frac{R_7}{R_7 + R_6} = \frac{0.65}{0.3} + \frac{32 - 5.3}{0.3} \frac{33}{3300 + 33} = 2.1 + 0.88 \approx 3A \quad (9)$$

Fig. 3 shows simulation results of  $V_0$  output voltage for two different values of the  $V_1$  supply voltage, 25V and 30V, respectively.

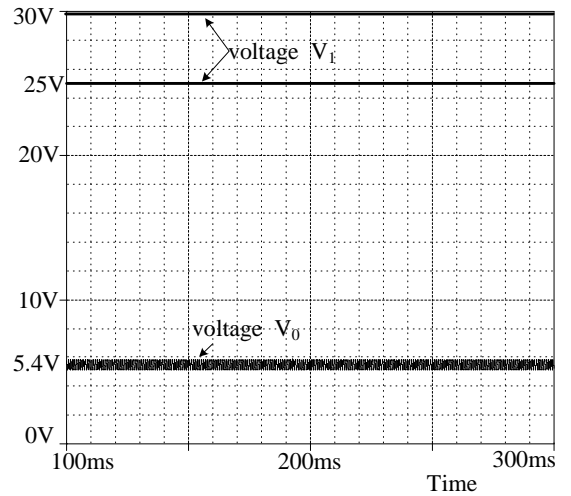
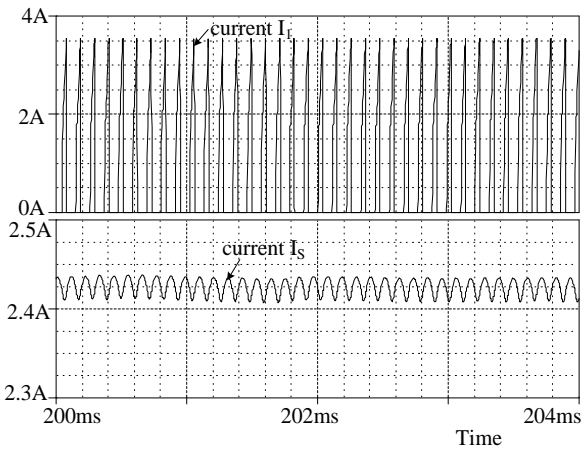


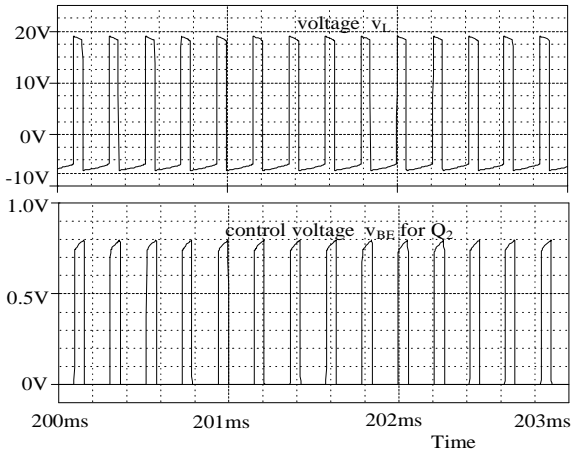
Fig. 3.  $V_1$  voltage waveforms and  $V_0$  voltage waveform

Fig. 4 shows simulation waveforms of the  $I_1$  current absorbed from the  $V_1$  power source and of the  $I_S$  load current for the load resistor  $R_S = 2.2[\Omega]$ .



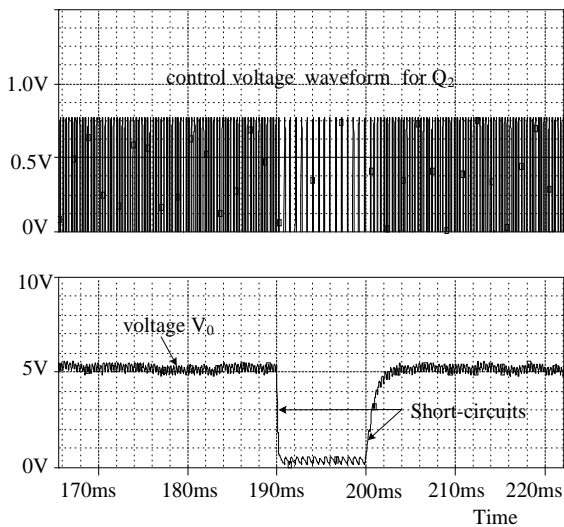
**Fig. 4.** Current waveform  $I_1$  and current waveform  $I_2$

Fig. 5 shows simulation waveforms of the  $v_L$  inductance voltage and of the  $Q_2$  transistor command signal.



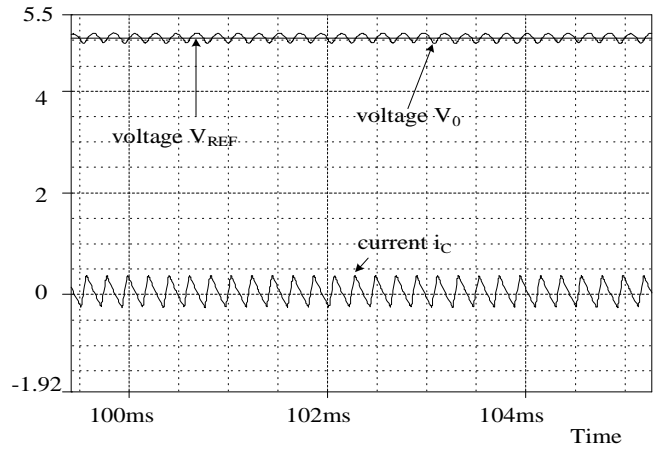
**Fig. 5.** Voltage waveform  $V_L$  and control voltage waveform for  $Q_2$

Fig. 6 shows simulation waveforms of the  $Q_2$  transistor command voltage and of the  $V_0$  output voltage when the load resistance is short-circuited.



**Fig. 6.** Control voltage waveform for  $Q_2$  and  $V_0$  voltage waveform when the circuit is protected against short-circuits

Fig. 7 shows simulation results of the  $V_0$  output voltage, of the  $V_{REF}$  voltage and of the  $C_S$  capacitor current for  $R_S = 15\Omega$ .

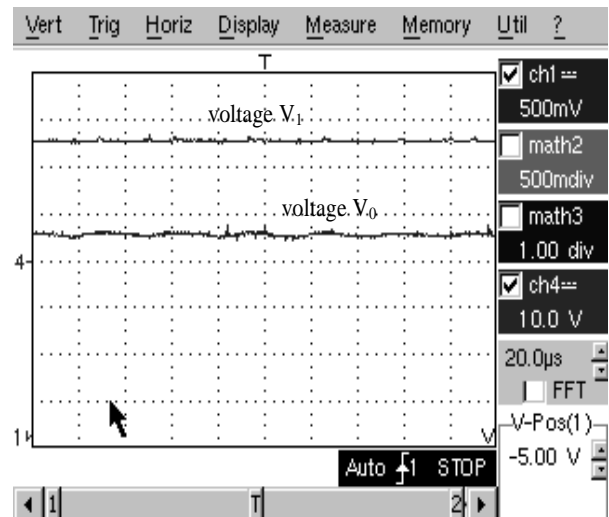


**Fig. 7.**  $V_{REF}$  voltage waveform,  $V_0$  voltage waveform and  $i_C$  current waveform

### Experimental Results

The circuit proposed in Fig. 2 was also tested experimentally. For its practical design, we used specifications and parameters presented in Table I.

Fig. 8 shows the oscilloscope waveforms of the supply voltage  $V_1$ -ch4/[10V/div] and of the load voltage  $V_0$ -ch1/[500mV/div].



**Fig. 8.** Experimental  $V_1$  and  $V_0$  voltage waveform

Fig. 9 shows oscilloscope waveforms of the current  $I_1$ -ch4[20mV/div-20mV/1A] absorbed from the power source  $V_1$ , and of the load current  $I_2$ -ch1[5mV/div-5mV/0.1A] for a load resistor  $R_S \approx 2.2\Omega$ .

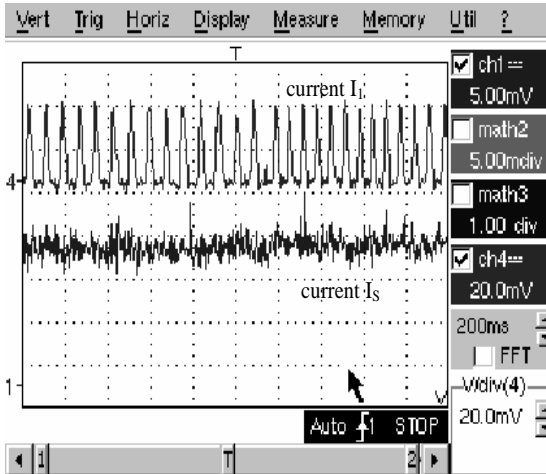


Fig. 9. Experimental  $I_1$  and  $I_5$  current waveform

Fig. 10 shows oscilloscope waveforms for the transistor command signal  $Q_2$ -ch1/[500mV/div] and for the inductance voltage  $v_L$ - ch4[10V/div].

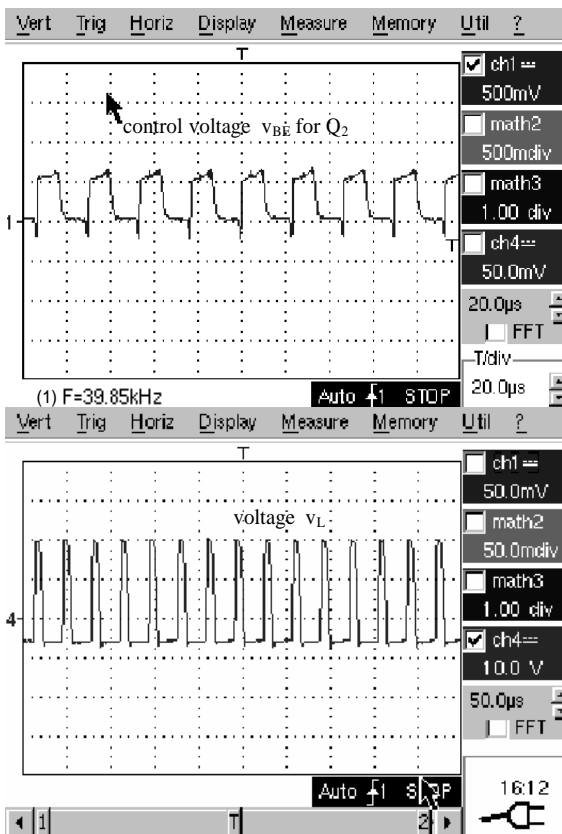


Fig. 10. Experimental control voltage waveform for  $Q_2$  and  $v_L$  voltage waveform

Fig. 11 shows oscilloscope waveforms of the transistor control voltage  $Q_2$  -ch4[500mv/div] and of the output voltage  $V_0$ -ch1[5V/div], when the load resistance is short-circuited.

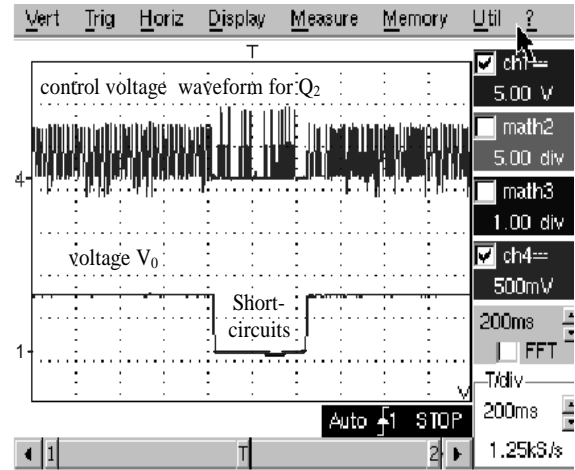


Fig. 11. Experimental control voltage waveform for  $Q_2$  and  $V_0$  voltage waveform when the circuit is protected against short-circuits

Fig. 12 shows oscilloscope waveform of the load voltage  $V_0$ -ch1/[1V/div] at “soft start” connection.

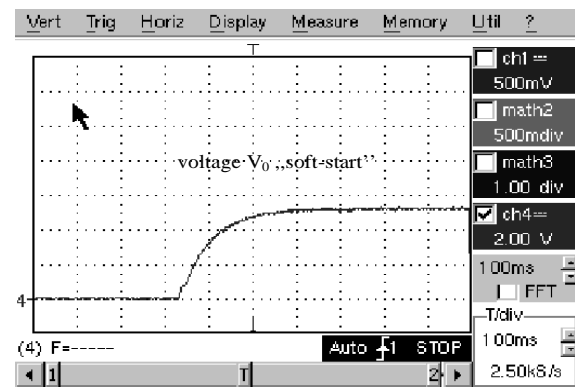


Fig. 12. Experimental  $V_0$  voltage waveform –“soft-start”

Fig. 13 shows oscilloscope waveforms of the output voltage  $V_0$ -ch1/[20mV/div] and of the  $i_C$  current through the capacitor  $C_S$ -ch4/[100mV/div].

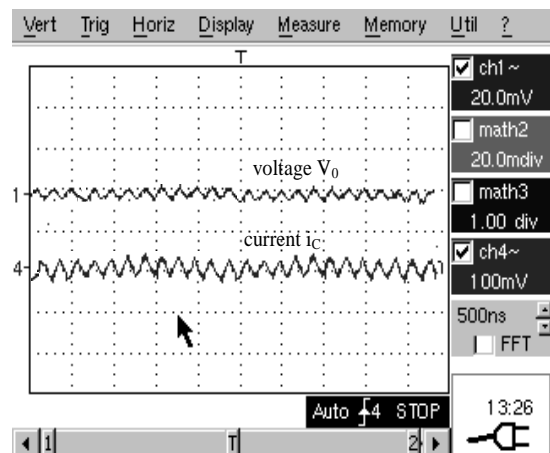


Fig. 13. Experimental  $V_0$  voltage waveform and  $i_C$  current waveform

Fig. 14 shows the efficiency evolution diagram in relation to the  $I_S$  load current variation for two different values of the supply voltage  $V_1=25\text{V}$  and  $V_1=30\text{V}$ , respectively, as well as the output voltage  $V_0=5.3\text{V}$ , which remains constant.

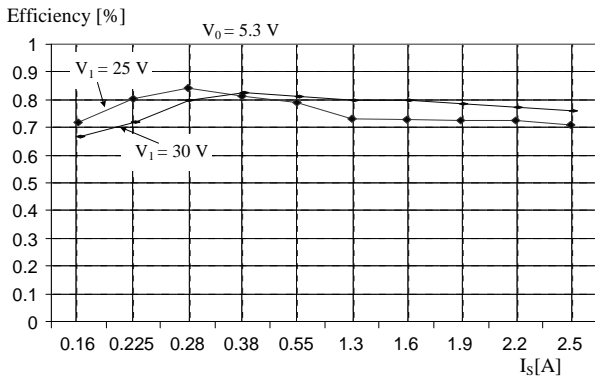


Fig. 14. Measured and calculated efficiency  $\eta$  [%] versus current output  $I_S$ , for constant output voltage  $V_0=5.3\text{V}$  and input voltage  $V_1=25\text{V}$  and  $V_1=30\text{V}$ , respectively

## Conclusions

The hysteretic power supply is simpler than the voltage- or current-mode closed-loop-control dc-dc switchers, although its simplicity may be a bit deceiving, due to component variations and potential sources of “injected” feedback voltage. Along with its simplicity, the hysteretic power supply is popular today for its low cost, inherently stable operation (there is no need to perform loop analysis), extremely fast load response time that requires no compensation, and suitability. The analysis carried out through simulations and experimental check proved and confirmed that the proposed circuit functions well.

The hysteretic controller IC is the key element in the conventional hysteretic power supply [11]. The hysteresis control method, implemented using IC LM723, allowed a low-cost design of the dc-dc converter, as well as high performance and multiple facilities (soft-start, protection against short-circuits, etc).

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The analysis and testing of a dc-dc converter by means of the hysteretic control method is presented. In order to design this control method, we used the LM723 integrated circuit, mostly used for the continuous control of the voltage and current sources. Experimental results, as well as simulation results, confirm that the circuit functions well. The proposed circuit represents an alternative for designing dc-dc converter control through the hysteresis method, without using specialized integrated circuits, with low costs and high performances. Il. 14, bibl. 11 (in English; summaries in English, Russian and Lithuanian).

O. Урсару, Ц. Агхион, М. Луцану. Управляемый регулятор напряжения с интегральной микросхемой LM723 // Электроника и электротехника. – Каунас: Технология, 2009. – № 7(95). – С. 45–50.

Описывается анализ и тестирование управляемого преобразователя постоянного тока. Равномерное управление параметрами источника напряжения и тока обеспечивается микросхемой LM723. Данную гистерически управляемую схему можно использовать как аналог других устройств. Предложенный вариант имеет наименьшую стоимость и высокую производительность. Ил. 14, библи. 11 (на английском языке; рефераты на английском, русском и литовском яз.).

O. Ursaru, C. Aghion, M. Lucanu. Histeriškaiai valdomas įtampos reguliatorius su integriniu grandynu LM723 // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2009. – Nr. 7(95). – P. 45–50.

Pristatoma histeriškaiai valdomo nuolatinės srovės keitiklio analizė ir testavimas. Tokio tipo valdymui įgyvendinti panaudotas integrinis grandynas LM723, kuriuo tolygiai valdomi įtampos ir srovės šaltiniai. Eksperimentiniai ir modeliavimo rezultatai patvirtina, kad grandynas funkcionuoja tinkamai. Galima teigti, kad siūlomas histeriškaiai valdomas grandynas gali būti naudojamas kaip alternatyva specializuotiems analogams, nes yra našus ir pigus. Il. 14, bibl. 11 (anglų kalba; santraukos anglų, rusų ir lietuvių k.).

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