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Investigation of p-i-n GaAs Structures by DLTS Method

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Introduction

The DLTS method is used for measuring of *p-n* structures, Schottky diodes etc. The *p-i-n* diodes are complicated multi layer structures, containing wide *i*-layer and two junctions: *n-i* and *p-i*. As a result, the scheme of such diode consist of two series capacities. Applied voltage is focused on *i*-layer and weakly modulates the space charge area in *n*- and *p*- layers. As a result, the „source" (technological layer) responsible for DLTS signal can not be definitely recognized. So it is difficult to estimate the deep levels concentration and determine the origin of the defects.

Nevertheless, at all DLTS spectrums any effective signals of deep levels connected with majority carriers can be recorded. Moreover, some weak signals that reflect the capture of minority carriers can be noted. The terms of experiment exclude the capture of minority carriers, therefore, the appearance of such signals could be connected with the injection of charge from contacts that confirm the complexity of samples for analysis.

Epitaxial-grown *p-i-n* layers in GaAs are relatively free of traps, except for levels A at EV +0,41eV and B at EV+0,68eV, present in concentrations of $5*10^{13}$-$5*10^{15}$ cm^{-3}. These two deep acceptor levels determine the minority carrier (hole) lifetime and the reverse recovery time of rectifiers respectively. The concentration of A and B traps have influence on the width of i-region and the location of *p-i-n* junction in epitaxial layer [1].

The main goal of the work is analytical review of DLTS spectra on commercial GaAs p^+-*pin*-n^+ structures to identify the deep level centers in –*pin*-region.

Device fabrication

For the experiments were used the GaAs p^+-*p-i-n*-n^+ structures fabricated in AS "Clifton", Tartu, Estonia. The schematic model of the device is shown in Fig. 1.

Fig. 1. The schematic picture of fast-acting GaAs diode

The liquid phase epitaxy (LPE) *p-i-n* structures were grown on the polished and etched *p*+ substrates, doped by Zn, 2 inches diameter, 450 μm thickness and orientation (111), Chohralsky grown. The substrates were purchased from CMK s.r.o., Gallium Arsenide Company, Slovakia.

The concentration of Zn doping in substrates was 5÷7E18 cm^{-3} and 1÷2E19 cm^{-3}. The epitaxy was fulfilled from solution of GaAs in Ga at temperatures 910°C and 920°C.

The n^+ layer was formed on the p^+-*pin*-*n* structures by separate LPE operation. The thickness of n^+ layer ~35μm. The p^+ surface of p^+-*pin*-n^+ structures was metalized by Ni and n^+ surface by combined AuGe/Au sputtering.
The plates with formed p^+-*pin*-n^+ structures were sectioned by 2x2 mm^2 and 3x3 mm^2 diode chips.

Experiments and discussion

During the experimental study were realized the following operating measurements:

- Current-voltage measurement – I-V;
- Capacitance-voltage measurement – C-V;
- Frequency Scan – FS;
- Temperature Scan – TS;
- Capture Cross Section measurement – CCS;
- Depth Profile measurement – DP.

DLTS (Deep Level Transient Spectroscopy) measurements were carried out by fully computer controlled deep level spectrometer DLS-83D (Semilab, Semiconductor Physics Laboratory, Inc., Hungary). The measurements were performed on the eleven commercial diode chips.

It was stated above that p^+-*pin*-n^+ is not quite suitable structure for DLTS measurement. The presence of two junctions (*p-i* and *n-i*) often give obstacles to simple direct identification of trap position. In some cases the grate hum noise makes it impossible to recognize the traps for some of the specimens. The traps situated in low doped area give the basic contribution in DLTS signal. In the same time, when *p-i*-junction is under reverse bias *n-i*-junction is not blocked and is the source of unintentional distortions that may completely smash the DLTS spectra (Fig. 2).

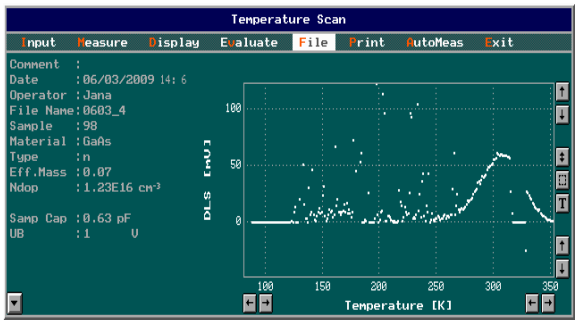

Fig. 2. The distorted DLTS spectra

The measurements were carried out under reverse biased voltage from -4V to -20V relating to p^+-*p*-*i* junction. Such polarity realizes the most asymmetrical model of junction, where the space charge is spread in depletion *p*-*i*-*n* zone. The barrier capacitance depends on the width of *i*-zone and whole *p*-*i*-*n* region width (Table 1).

Table 1. Dependence of barrier capacitance on *p*-*i*-*n* width

***p*-*i*-*n* width (μm)**	**C@U=0 (pF)**
50-14-50	7,82
50-14-50	9,11
50-14-50	14,1
43-17-103	21,32
43-17-105	21,51
45-17-100	22,83
50-17-87	28,75
20-14-13	304,19
20-14-13	328,79

The typical picture of the spectra for most of the samples gives the reliable possibility to estimate the level depth, concentrations and capture cross section of the traps.

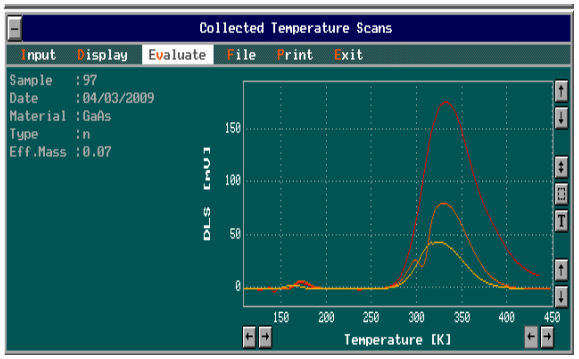

Fig. 3. The conventional DLTS temperature scan measurement

For all the specimens the position of the picks coincides from spectra to spectra (Fig. 3) and experimental Arrhenius plots be compared with library dates (Fig. 4) give the levels most close to L2 and L5, which Martin, Mitonneau and Mircea [2] connect with A and B centers.

All traps demonstrates the high temperature dependence of emission rate and capture cross section (Fig. 5, Fig. 6).

The emission rate e_n depends very much on the temperature. As appears from the equation (1) both the thermal velocity and effective density of states are temperature dependent and temperature can be found in exponential term too.

$$e_n = V_{th}\sigma n e^{-(E_c - E_t)/kT}\ , \qquad (1)$$

where $V_{th} = \sqrt{\frac{3kT}{m_{eff}}}$ – thermal velocity; σ – capture cross section; n – free carriers concentration; E_c – bottom of conduction band; E_t – trap level.

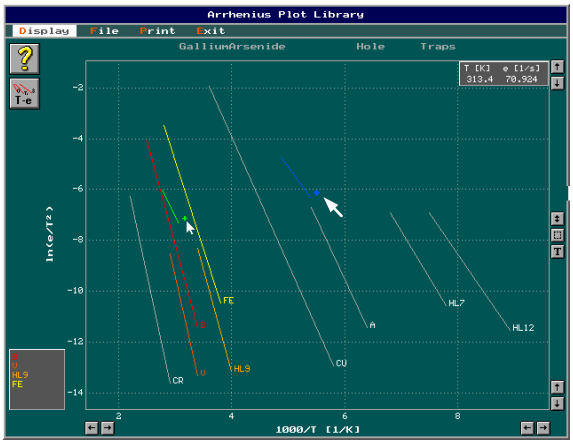

Fig. 4. The library of Arrhenius plots and position of measured points (experimental results are marked by arrows)

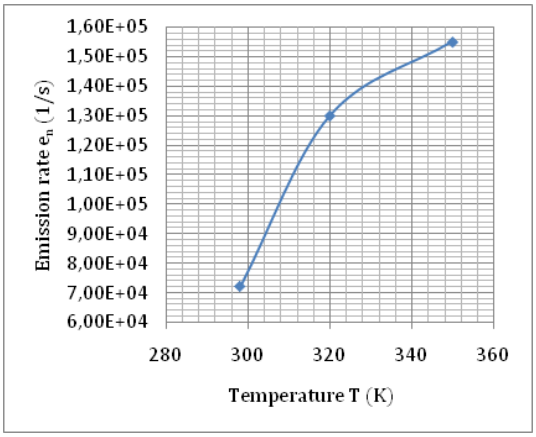

Fig. 5. The temperature dependence of emission rate

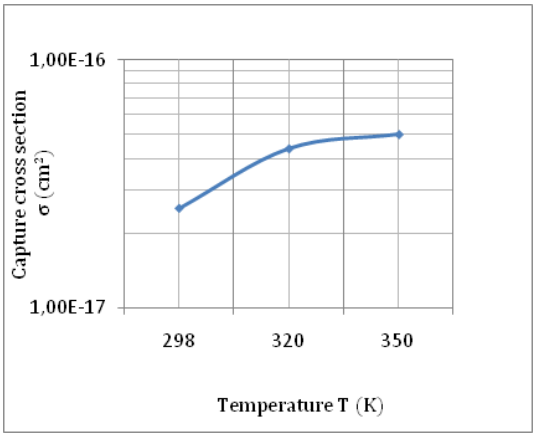

Fig. 6. The temperature dependence of capture cross section

At the same time the temperature rise stimulates the thermal generation of free carriers. The increase of carriers concentration lead to decrease of capture cross section (equation 2).

$$\sigma = \frac{1}{\tau_c n V_{th}}, \qquad (2)$$

where τ_c – time constant of the capture process (see the diminution of the process in Fig. 5, Fig. 6). These two contrary processes compensate each other and as a result we have the temperature stability of dynamic characteristics that is the specific of GaAs devices.

The depth profiling measurements for all the specimens always give the steady picture, when in quite narrow region close to p^+-*p*-*i*-*n* junction are observed the heightened concentration of the traps (Fig. 7). Then, on the distance of ~0,25μm from the junction the profile curve slopes to the "normal" level of trap concentration, which is in good correlation with the concentrations given by other operation measurements. Now we can't give the explanation to such behavior and can only fix it as a fact.

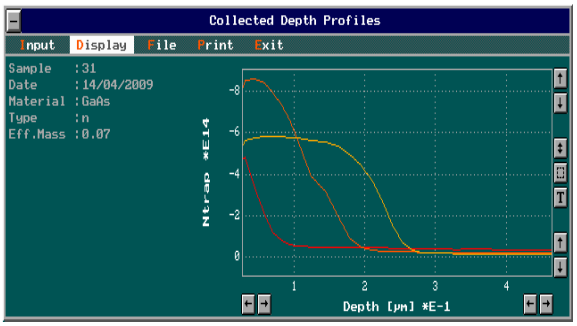

Fig. 7. The typical picture of depth profile measurement for different resolution

Conclusion

During the DLTS measurements we have found all the difficulties, which were expected for GaAs p^+-*pin*-n^+ structures. We were fully aware of the fact that structures are not good for measurements. Never the less most of the samples placed in disposal gave steady picks in DLTS spectra. And in many cases, under the proper task statement the analytical study of p^+-*pin*-n^+ objects is possible. At the same time for the firm belief of the results we suggest the following of experiments. First, the p^+-*pin*-n^+ chips, cut out from one and the same maternal plate are to be modified in accordance to the schemes as shown in Fig. 8. Then in consecutive order each kind of specimen is going to be measured by DLTS method.

The trap parameters measured in Schottky model we accept for more reliable. Then we can observe the consecutive mutation of trap parameters from one model to another. The results obtained by such experiment will give possibility to draw up the correction factors or transient functions as a pass from ideal Schottky specimen to variable *p*-*i*-*n* models.

These series tests made in wide interval of technological conditions will get us the steady potentiality for direct DLTS measurements on p^+-*pin*-n^+ structures.

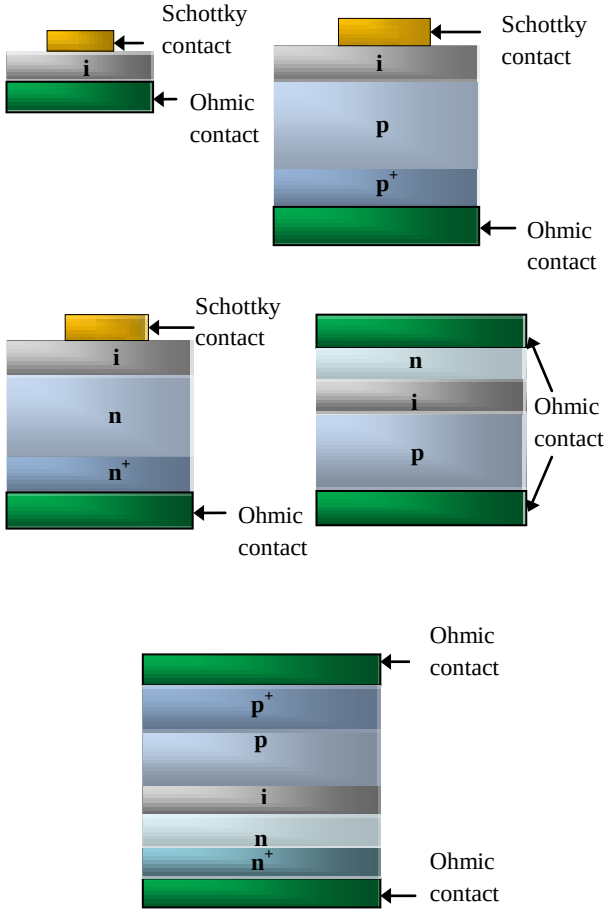

Fig. 8. The schemes of modified models of *p*-*i*-*n* for DLTS measurements

So there is the possibility to make the following conclusion. For more precise identification of defects in *p*-*i*-*n* diodes structural layers it is necessary to carry out separate analysis on more simple test structures, each of all is formed on fixed technological layer and is represented either by p-n junction or by Schottky diode.

Acknowledgment

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References

1. **Voitovich V.** LPE structures for power GaAs rectifiers // Proceedings BEC–2000. – Tallinn, 2000. – P. 237–240.
2. **Mitonneau A., Martin G. M., Mircea A.** Hole traps in bulk and epitaxial GaAs crystals // Electronics Letters. – 1977. – Vol. 13. – P . 666–668.

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J. Toompuu, O. Korolkov, N. Sleptšuk, T. Rang. Investigation of p-i-n GaAs Structures by DLTS Method // Electronics and Electrical Engineering. – Kaunas: Tehnologija, 2010. – No. 4(100). – P. 51-54.

The main goal of the work is the interpretation of DLTS (Deep Level Transient Spectroscopy) spectra measurements on commercial GaAs p^+-*p*-*i*-*n*-n^+ structures to identify the deep level centers and their properties in *p*-*i*-*n* region. The experimental study operates the measurements of I-V and C-V relationships. The frequency and the temperature scan have been included. And finally, the capture cross section and depth profile measurements have been accomplished. For all the specimens the positions of the picks coincide from spectra to spectra and give the levels most close to A and B centers. During analytical review was determined the following dependences: barrier capacitance dependence on *p*-*i*-*n* width, the temperature dependence of emission rate, the temperature dependence of capture cross section. In the conclusion was made the suggestion that for more precise identification of defects in *p*-*i*-*n* diodes structural layers it is necessary to carry out separate analysis on more simple test structures. Ill. 8, bibl. 2, tabl. 1 (in English; abstracts in English, Russian and Lithuanian).

Я. Тоомпуу, О. Корольков, Н. Слепчук, Т. Ранг. Исследование p-i-n GaAs структур методом DLTS // Электроника и электротехника. – Каунас: Технология, 2010. – № 4(100). – С. 51–54.

Основной целью работы является интерпретация DLTS (Deep Level Transient Spectroscopy) спектров замеренных на промышленных GaAs p^+-*p*-*i*-*n*-n^+ структурах для идентификации глубоких уровней и их параметров в *p*-*i*-*n* области. В экспериментальной части рассмотрены соотношения I-V и C-V характеристик, проведено частотное и температурное сканирование, определены сечение захвата и профиль концентрации ловушек. Позиции пиков $\Delta C/C$ замеренных на различных образцах совпадают, а их параметры наиболее близки A и B центрам. В аналитическом обзоре представлены зависимости барьерной ёмкости от ширины *p*-*i*-*n* области, а также температурные зависимости скорости эмиссии и сечения захвата глубоких уровней. В заключительной части представлены модели тестовых структур и схема проведения эксперимента для более точного и надежного определения глубоких уровней методом DLTS в p^+-*p*-*i*-*n*-n^+ структурах. Ил. 8, библ. 2, табл. 1 (на английском языке; рефераты на английском, русском и литовском яз.).

J. Toompuu, O. Korolkov, N. Sleptšuk, T. Rang. Gilių lygmenų talpinės spektroskopijos metodo taikymas p-i-n GaAs struktūroms tirti // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2010. – Nr. 4(100). – P. 51–54.

Giluminių *p*-*i*-*n* sričių centrams nustatyti ir jų savybėms tirti taikomas giliųjų lygmenų talpinės spektroskopijos GaAs p^+-*p*-*i*-*n*-n^+ struktūrose metodas. Eksperimentiškai tai galima atlikti matuojant I-V ir C-V charakteristikas įvertinant skenavimo dažnį bei temperatūrą ir atliekant struktūrų skerspjūvio ir gylio profilių matavimus. Taikant spektroskopiją daug dėmesio skiriama gautų spektrų pikams. Atlikus gautų rezultatų analizę nustatyta slenkstinės talpos priklausomybė nuo *p*-*i*-*n* srities pločio, taip pat emisijų greičio ir priemaišų pasiskirstymo giliuose sluoksniuose temperatūrinės priklausomybės. Pateikti bandytų struktūrų modeliai. Taikant giliųjų lygmenų talpinės spektroskopijos metodą giluminėms p^+-*p*-*i*-*n*-n^+ sritims tiksliau ir patikimiau tirti, būtina atlikti papildomą analizę su paprastesnėmis struktūromis. Il. 8, bibl. 2, lent. 1 (anglų kalba; santraukos anglų, rusų ir lietuvių k.).