

## An Analog Array Approach to Variable Topology Filters for Multi-mode Receivers

**D. Csipkes, G. Csipkes, S. Hintea**

*Technical University Cluj-Napoca,  
 Memorandumului 1, Romania, phone: +400264401463, e-mails: doris.csipkes@bel.utcluj.ro, gabor.csipkes@bel.utcluj.ro, sorin.hintea@bel.utcluj.ro*

**H. Fernandez-Canque**

*Glasgow Caledonian University,  
 Cowcaddens Road, Glasgow G4 0BA, United Kingdom, e-mail: h.fernandez@gcu.ac.uk*

### Introduction

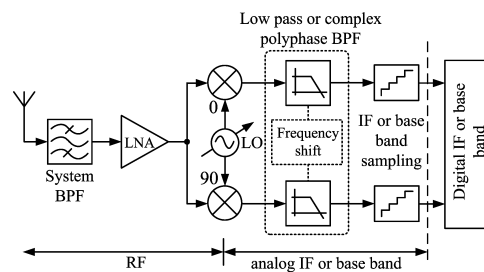
Recent development of the communication industry imposes new challenges on the design of wireless terminals. The ever increasing diversification of services has led to more and more complicated equipments, supporting extended functionality. The digital section of wireless terminals greatly benefits of the advantages offered by the rapid advancement of semiconductor technologies. Miniaturization allowed an increasing complexity and higher operating frequencies, leading to better performance and more integrated functionality of digital circuits. Therefore, digital processors and their driving software can relatively easily cope with the demands of modern multi-mode wireless technologies [1].

Traditionally the bottleneck in the development of mixed signal IC-s has been the analog interface. Along with the increasing digital functionality, analog circuits must support extensive reconfiguration, not only to adapt to the processed signal characteristics, but also to deal with various environmental effects, variable supply voltages, fabrication tolerances and a wide range of operating temperatures specific to portable equipments [2, 3].

Among the multitude of multi-mode wireless front end architectures proposed in the literature two really stand out: the zero-IF or direct conversion and the low-IF architectures. Direct conversion front ends have been typically used for fixed frequency systems due to their predictable, well known behavior and low component count. This architecture is flawed by DC offset that may be difficult to compensate when narrow bandwidth signals are processed. The low-IF architecture emerged as an alternative to zero-IF, eliminating the DC offset issues by converting the signal to some low intermediate frequency instead of the base band. However, channel or band selection has become more tedious due to the demand to suppress image signals. Reconfigurability exacerbates

these problems through variable carrier frequencies and different signal dynamics, specific to each supported communication standard.

A possible solution supporting wide band reconfigurability would be to combine the two architectures and emphasize the advantages depending on the characteristics of the processed signals. The block diagram of a low-IF-zero-IF multi-mode front end is shown in Fig. 1.



**Fig. 1.** Block diagram of a reconfigurable low-IF/zero-IF analog front end

The variable LO allows the conversion to various intermediate frequencies, including the base band. The channel or band select filter may be switched from a low pass to a polyphase band pass type of frequency response in order to accommodate the changes of the architecture and the target center frequency. Sampling may occur at the IF or in the base band. The reconfigurable filter is one of the key components in this architecture, being directly responsible for the receiver selectivity. The remainder of this paper describes an analog array approach to variable topology filters, suitable for multi-mode wireless applications.

### CCII filter implementation techniques

With the continuous reduction of supply voltages,

conventional voltage mode design techniques show their inherent limitations, being more and more often replaced by current mode signal processing. In many applications current mode circuits offer a reasonable trade-off between signal amplitude, bandwidth, linearity, complexity and current consumption. Two of the most widely used fundamental building blocks in current mode signal processing are the operational transconductance amplifier (OTA) and the second generation current conveyor (CCII). The latter is often preferred for its versatility in operation. The CCII cell typically has one high impedance voltage input (Y), one low impedance current input (X) and one or more high impedance current outputs. The operation can be briefly described by (1):

$$\begin{cases} I_Y = 0, \\ V_X = V_Y, \\ I_Z = \pm \alpha \cdot I_X. \end{cases} \quad (1)$$

where  $\alpha$  is a current scaling factor.

CCII based current mode filters can be synthesized either by using the voltage-current duality principle, or by directly implementing the functional equations defined by the imposed attenuation characteristics. Two main synthesis methods are widely used in practice, fulfilling most demands, architecturally and performance wise.

The first method employs a cascade of elementary second order sections to build higher order filters. These biquads can be obtained by applying the duality principle to classical opamp-RC filters. Typical, double output CCII (DOCCII) based implementations of the Tow-Thomas (TT) and the Kerwin-Huelsman-Newcomb (KHN) biquads are illustrated in Fig. 2.

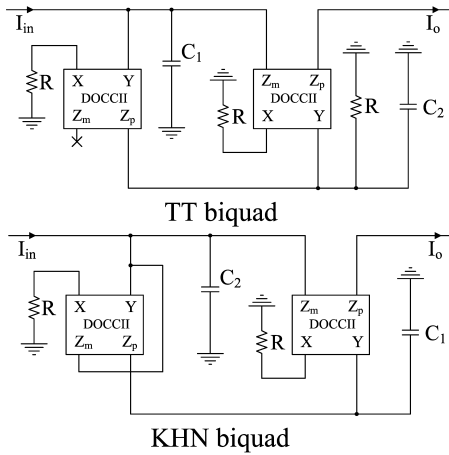


Fig. 2. The DOCCII based TT and KHN second order filters

Both biquads share the same transfer function, given in (2)

$$H(s) = \frac{1}{s^2 + \frac{1}{RC_2}s + \frac{1}{R^2C_1C_2}}. \quad (2)$$

Biquads are mostly used in modular designs with moderate filter orders. However, the implementation of

arbitrary transmission zeros can be tedious and the sensitivity performance of the filters decreases with the filter order. The second synthesis method, based on the functional simulation of a low pass ladder prototype, leads to a filter architecture that can easily support transmission zeros and inherits the sensitivity of doubly matched LC ladder filters. The modular implementation of a current mode leap-frog filter starts with the passive prototype and its associated signal flow graph, in which all state variables have been written as currents. The generalized odd order ladder prototype with transmission zeros is given in Fig. 3. The even order ladder is very similar, but the impedance  $Z_{2n+1}$  and the capacitance  $C_{z2n}$  are missing.

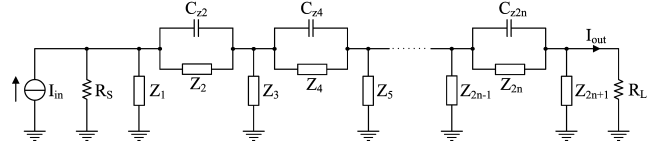


Fig. 3. The generalized, odd order passive ladder prototype

The functional equations may be written as shown in (3), where  $R$  is the characteristic resistance of the network, while the currents  $\hat{I}$  have been obtained from node voltages through resistive scaling.

$$\begin{cases} \hat{I}_1 = \frac{R_S \parallel Z_1}{R} \cdot [I_{in} - I_2 + sC_{z2}(V_1 - V_3)], \\ I_2 = \frac{R}{Z_2} \cdot (\hat{I}_1 - \hat{I}_3), \\ \hat{I}_3 = \frac{Z_3}{R} \cdot [I_2 - I_4 + sC_{z2}(V_1 - V_3) - sC_{z4}(V_3 - V_5)], \\ \vdots \\ I_{2n} = \frac{R}{Z_{2n}} \cdot (\hat{I}_{2n-1} - \hat{I}_{2n+1}), \\ \hat{I}_{2n+1} = \frac{Z_{2n+1}}{R} \cdot [I_{2n} - I_{out} + sC_{z2n}(V_{2n-1} - V_{2n+1})] \end{cases} \quad (3)$$

The recursive equations show that the terms  $sC_{z2k} \Delta V$  correspond to currents extracted or injected into adjacent circuit nodes. Since these terms already represent state variable currents, there is no need to scale them with the characteristic impedance of the network. The corresponding signal flow graph of the generalized filter is illustrated in Fig. 4.

For filtering in multi-mode wireless front ends only low pass transfer functions are of interest. In this case, odd order impedances are capacitors and even order impedances are inductors. From (3) results that in the final filter structure inductive impedances will be inverted (e.g.  $R/Z_2$ ). As a consequence, all the reactive elements in the active current mode filter will be capacitances and no electronic emulation of inductances is required. Fig. 5 shows the DOCCII based implementation of the odd order current mode leap-frog filter. The even order version can be easily obtained by eliminating the final DOCCII and the attached  $C_{z2n}-C_{2n+1}$  capacitors. Furthermore,  $I_{2n}$  becomes the output current.

Classical band pass filters can be implemented by means of a bilinear frequency transformation performed on a normalized low pass prototype. The transformation translates the low pass frequency response into a double side band characteristic that passes the wanted signal along

with its mirror image at both positive and negative frequencies. Therefore, these filters are not suitable for low-IF front end architectures where the suppression of the image signals is usually compulsory.

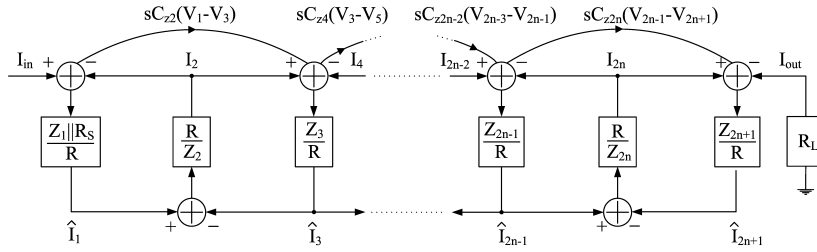


Fig. 4. The signal flow graph of the generalized state variable filter

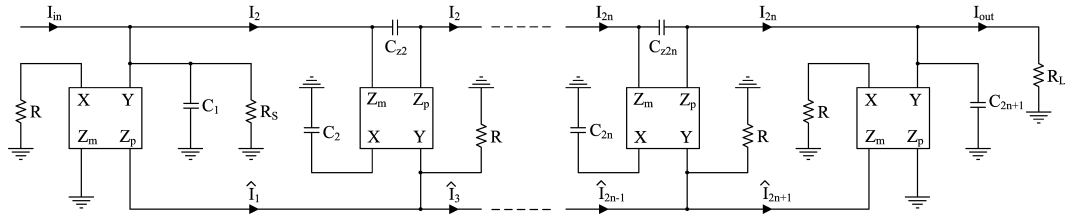


Fig. 5. Current conveyor based implementation of the generalized leap-frog filter

A single sideband response can be obtained by performing a linear frequency transformation according to (4) where  $\omega_C$  is the desired center frequency. The bandwidth of the filter is calculated by doubling the original low pass cut-off frequency [11].

$$s = j\omega \rightarrow s^* = j\omega \pm j\omega_C. \quad (4)$$

It can be seen that the transformation is performed on the frequency variable  $\omega$  and it only affects the capacitors in the low pass prototype. Each capacitor will be connected in parallel with a complex impedance according to (5).

$$j\omega C \rightarrow j\omega C \pm j\omega_C C. \quad (5)$$

The complex impedance  $j\omega C$  can be readily implemented if quadrature signal paths are available. This is usually the case in low-IF receivers. The block diagram of the linear frequency shifting circuit is shown in Fig.6. Note that a proper frequency transformation also shifts the longitudinal capacitors if arbitrary transmission zeros are present in the filter transfer function [10].

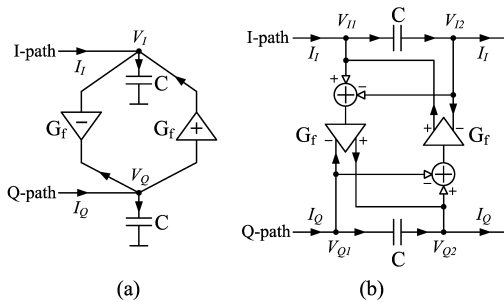


Fig. 6. Frequency shifted (a) grounded and (b) floating capacitor

In both cases the complex input impedance of the quadrature network and the value of the conductance  $G_f$  are given by (6).

$$Z = \frac{1}{j\omega C \pm jG_f} = \frac{1}{j\omega C \pm j\omega_C C} \Rightarrow G_f = \omega_C C. \quad (6)$$

Fig. 7 shows the implementation of the block diagrams from Fig. 6 with CCII cells.

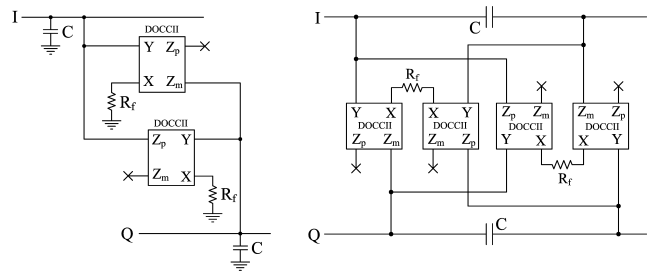


Fig. 7. DOCCII based linear frequency shift network for grounded and floating capacitors

The following paragraph describes an analog array based on DOCCII-s that support the implementation of all the filter types presented above [8, 9].

### The DOCCII based FPAA

Traditional FPAA architectures have been based on crossbar type signal routing [4]. In this concept, the configurable analog blocks (CABs) are considered the nodes of a regular matrix and can be freely interconnected through horizontal and vertical signal paths. The routing between these paths is implemented with omnidirectional switch arrays. Many of these applications have been built

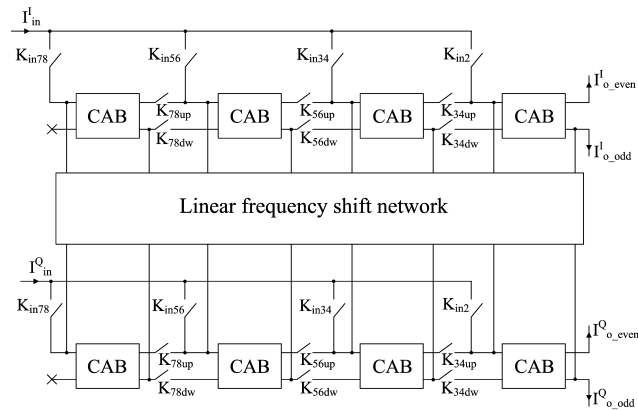
for rapid prototyping of analog functions. Therefore, a wide variety of basic operations, such as amplification, filtering and multiplication is supported by each CAB [5].

The FPAA proposed in this paper has been developed specifically for filtering applications. The architecture of the system and of each individual CAB has been derived by observing peculiarities common to typical, fixed topology filter design techniques and synthesis methods. The resulting FPAA is based on CABs connected in a reconfigurable cascade. A programmable signal bus, used as a demultiplexer, allows the injection of the current mode input signal into various nodes of the circuit, depending on the desired filter order [6, 7].

The chain of CABs, together with the input signal bus, support the implementation of a low pass filter based either on a cascade of second order sections, or on a leap-frog state variable topology. The latter is particularly useful for implementing filters with arbitrary transmission zeros and enhanced sensitivities at higher filter orders. The low pass filter order can be reconfigured to any value between 2 and 8 according to the imposed attenuation template.

In many cases target applications, such as the analog front ends in wireless receivers, impose a band pass filter capable of selectively suppressing image signals at positive or negative frequencies. These circuits are typically implemented as complex polyphase filters that require the replication of the low pass prototype on the quadrature signal path and a linear shift of the low-pass frequency response. The proposed FPAA supports the implementation of complex filters, derived from any prototype realized by the low pass chain of CABs. The frequency transformation is based on the circuits in Fig. 7.

The resulting architecture of the FPAA is illustrated in Fig. 8.



**Fig. 8.** General architecture of the proposed current mode FPAA

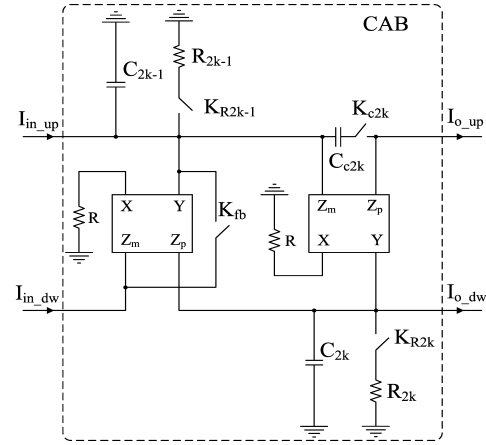
The switch network supports the mapping of individual filters on the array according to Table 1. This table shows the switch position for the leap-frog topology of different orders. Since second order sections require only local feedback and a single connection to the following CAB, all switches corresponding to the "down" signal path are in OFF state if this synthesis technique is considered. The other switches will be configured identically, while the output signal is always taken from  $I_{o\_even}$  or  $I_{o\_odd}$ .

**Table 1.** Switch states depending on filter type and order

Order	2	3	4	5	6	7	8
$K_{in2}$	ON						
$K_{in34}$		ON	ON				
$K_{in56}$				ON	ON		
$K_{in78}$						ON	ON
$K_{34up}$		ON	ON	ON	ON	ON	ON
$K_{34dw}$		ON	ON	ON	ON	ON	ON
$K_{56up}$				ON	ON	ON	ON
$K_{56dw}$				ON	ON	ON	ON
$K_{78up}$						ON	ON
$K_{78dw}$						ON	ON

The linear frequency shift network is connected between the two low pass replicas only if a band pass transfer function is required.

The internal structure of a CAB has been defined in order to support the implementation of any biquad from Fig. 2 and a complete up-down section of the leap-frog filter in Fig. 5. The schematic of the CAB is given in Fig. 9.



**Fig. 9.** Structure of a single CAB within the FPAA

The switches  $K_{R2k-1}$  and  $K_{R2k}$  serve the realization of termination resistors in leap-frog filters when CABs are first or last in the chain, or of the resistors required by the biquads of Fig. 2 and a lossy integrator. The switch  $K_{fb}$  is used to connect the local feedback path around the first DOCCII in KHN biquads, while  $K_{C2k}$  inserts a transmission zero in the filter transfer function. Table 2 shows the position of specific switches within the CAB for different basic configurations.

**Table 2.** Switch states within the CAB according to the filter type

Synthesis	$K_{R2k-1}$	$K_{R2k}$	$K_{fb}$	Output
TT biquad		ON		$I_{o\_up}$
KHN biquad			ON	$I_{o\_up}$
lossy integrator	ON			$I_{o\_dw}$
leap frog (LF)				$I_{o\_up} + I_{o\_dw}$
LF input	ON			$I_{o\_up} + I_{o\_dw}$
LF output (even)		ON		$I_{o\_up}$
LF output (odd)	ON			$I_{o\_dw}$

## Simulation results

The operation of the FPAA for various filter configurations and approximations has been validated through

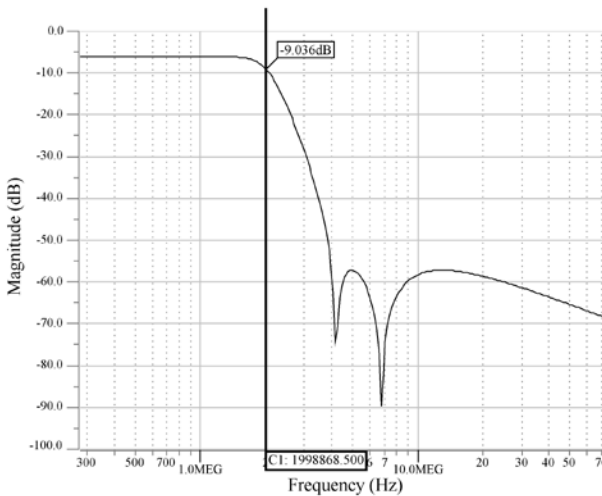
simulations performed in the Eldo simulator provided by Mentor Graphics. The DOCCIs have been modeled with controlled sources. The models include first order non-idealities, such as a frequency dependent transfer function, finite output resistance and non-zero input resistance at the conveyor X terminals.

The first filter example shown in this section is a 5<sup>th</sup> order low pass filter with inverse Chebyshev approximation built upon the leap-frog topology. The filter has been designed for a 2MHz cutoff frequency and a stopband ratio equal to 2. The input current is injected to the CAB2, while the output signal is taken from  $I_{o-dw}$  of the CAB4. The resistor  $R_{2k-1}$  in CAB2 implements the source resistance and  $R_{2k}$  in CAB4 the termination of the ladder. The switch positions in each CAB are summarized in Table 3. The overall configuration of the switches in the FPAA can be taken from Table 1 for a 5<sup>th</sup> order filter.

**Table 3.** CAB switch configuration for the first filter example

	$K_{C2k}$	$K_{R2k-1}$	$K_{R2k}$	$K_{fb}$	Output
CAB1					
CAB2	ON	ON			
CAB3	ON				
CAB4		ON			$I_{o-dw}$

The simulated magnitude response of the filter and the measure -3dB cutoff frequency are illustrated in Fig.10.



**Fig. 10.** The simulated low pass magnitude response of the FPAA for an inverse Chebyshev approximation

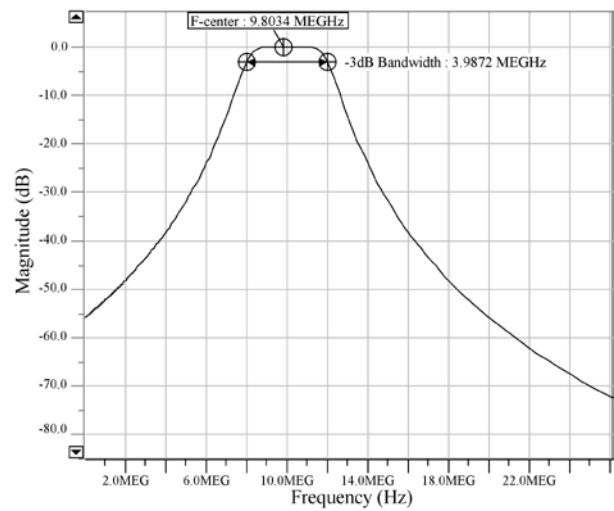
The second example is a 4<sup>th</sup> order complex band pass filter with Butterworth approximation. The filter has been built with a cascade of two Tow-Thomas second order sections. The required bandwidth was 4MHz, while the magnitude response was centered on 10MHz. The configurations of the switches within each CAB and the entire FPAA can be determined from Table 1 and Table 4, similarly as for the previous example. Additionally, the frequency shift network performs the linear low pass to band pass transformation for each of the four capacitors connected into the circuit.

Fig. 11 illustrates the simulated band pass magnitude response of the filter. The measurements show the imposed 10MHz center frequency and 4MHz bandwidth.

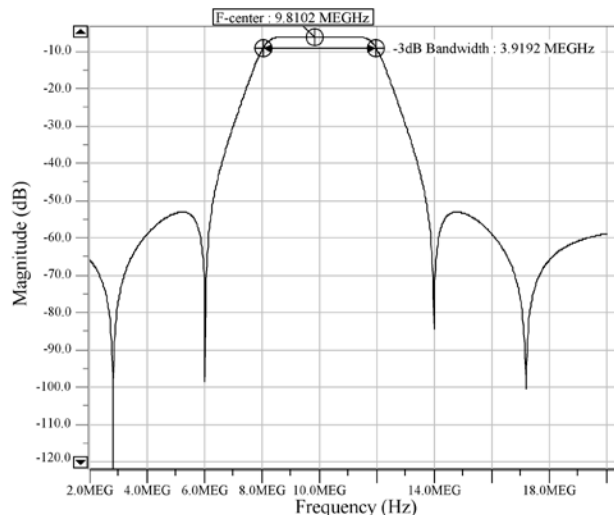
**Table 4.** CAB switch configuration for the second filter example

	$K_{C2k}$	$K_{R2k-1}$	$K_{R2k}$	$K_{fb}$	Output
CAB1					
CAB2					
CAB3			ON		
CAB4			ON		$I_{o-up}$

The third example is a complex band pass filter whose low pass prototype has been presented in the first example. The inverse Chebyshev low pass transfer function has been shifted to a 10MHz center frequency while the 2MHz cutoff frequency yields a 4MHz bandwidth. The switch configurations are identical with the low pass prototype but the frequency shift network is also connected between I and Q signal paths. Fig. 12 shows the simulated magnitude response of the filter and the measured frequency parameters.



**Fig. 11.** The simulated band pass magnitude response of the FPAA for a Butterworth approximation



**Fig. 12.** The simulated band pass magnitude response of the FPAA for an inverse Chebyshev approximation

## Conclusions

This paper investigated the system level aspects of

using a dedicated analog array approach to reconfigurable filter design with applications in future communication systems such as software defined radio and cognitive radio. The proposed signal bus based architecture, combined with a filtering oriented CAB design is different from regular, multi-purpose FPAA-s used in rapid prototyping of analog functions.

The FPAA can accommodate to variable filter topologies in order to optimize the selectivity depending on the spectral characteristics of the processed signal. The filters mapped onto the array can be configured for orders variable between 2 and 8 and different synthesis methods, including the functional simulation of ladder filters and a cascade of second/first order sections. Furthermore, the selectivity can be enhanced by using approximations with arbitrary transmission zeros. The analog array supports the reconfiguration of low pass transfer functions into complex band pass responses, often used in low-IF receivers along with quadrature signal processing.

The fundamental building block of the array is a CAB based on current conveyors, allowing current mode signal processing, as a potential candidate for low voltage applications

All the possible configurations have been extensively simulated in Eldo. The functional building blocks have been implemented at system level with first order non-idealities. The complete transistor level implementation of the circuits is the subject of current research.

#### Acknowledgements

The authors wish to thank CNCSIS Romania (National Council for Research and Higher Education) for the financial support (grant no. 657/2009). Special thanks to Mentor Graphics for providing software and financial help with our research and publications.

#### References

1. **Cafaro G., Correal N., Taubenheim D., Orlando J.** A 100 MHz–2.5 GHz CMOS // *Transceiver in an Experimental*

*Cognitive Radio System, SDR Forum Technical Conference, 2007.*

2. **Eidukas D., Kalnius R.** Two-Parameter Electronic Devices Quality Models // *Electronics and Electrical Engineering.* – Kaunas: Technologija, 2010. – No. 7(103). – P. 3–8.
3. **DAmico S., Gianini V., Baschiroto A.** A Low-Power Reconfigurable Analog Filter for UMTS/WLAN Receivers // *Proceedings of Norchip Conference, 2004.* – P.179–182.
4. **D'Mello D. R., Gulak P. G.** Design Approaches to Field-Programmable Analog Integrated Circuits // *Journal on Analog Integrated Circuits and Signal Processing, 1998* – Vol. 17. – P. 7–34.
5. **Becker J., Henrici F., Trendelenburg S., Ortmanns M., Manoli Y.** A Hexagonal Field Programmable Analog Array Consisting of 55 Digitally Tunable OTAs // *International Symposium on Circuits and Systems (ISCAS), 2008.* – P. 2897–2900.
6. **Pankiewicz B., Wojcikowski M., Szczepanski S., Sun Y.** A Field Programmable Analog Array for CMOS Continuous-Time OTA-C Filter Applications // *IEEE Journal of Solid-State Circuits, 2002.* – Vol. 37. – P. 125–136.
7. **Premont C., Grisel R., Abouchi N., Chante J.P.** Current-Conveyor Based Field Programmable Analog Array // *Analog Integrated Circuits and Signal Processing.* – Springer, 1998 – Vol. 17. – P. 105–124.
8. **Soliman E.A., Mahmoud S.A.** New CMOS Fully Differential Current Conveyor and its Application in Realizing Sixth Order Complex Filter // *IEEE International Symposium on Circuits and Systems (ISCAS), 2009.* – P. 57–60.
9. **Hwang Y.S., Chen J.J., Li J.P.** New Current-Mode All-Pole and Elliptic Filters Employing Current Conveyors // *Springer Journal of Electrical Engineering (Archiv fur Elektrotechnik), 2006.* – Vol. 89. – P. 457–459.
10. **Csipkes D., Csipkes G.** Synthesis Method for State Variable Gm-C Filters with a Reduced Number of Active Components // *Mixed Design of Integrated Circuits and Systems (MIXDES), 2003.* – P. 292–297.
11. **Csipkes G., Csipkes D.** Synthesis Method for Gm-C Complex Polyphase Filter Design // *Mixed Design of Integrated Circuits and Systems (MIXDES), 2003.* – P. 286–291.

Received 2010 07 22

**D. Csipkes, G. Csipkes, S. Hintea, H. Fernandez-Canque.** An Analog Array Approach to Variable Topology Filters for Multi-mode Receivers // *Electronics and Electrical Engineering.* – Kaunas: Technologija, 2010. – No. 9(105). – P. 43–48.

This paper presents some system level investigations on the possibilities to implement reconfigurable topology filters intended for wireless applications. The proposed filter is built around a signal bus and a current mode configurable analog block that support the mapping of various filter orders and synthesis methods onto the same circuit. The selectivity of the filter can be extended to arbitrary transmission zeros and complex band pass type of responses. The different configurations have been tested through Eldo simulations, including first order non-idealities of the building blocks. Ill. 12, bibl. 11, tabl. 4 (in English; abstracts in English and Lithuanian).

**D. Csipkes, G. Csipkes, S. Hintea, H. Fernandez-Canque.** Keičiamosios topologijos filtrų tyrimas daugelio būsenų imtuvuose // *Elektronika ir elektrotechnika.* – Kaunas: Technologija, 2010. – Nr. 9(105). – P. 43–48.

Apžvelgta keletas galimų keičiamosios topologijos filtrų patobulinimų, skirtų bevielio ryšio įrenginių kokybei gerinti. Siūlomasis filtras yra įmontuotas signalų magistralėje. Esama būseną gali būti keičiama analoginio bloko, kuris suderinamas su įvairių eilių filtrų atvaizdų ir sintezės metodais. Atliktas Eldo matematinis modeliavimas su skirtingų parametrų filtrais. Il. 12, bibl. 11, lent. 4 (anglų kalba; santraukos anglų ir lietuvių k.).