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CMOS Technology based Current Source with Harmonic Reducing Properties

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Introduction

The replacement of sinusoidal signals in many practical cases can be solved using suitable approximations. The three level shortened square waves' technique could be used. The basic idea of such a solution is that more equally spaced converting levels are introduced, and therefore higher harmonics, especially the lower end of higher harmonics, can be reduced. This multilevel signal can be easily generated digitally and it enables simple digital processing involving only additions and shifting. An efficient CMOS technology based current source can be designed to work with such nontraditional waveforms. The current source consists of circuit, switchable current mirrors to select different current ranges and H-bridge current output stage. In this case the use of H-bridge current output permits possibility to avoid the conventional instrumentation amplifier (simple buffer amplifier can be used), resulting a reduction of the whole measuring system complexity.

This paper proposes an advanced solution for the shortened square wave CMOS current source with H-bridge current output. The analysis of the proposed system is given and new practical solutions for applications in portable devices are described. The proposed solution improves the power consumption and reduces the complexity of the system as a whole. The main advantage of this method is greater efficiency because of the fact that for measuring cycle only one or two pairs of switchable current mirrors will be activated to drive the H-bridge.

Shortened square waves

Synchronous signal processing enables measurement of low-level signals with lock-in amplifiers, and is used in different network analyzers. Classically sinusoidal excitation is used and Fast Fourier Transformation (FFT) or similar takes care of spectral separation. It enables determination of magnitude and phase of the response signal compared to the excitation signal, and gives relatively good results, depending on the quality of the excitation signal and signal processing algorithms. Situation changes dramatically in case of implantable devices, such as pacemakers. Both analog circuitry and digital signal processing tend to consume a lot of energy, and size of the device should be kept as small as possible. It is not necessary to measure with sinusoidal excitation current. Systematic errors introduced by higher harmonics of simple square wave signals can be drastically reduced by slightly modifying the waveform [1]. In case of shortening the excitation and reference signals by 30° and 18° (Fig. 1) errors can be reduced by order of magnitude in comparison with regular rectangular waves

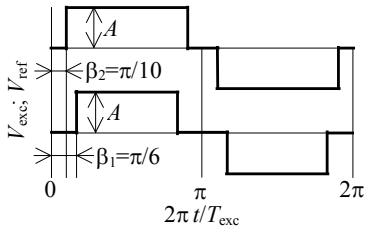

Fig. 1. Shortened square wave pulses: 18° shortened three-level signal (a); and 30° shortened three-level signal (b)

Spectra of these signals can be expressed as the Fourier series of odd harmonics

$$F(\omega t)=\frac{4A}{\pi}\left[\frac{\cos\beta}{1}\sin\omega t+\frac{\cos 3\beta}{3}\sin 3\omega t+\ldots\right]=\frac{4A}{\pi}\left[\sum_{i=1}^{\infty}\frac{\cos(2i-1)\beta}{2i-1}\sin(2i-1)\omega t\right], \quad (1)$$

where F is the Fourier spectra; A is the amplitude of the pulse signal, ω is the repetition frequency, β is measure of shortening in degrees and i is the number of the harmonic. Synchronous demodulation is sensitive only to higher harmonics, which are existing simultaneously in both, the excitation and reference signals, such as 7th, 11th, 13th,

17th, 19th, 23rd, 29th, and 31th in case of 30°/18° shortened signals. Better result is achievable using different suitable sums of waveforms together with introducing third 42° shortened three level square wave. When we sum three signals as 18° shortened signal with + sign, 30° shortened signal with – sign, and 42° shortened signal with + sign, the new waveform is free from both the 3rd and 5th harmonics. Even 7th harmonic is reduced compared to square wave. Higher harmonics however are still relatively strongly present. This situation can be improved by changing the addition coefficients from 1, -1, 1 to 2, -1, and 1 [2]. Resulting waveform is shown on Fig. 2. Appearing 3rd and 9th harmonics could pose a problem; however in case of suitably chosen signal pair it is possible to eliminate them from the multiplication result. One possible solution for such a specific pairing signal is the sum of 18°, 30° and 42° shortened signals with coefficient +1.

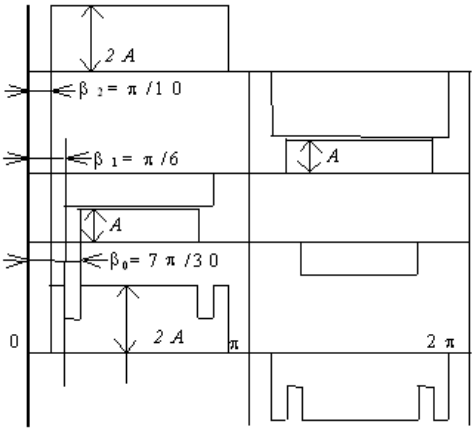

Fig. 2. Sum of three shortened square wave pulses

Signal forming for excitation is similarly simple as described earlier. It is worth noting here that a compared to piecewise continuous approximation of sinusoidal signals usage of equal levels is much more feasible in digital domain of signal generation.

CMOS Current Source

To utilize the shortened square waveform theory into practice, a low voltage and low power current exciter has to be designed. First the flexible current source with selectable output current in range from 5 to 500μA, and with supply voltage from 2.4 to 5V has been designed.

The core part of this current source will be the H-bridge output stage with multiple switchable current mirrors driving the output stage. Such realization of H-bridge output permits to use simple buffer amplifier, resulting a reduction of the whole measuring system complexity afterwards.

From the MOS transistor behavior we know that the output current range is limited. If we want to stay at minimum output current range in saturation region and strong inversion mode, then the H-bridge output transistor drain to source saturation voltage $V_{DS,\ sat}$ should not decrease below the four times thermal voltage V_T value. It means that at room temperature the minimum $V_{DS,\ sat}$ value should be about 100mV. On the other hand the $V_{DS,\ sat}$ cannot step over the 1V value due to the fact that the load impedance is about 100Ω (body tissue).

The MOS transistor drain current can be calculated [3–5]

$$I_D = \frac{KP}{2} \cdot \frac{W}{L} \cdot V_{DS,sat}{}^2, \qquad (2)$$

where the KP is the transconductance parameter, W is channel width, and L is channel length. In our case the $V_{DS,sat}$ is changing from 100mV to 1V. It means that the transistor drain current can change exactly from 5 to 500μA. The MOS transistor drain current changing interval is limited compared for example to the bipolar transistor collector current.

The next limiting factor is the single transistor output resistance r_O. To increase the output resistance and approximate the transistor output as an ideal current source, the cascode output stage must be introduced. Unfortunately the cascode output stage in H-bridge solution needs more than 3V power supply voltage. Therefore the test chip H-bridge output stage realization will use only single transistor solution.

Single transistor output resistance r_O can be calculated from formula [3]

$$r_O = \frac{1}{\lambda \cdot I_{DS,sat}}, \qquad (3)$$

where $I_{DS,sat}$ is the source drain saturation current and λ is the channel length modulation parameter. In this work the 0.5μm CMOS technology is used, where the channel lengths of output stage transistors are equal to 2μm. The λ value is approximately $0.01V^{-1}$. Using this data the single transistor output resistance at current level of 5μA will give the value of 20MΩ. At output current level of 500uA the 200kΩ output resistance will be calculated. Taking into the consideration that he output resistance below 1MΩ is undesirable; the current source test chip output current range should be in range from 5 to 100μA.

The current source required work frequency at 5μA output current should be at least 100 kHz. Single transistor transition frequency can be calculated as [3]

$$f_T \approx \frac{3KP \cdot V_{DS,sat}}{4\pi \cdot L^2 C'_{ox}}, \qquad (4)$$

where C'_{ox} is the oxide capacitance per unit area. In this work the C'_{ox} value is 1,75fF/μm^2, which is defined by used CMOS technology. The calculated minimum transition frequency for PMOS transistors is 146 MHz. This value gives the clear expectation that ON-OFF switching process of transistors with the 5μs time interval is enough to guaranty the fast enough slope rise and fall times for our application.

The design of the current source chip concludes with the 4x6 different current sources connected through switches to one H-bridge output stage. The current source as a black box is seen in Fig. 3. The current source needs two external bias signal pads to bias the inner circuitry – V_{biasn} and V_{biasp}. For switching and combining the currents

the 2x6 control inputs must be included (inputs c1 to c6 and their inversions) and two inputs to switch the H-bridge off (third) state. Table 1 shows the possible output current generating scheme for switching all of the six current sources to get the maximum 100µA output current.

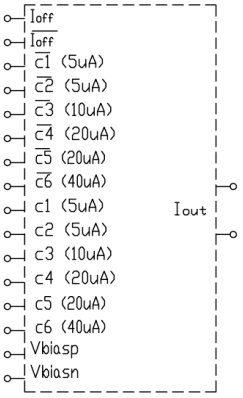

Fig. 3. Current source block diagram

Table 1. Possible output currents

Control signals	Iout
c1	5 µA
c2	5 µA
c3	10 µA
c4	20 µA
c5	20 µA
c6	40 µA

The schematic of the current source is given in Fig. 4. The V_{biasn} and V_{biasp} voltages are driving the current mirrors and afterwards the current is mirrored to 4x6 independent current sources. To achieve the simple current mirror ratio 1:1 the transistor matching error should stay ultimately bellow 2%. To fulfill the demand for so small error the channel length of the transistor must be at least four times over the minimum strip dimensions (0.5µm technology in our case) and the channel area (LxW) must be larger than 25µm^2. Unfortunately the bigger is the mirrored current and primal current ratio; the bigger is the matching error. The current mirroring ratios over 1:8 are therefore not usable. The attempt was made to find the best optimum for transistor channel length and width ratios so, that the matching error at 1:1 ratio stays under 2% and 1:8 ratio does not exceed 5%. The "worst case" simulation results are shown in Fig. 5. The design and calculations show that the current error for all added currents did not exceed the 5% level.

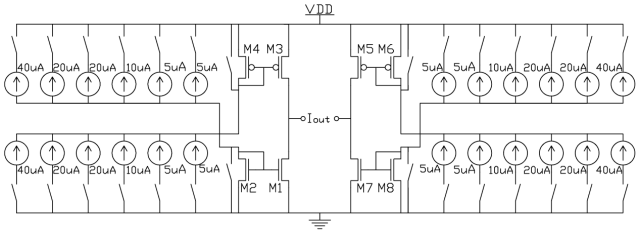

Fig. 4. Current source schematic

The current source simulation results in Fig. 5 exposit the H-bridge output current through the load. The resistors R7 and R8 were chosen equal to 1Ω in simulations and they are imitating the resistivity of the pad contacts. Load impedance, with low frequency value of 100Ω, is connected in series with this contact resistivity. In reality in most applications the load resistivity is complex and instead of resistivity the impedance must be handled.

Fig. 5 shows all the possible current values what can be generated and switching responses of the developed current source. When we are using the generated shortened square wave solutions, then only one certain current value like shown on Fig. 1, or two current values like on Fig. 2, will be used.

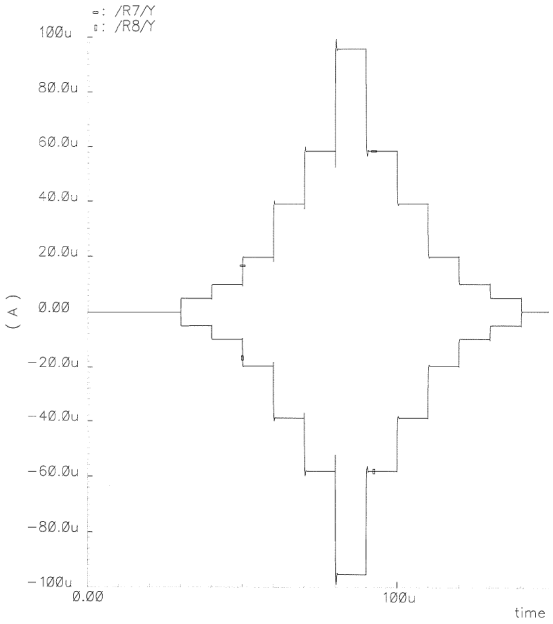

Fig. 5. Current source output current simulation results

The test chip is designed with the possibility to use external bias voltage. The nominal bias voltage value is chosen to be 1.2V. The low-power biasing circuitry solution is shown in Fig. 6.

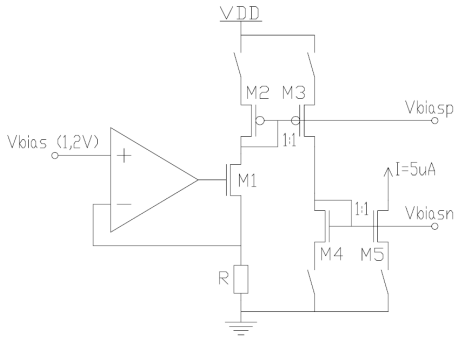

Fig. 6. Biasing circuit

The voltage to current conversion is realized using low-power operational amplifier, transistor M1 and resistor R. The weak point of this solution is the resistor R with nominal value 240Ω. In used 0.5µm technology all resistors have unfortunately positive temperature coefficients. Additionally the lay-out geometry dimension of the resistor becomes too big. To scale down the resistor lay-out about 20% leads us to the one long channel NMOS transistor in series with resistor R, when the transistor is

working in linear region. The resistor nominal value will be then 190kΩ.

Results of the simulation comparing one 240kΩ resistor with 190kΩ resistor in series with n-channel transistor are shown on Fig. 7. The resistor in series with n-channel transistor gives the good output current stability in wide enough temperature range (from 0 to 40℃), but only then when the input bias voltage stays at 1.2V.

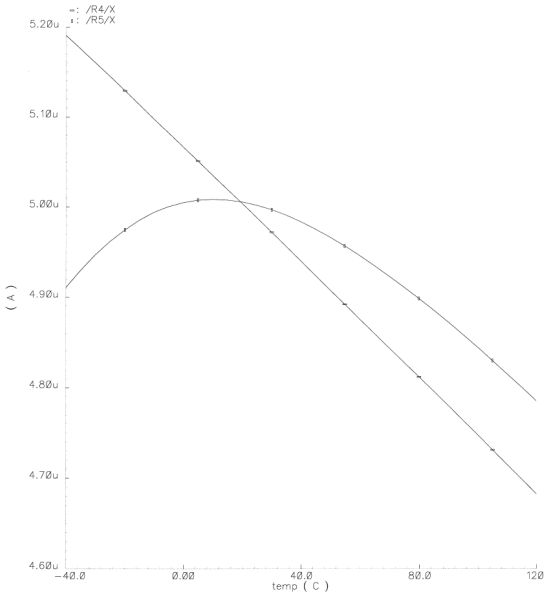

Fig. 7. Bias circuit output current temperature dependence simulations

Conclusions

The design of the CMOS technology based efficient low-power high speed current source has been made. The test chip layout has been made using NSC 0.5μm technology. The novel results are as follows:

- Reduced system circuit complexity and therefore smaller chip lay-out area.
- Greater efficiency, measuring cycles are short and in stand by regime only the bias circuit consumes power.

The next paper on this topic will include the realistic lay-out the whole designed circuitry and the experimental measurement results.

Acknowledgement

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Multilevel higher harmonics reducing algorithm is proposed for digitally generated signal processing code involving only additions and shifting. An efficient CMOS technology based current source is designed to work with shortened square wave waveforms. The current source consists of biasing circuit, switchable current mirrors and H-bridge current output stage. The analysis of the proposed system is given and new practical solutions for applications in portable devices are described. The proposed solution improves the power consumption and reduces the complexity of the system as a whole. The main advantage of this method is greater efficiency because for measuring cycle only one or two pairs of switchable current mirrors will be activated to drive the H-bridge. Ill. 7, bibl. 5, tabl. 1 (in English; abstracts in English and Lithuanian).

A. Kasemaa, P. Annus. Srovės šaltinio harmonikų mažinimo ypatybės taikant KMOP technologiją // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2010. – Nr. 10(106). – P. 143–146.

Pasiūlytas naujas daugiapakopis aukštesniųjų harmonikų mažinimo algoritmas. Jis sukurtas atlikus generuojamo signalo papildymus ir pakeitimus. KMOP technologijos pagrindu suprojektuotas srovės šaltinis, dirbantis su sutrumpintos stačiakampės formos signalais. Pateikta naujų pasiūlytos sistemos praktinio taikymo mobiliems įrenginiams būdų. Nors įdiegus šį pasiūlymą padidėja energijos sąnaudos, tačiau supaprastėja visa sistema. Pagrindinis šio metodo pranašumas – didesnis efektyvumas. Il. 7, bibl. 5, lent. 1 (anglų kalba; santraukos anglų ir lietuvių k.).