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A New Method of Power Arithmetic for Parallel Inverter

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Introduction

Inverters are connected to an ac common bus with the aim to share properly the loads. In addition, every unit must be able to operate independently when communication is too difficult due to the long distance between its connection points [1]. The droop control technique applies to wireless interconnections [2–5]. This technique consists of adjusting the output-voltage frequency and amplitude in function of the active and reactive power delivered by the inverter [6, 7].Thus, the active and reactive power arithmetic is one of the key issues in the wireless drop control systems.

The power arithmetic methods for droop control technique have been presented in some literatures. Y. B. Byun proposed a power arithmetic method [8]. It can achieve a good load sharing. But, it is too complex. In addition, the existing integral unit causes one fundamental cycle delay, which decreases the stability of system. An improved method which imports slide window function can greatly reduce delay time (one sampling cycle) [9–11]. However, the latter method can't accurately calculate power value while abrupt change of load. It is just a compromise way between the rapidity and precision. In previous work, most methods occupy a great amount of DSP memory space using sine and cosine tables and make power arithmetic complex.

In this paper, a novel method of power arithmetic is proposed, which improves the steady state and the transient response of the parallel inverter. It rebuilds sinusoidal signal according to three elements of sine using the last-value and next-value of signal in discrete domain. Thus, it can obtain power value only one sampling cycle under load sudden changes. Moreover, without sine and cosine tables make much smaller DSP space and cut down computing process.

The paper is organized as follows. In Section 2, the principle of droop control method is analyzed. Section 3 presents the conventional power arithmetic. Section 4 proposes a new power arithmetic method. Section 5 provides the simulation and experimental results from a two-*75-kVA*- inverter system.

Principle of droop control

The equivalent circuit of two paralleling inverters is shown in Fig. 1.

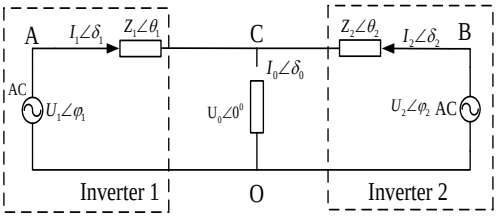

Fig. 1. Equivalent circuits of two paralleling inverters

Where U_1 and U_2 are output voltages root mean square (RMS) of two inverters. φ_1 and φ_2 are the phase angles, U_0 is RMS of the load voltage, Z and θ are the magnitude and the phase of the output impedance, and $R=Z\cos\theta$, $X=Z\sin\theta$:

$$S_1 = \dot{U}_1\dot{I}_1^* = \frac{U_1^2}{Z_1}e^{j\theta_1} - \frac{U_1U_0}{Z_1}e^{j(\varphi_1+\theta_1)} = P_1 + Q_1, \quad (1)$$

$$\begin{cases} P_1 = \dfrac{U_1^2}{Z_1}\cos\theta_1 - \dfrac{U_1U_0}{Z_1}\cos(\varphi_1+\theta_1), \\ Q_1 = \dfrac{U_1^2}{Z_1}\sin\theta_1 - \dfrac{U_1U_0}{Z_1}\sin(\varphi_1+\theta_1). \end{cases} \quad (2)$$

The active power and the reactive power are expressed as follows:

$$\begin{cases} P_1 = \dfrac{U_1R_1}{R_1^2+X_1^2}(U_1 - U_0\cos\varphi_1) + \dfrac{U_1U_0X_1}{R_1^2+X_1^2}\sin\varphi_1, \\ Q_1 = \dfrac{U_1X_1}{R_1^2+X_1^2}(U_1 - U_0\cos\varphi_1) + \dfrac{U_1U_0R_1}{R_1^2+X_1^2}\sin\varphi_1. \end{cases} \quad (3)$$

$$\begin{cases} U_1 - U_0\cos\varphi_1 = \dfrac{R_1P_1 + X_1Q_1}{U_1}, \\ U_0\sin\varphi_1 = \dfrac{X_1P_1 - R_1Q_1}{U_1}. \end{cases} \quad (4)$$

Assumed that $X_1 >> R_1$ and φ_1 is very small, thus, R_1 is neglected and, $sin\varphi_1 \approx \varphi_1$, $cos\varphi_2 \approx 1$:

$$\begin{cases} U_1 - U_0 \approx \dfrac{X_1Q_1}{U_1}, \\ \varphi_1 \approx \dfrac{X_1P_1}{U_1}. \end{cases} \quad (5)$$

(5) shows the amplitude and the phase of output voltage is respectively determined by the reactive power and the active power. In other words, the angle φ can be controlled by regulating P, whereas the inverter voltage U is controllable through Q:

$$\begin{cases} f_1 - f_{10} = -m(P_1 - P_{10}), \\ U_1 - U_{10} = -n(Q_1 - Q_{10}). \end{cases} \quad (6)$$

Where, m and n are the droop coefficients for the frequency and amplitude, respectively. f_0 and U_0 are rated frequency and rated voltage, respectively. P_0 and Q_0 are the quiecsent points for active and reactive power. The frequency and voltage droop control characteristics are shown in Fig. 2. When the frequency f deviates from the steady-state operating point $A0$ to $A1$(or $A2$), P regulater makes the operating point close to the point $A0$. Similarly, the inverter voltage U is controllable through Q regulater.

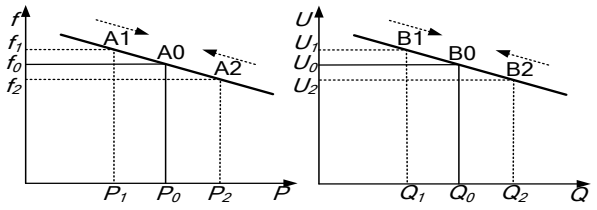

Fig. 2. Droop control characteristics of frequency and voltage

Conventional power arithmetic

The expressions of instantaneous output voltage and current are as follows:

$$v = \sqrt{2}V\sin(\omega t + \varphi_v),\ i = \sqrt{2}I\sin(\omega t + \varphi_i), \quad (7)$$

where V and I are the RMS value of voltage and current, respectively. φ_v and φ_i are initial phase angle of voltage and current. the value of instantaneous power is obtained as

$$P(t) = VI\cos(\varphi_V - \varphi_i) - VI\cos(2\omega t + \varphi_V + \varphi_i). \quad (8)$$

The average power (the average value during a fundamental cycle) can be obtained as follows

$$P = \frac{1}{T}\int_0^T P(t)dt = VI\cos(\varphi_V - \varphi_i). \quad (9)$$

The parameters V_R, V_I, I_R, and I_I are defined:

$$\begin{cases} \dfrac{1}{2\pi}\int_0^{2\pi} v.\cos\omega t d(\omega t) = \dfrac{\sqrt{2}}{2}V\sin\varphi_v = V_R, \\ \dfrac{1}{2\pi}\int_0^{2\pi} v.\sin\omega t d(\omega t) = \dfrac{\sqrt{2}}{2}V\cos\varphi_v = V_I, \\ \dfrac{1}{2\pi}\int_0^{2\pi} i.\cos\omega t d(\omega t) = \dfrac{\sqrt{2}}{2}I\sin\varphi_i = I_R, \\ \dfrac{1}{2\pi}\int_0^{2\pi} i.\sin\omega t d(\omega t) = \dfrac{\sqrt{2}}{2}I\cos\varphi_i = I_I. \end{cases} \quad (10)$$

The active and reactive power can be written as follows:

$$\begin{cases} P = VI\cos(\varphi_v - \varphi_i) = 2(V_R.I_R + V_I.I_I), \\ Q = VI\sin(\varphi_v - \varphi_i) = 2(V_R.I_I + V_I.I_R). \end{cases} \quad (11)$$

However, the digital control in DSP can't directly calculate integral. Hence, the integral is rewritten as cumulative summing in the discrete domain. Assumption that the number of sampling points is N in one fundamental cycle. The conventional power arithmetic is shown in Fig. 3.

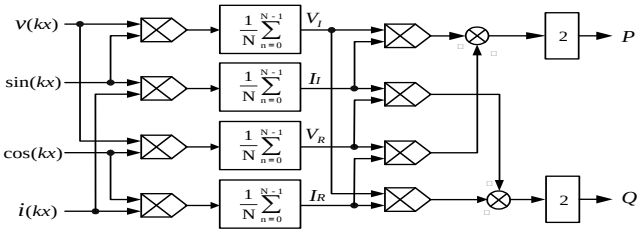

Fig. 3. Diagram of conventional power arithmetic in digital domain

Power arithmetic is achieved in one fundamental cycle. It can satisfy the requirements when the output power is stable. If the load varies abruptly, the real value of power is obtained at least one fundamental cycle delay. The sine and cosine tables occupy DSP resources and cause calculating complex.To solve this problem, an improved method with sliding windows was proposed as shown in Fig. 4.

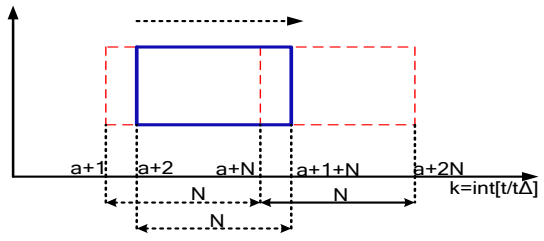

Fig. 4. Diagram of power arithmetic with sliding windows

In Fig. 4, the length of the sliding window is N, the shifting distance N is chosen equal to the number of sample points in one fundamental cycle. It puts the sample value of (a+1)+N point into the.a+1 unit, and gives the power values from a+1 point to a+N point.The delay of power arithmetic is reduced from N sampling cycles (a

fundamental cycle) to one sampling cycle. But, computing power values are imprecise under load change. Therefore, this method is only a compromise way between the rapidity and precision.

Novel method of power arithmetic

The sinusoidal signal in time domain is $y=Y_m sin(\omega t+\varphi)$. If the three elements are known, the waveform can be determined. In the general case, the fundamental frequency ω is known, so only two parameters need to decide. The initial phase angle is φ and the amplitude is Y_m. The sinusoidal signal is shown in Fig. 5.

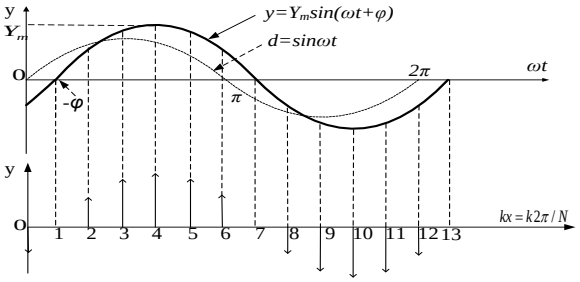

Fig. 5. Diagram of continuous sinusoidal signal

Assumed that the fundamental cycle is T_s, and the sampling cycle is T_c. The sinusoidal signal is $y=Y_m sin(\omega t+\varphi)$. The sampling value of sinusoidal signal is y_k

$$y_k = Y_m \sin(kx+\varphi) = Y_m \cos\varphi \sin kx + Y_m \sin\varphi \cos kx, \quad (12)$$

where $x=2\pi T_c/T_s=2\pi/N$, N is the ratio of fundamental cycle to the sampling cycle. the next cycle value y_{k+1} is as follows:

$$\begin{aligned} y_{k+1} &= Y_m \sin((k+1)x+\varphi) = \\ &= Y_m \cos\varphi \sin(k+1)x + Y_m \sin\varphi \cos(k+1)x, \end{aligned} \quad (13)$$

$$\begin{bmatrix} \sin kx & \cos kx \\ \sin(k+1)x & \cos(k+1)x \end{bmatrix} \begin{bmatrix} Y_m \cos\varphi \\ Y_m \sin\varphi \end{bmatrix} = \begin{bmatrix} y_k \\ y_{k+1} \end{bmatrix}, \quad (14)$$

$$\begin{bmatrix} Y_m \cos\varphi \\ Y_m \sin\varphi \end{bmatrix} = V_k . \begin{bmatrix} y_k \\ y_{k+1} \end{bmatrix}, \quad (15)$$

where

$$V_k = \begin{bmatrix} -\dfrac{\cos x}{\sin x}\cos kx + \sin kx & \dfrac{1}{\sin x}\cos kx \\ \cos kx + \dfrac{\cos x}{\sin x}\sin kx & \dfrac{1}{\sin x}\sin kx \end{bmatrix}. \quad (16)$$

The single-phase voltage and current are as follows:

$$\begin{cases} u = U_m \sin(\omega t + \varphi_u), \\ i = I_m \sin(\omega t + \varphi_i). \end{cases} \quad (17)$$

Thus

$$\begin{bmatrix} U_m \cos\varphi_u \\ U_m \sin\varphi_u \end{bmatrix} = V_k . \begin{bmatrix} U_k \\ U_{k+1} \end{bmatrix}, \quad (18)$$

where U_k, U_{k+1} are the last-value and next-value of voltage, respectively.

$$\begin{bmatrix} U_m \cos\varphi_u \\ U_m \sin\varphi_u \end{bmatrix} = V_k . \begin{bmatrix} U_k \\ U_{k+1} \end{bmatrix}, \quad (19)$$

where I_k, I_{k+1} are the last-value and next-value of current, respectively.

The expressions of active power and reactive power are as follows:

$$\begin{cases} P = \dfrac{1}{2} U_m I_m \cos(\varphi_u - \varphi_i) = \\ \quad = \dfrac{1}{2}(U_m \cos\varphi_u . I_m \cos\varphi_i + U_m \sin\varphi_u . I_m \sin\varphi_i), \\ Q = \dfrac{1}{2} U_m I_m \sin(\varphi_u - \varphi_i) = \\ \quad = \dfrac{1}{2}(U_m \sin\varphi_u . I_m \cos\varphi_i - U_m \cos\varphi_u . I_m \sin\varphi_i). \end{cases} \quad (20)$$

The active power and reactive power in discrete domain is expressed:

$$\begin{cases} P = \dfrac{1}{2\sin^2 x}(U_k I_k + U_{k+1} I_{k+1}) - \\ \quad - \dfrac{\cos x}{2\sin^2 x}(U_k I_{k+1} + U_{k+1} I_k), \\ Q = \dfrac{1}{2\sin x}(U_k I_{k+1} - U_{k+1} I_k). \end{cases} \quad (21)$$

The variable x is a constant once the number N of sampling points is given. According to (21), the active power and reactive power are combined by twice sample values of voltage and current. The diagram of proposed power arithmetic in digital domain is shown in Fig. 6.

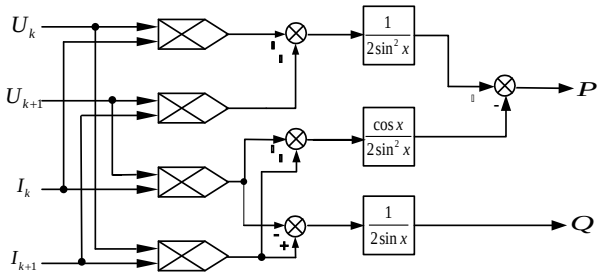

Fig. 6. Diagram of proposed power arithmetic in digital domain

There are not sine function *sin(kx)* and cosine function *cos(kx)* in equation(21). Hence, a large amount of storage space for DSP is released in digital domain. Moreover, there are no quantitative errors and power arithmetic becomes simple. Because the arithmetic of power is obtained in just one sampling cycle, the system can achieve an improved transient response. In order to verify the validity of the principle and the fast-track dynamic performance, simulation and experiment results are given in the next section.

Simulation and experiment results

In the simulation, set-up *N=60, f=50Hz, x=π/30*. According to eq.(21), the discrete-time equivalent expressions of power arithmetic is given as:

$$\begin{cases} P = 45.76*(U_k I_k + U_{k+1} I_{k+1}) - \\ \quad -45.51*(U_k I_{k+1} + U_{k+1} I_k), \\ Q = 4.78*(U_k I_{k+1} - U_{k+1} I_k). \end{cases} \quad (22)$$

The simulation results of power arithmetic with different current amplitudes and phases are given. The voltage RMS is *220V* and its phase is zero. The voltage and current expressions are as follows:

$$\begin{cases} u = 220\sqrt{2}\sin(100\pi t), \\ i_1 = 320\sqrt{2}\sin(100\pi t), \\ i_2 = 320\sqrt{2}\sin(100\pi t - \pi/6), \\ i_3 = 160\sqrt{2}\sin(100\pi t), \\ i_4 = 160\sqrt{2}\sin(100\pi t - \pi/6). \end{cases} \quad (23)$$

The current i_1 and i_3 are working in resistance load, and the current i_2 and i_4 are working in inductive load. The active power value is *P1*, P2, *P3* or *P4* and the reactive power value is *Q1*, *Q2*, *Q3* or *Q4*, when the current is i_1, i_2, i_3 and i_4, respectively.

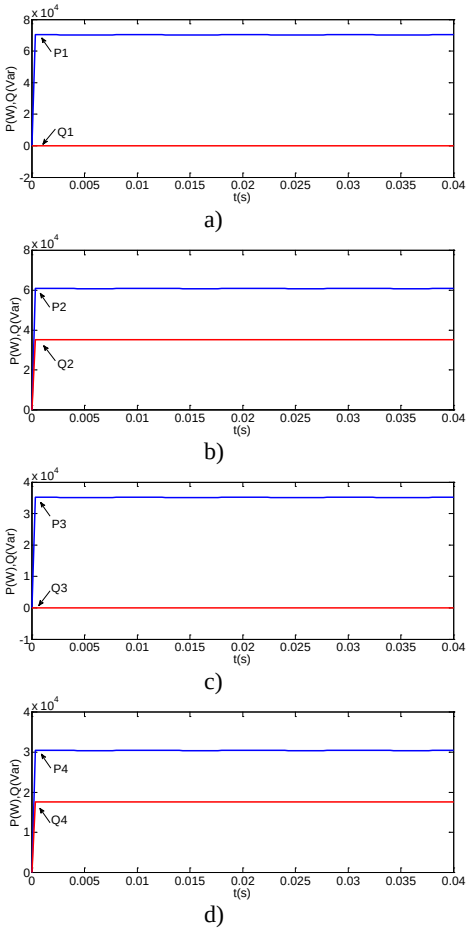

Fig. 7. Power arithmetic with the phase of current: a – i_1; b – i_2; c – i_3; d – i_4

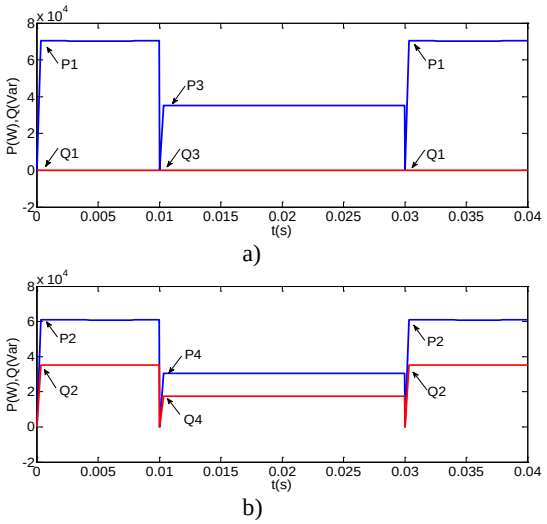

Fig. 8. Power arithmetic with the amplitude of current varying abruptly: a – i_1->i_3->i_1; b – i_2->i_4->i_2

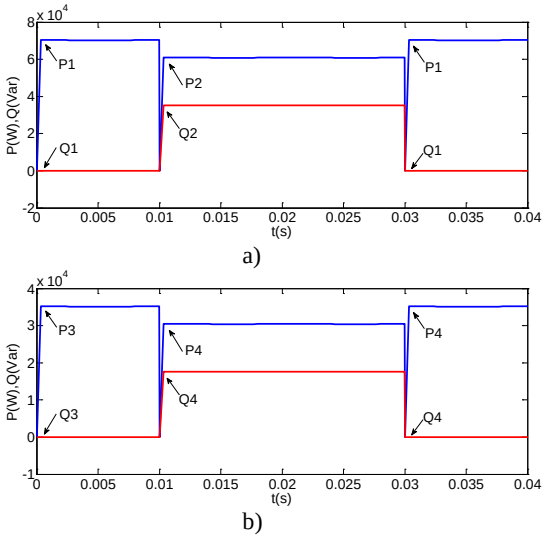

Fig. 9. Power arithmetic with the phase of current varying abruptly: a – i_1->i_2->i_1; b – i_3->i_4->i_3

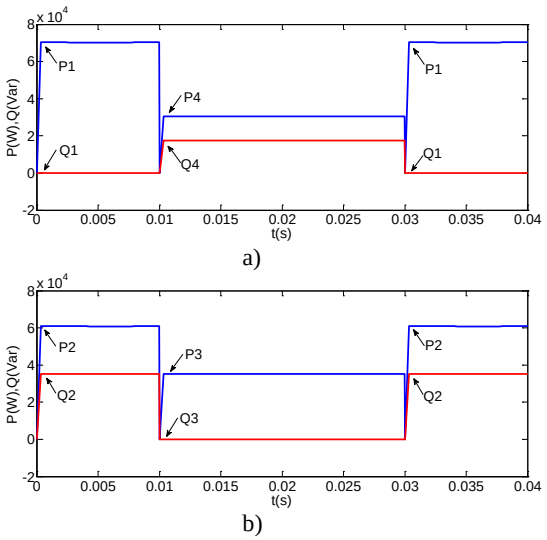

Fig. 10. Power arithmetic with the amplitude and phase of current varying abruptly: a – i_1->i_4->i_1; b – i_2->i_3->i_2

Fig. 7 shows the simulation results of the novel power arithmetic for various load condition. As it can be seen, the

novel method has high accuracy of active and reactive power value. The dynamic characteristics of the novel power arithmetic scheme are depicted in Fig. 8, Fig. 9 and Fig. 10, in which the current amplitude and phase are abruptly changed at the moment of 0.1 second and 0.3 second. Fig. 8 shows the power arithmetic results when the current amplitude varied abruptly. The power arithmetic value has reached steady state only one sampling cycle delay. Fig. 9 shows the power arithmetic results when the current phase varied abruptly. The power arithmetic value is changed with the varied current phase angle, and the power arithmetic value has reached steady state only one sample time delay. Fig. 10 shows power arithmetic when the current phase and amplitude varied abruptly. The power arithmetic value is changed with the varied current phase angle.

Simulation results indicate that the truth value of power is obtained accurately only in one sampling cycle under load change. The power arithmetic peak values at the moment of 0.1 second and 0.3 second are yielded, as the last-value and next-value of current are constructed the error sinusoidal current waveform. However, this power arithmetic peak values don't affect the power droop control of parallel inverters, as the PID and repetitive controller can limit the amplitude.

Table1. Comparisons of ideal value and simulation value

Load	Active power $P(W)$		Reactive power $Q(Var)$	
	Ideal value	Simulation value	Ideal value	Simulation value
Current i_1	70400	70394	0	0
Current i_2	60968	60960	35200	35190
Current i_3	35200	35196	0	0
Current i_4	30480	30477	17600	17595

Table 1 is the comparisons of ideal value and simulation value. It shows that the steady-state active and reactive errors are slower than *0.013%, 0.028%*. The novel method has high precision of active and reactive power value.

In the experiment, two 60-KW single-phase inverters units are built. Each inverter consists of IGBT with a switching frequency of 3000 Hz and an LC output filter, with the following parameters: L=60μH,C= 1200μF,The IGBT(Eupec-*FZ2400R17KF6C-B2*) is chosen and this system is controlled by *TMS320LF2407* fixed-point 40-Million Hz digital signal processor (DSP) from Texas Instruments. DC voltage is 350-640 V, and output voltage RMS is 220 V at 50 *Hz*. Fig. 11 shows the voltage and current waveform of the parallel inverters in state-steady operation. u_1, i_1, i_2 are the output voltage, the output current of one inverter and the current of the other inverter, respectively. The total current is 130A and the parallel circulation current is less than 10A.

Fig. 12 shows the voltage and current waveform of the parallel three-phase inverters in dynamic process. The total load current is changed from 90A to 240A at the moment t1. The parallel circulation current is less than 15A.

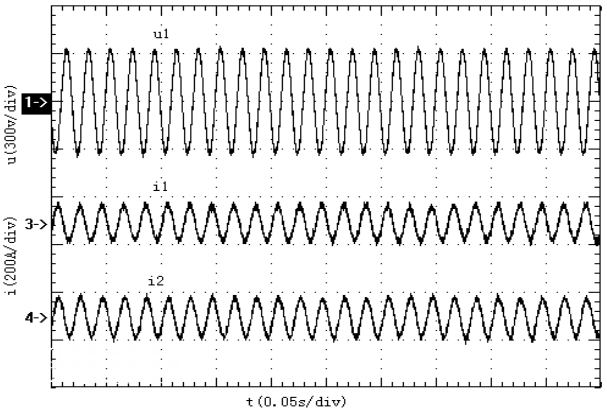

Fig. 11. Voltage and current waveforms in steady-state operation for parallel inverters

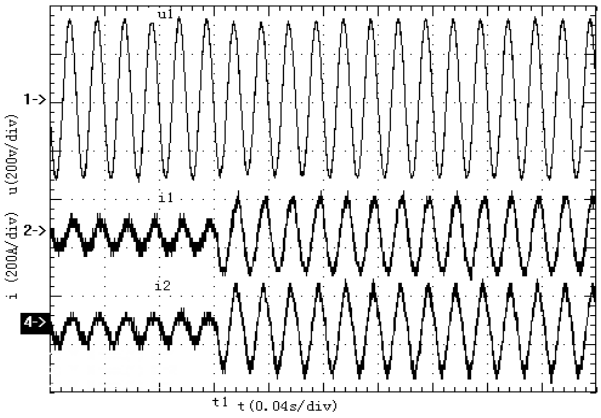

Fig. 12. Voltage and current waveforms under load sudden changes for parallel inverters

Conclusions

In this paper, new power arithmetic for parallel inverters has been proposed. The proposed power arithmetic has advantages of smaller occupied DSP resources and arithmetic steps than the conventional power arithmetic, as the sine and cosine tables are cancelled. Moreover, the value of power is obtained only one sampling cycle under load changes. Simulation shows that it has high precision in steady-state operation and obtains real power value only one sample cycle under load sudden changes. Experiment results show a good steady-state characteristics and a proper transient response in sharing loads.

Acknowledgements

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References

1. **Barsi S., Ceraolo M., Pelachi P., Poli D.** Control techniques of dispersed generators to improve the continuity of electricity supply // IEEE power engineering society winter meeting. – 2002. – P.789–794.
2. **Guerrero J. M., de Vicuna L. G., Matas J., Castilla M., Miret J.** A wireless controller to enhance dynamic

performance of parallel inverters in distributed generation systems // IEEE Transactions on Power Electronics, 2004. – Vol.19. – No. 5. – P.1205–1213.
3. **Bekiarov S. B., Emadi A.**Uninterruptible power supplies: classification, operation, dynamics, and control // IEEE Applied Power Electronics Conference and Exposition. – 2002. – P. 597–604.
4. **Guerrero J. M., de Vicuna L. G., Matas J., Castilla M., Mire J.** Output impedance design of parallel–connected UPS inverters with wireless load–sharing control // IEEE Transactions on Industrial Electronics. – 2005. – Vol. 52. – No. 4. – P. 1126–1135.
5. **Gang Yao, LiXue Tao, LiDan Zhou, Chen Chen.** State-feedback Control of a Current Source Inverter-based STATCOM // Electronics and Electrical Engineering. – Kaunas: Technologija, 2010. – No. 3(99). – P. 17–22.
6. **Guerrero J. M., Matas J., de Vicuna L. G., Castilla M., Miret J.** Wireless–control strategy for parallel operation of distributed–generation inverters // IEEE Transactions on Industrial Electronics, 2006. – Vol. 53. – No. 5. – P. 1461–1470.
7. **Brabandeer K. D., Bolsens B., Den K. V.** A Voltage and Frequency Droop Control Method for Parallel Inverters // IEEE Transactions on Power Electronics, 2007. – Vol. 22. – No.4. – P. 1107–1115.
8. **Byun Y. B., Koo T. G., Joe K. Y.** Parallel Operation of Three–Phase UPS Inverters by Wireless Load Sharing Control // IEEE International Telecommunications Energy Conference, 2000. – P. 526–532.
9. **Jiarong K., Shaojun X.** An Arithmetic of Power to Improve the Stability of Parallel UPS Without Control Interconnection // Transaction of China Electrotechnical Society, 2007. – Vol. 22. – No. 3. – P. 85–90.
10. **Hongliang W., Xiumei Y., Xuejun P., Yong K.** A New Method of Power Calculation Based on Parallel Inverter // IEEE International Power Electronics and Motion Control Conference, 2009. – P. 1573–1576.
11. **Zmood D. N., Holmes D. G.** Stationary frame current regulation of PWM inverters with zero steady–state error // IEEE Transaction on Power Electronics, 2003. – Vol. 18. – No. 3. – P. 814–822.

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To overcome the one fundamental cycle delay of the conventional power arithmetic under the load change, a new method of power arithmetic is proposed, which rebuilds the sinusoidal signal only using the last-value and next value of signal in discrete domain. Thus, it is able to fast calculate power value and can obtain the true power value only in one sampling cycle. Moreover, it occupies much smaller DSP space and cuts down computing process, as the sine and cosine tables are cancelled. The high precision of proposed method has validated through comparison with the ideal and simulation values of active, reactive power. Experimental results from a two-75-kVA-inverters system show the proposed method is practicable. Ill. 12, bibl. 11, tabl. 1 (in English; abstracts in English and Lithuanian).

Hongliang Wang, Yinyin Xie, Xuejun Pei, Yong Kang, Xiumei Yue. Naujo galios skaičiavimo metodo taikymas lygiagrečiuosiuose inverteriuose // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2010. – Nr. 10(106). – P. 3–8.

Kai apkrova didelė, dėl susidariusių didelių duomenų srautų elektros variklį sunku kontroliuoti. Pasiūlytas naujas galios skaičiavimo metodas, įvertinantis tik sinusinio signalo vieną atsitiktinę ir paskutinę vertes. Tai leidžia labai greitai apskaičiuoti esamą elektrinę galią. Mažesni reikalavimai keliami skaitmeniniam signalų apdorojimui. Tokio metodo tikslumą patvirtina apskaičiuotos ir sumodeliuotos vertės. Atlikti eksperimentiniai tyrimai su dviem 75 kVA inverteriais. Il. 12, bibl. 11, lent. 1 (anglų kalba; santraukos anglų ir lietuvių k.).