Recursive PLL based on the Measurement and Processing of Time

D. Perisic[1], A. Zoric[2], M. Perisic[1], V. Arsenovic[1], L. Lazic[3]
[1]Faculty of Information Technologies, Slobomir P University,
St. Pavlovica put bb, 76300 Slobomir, Republic of Srpska, Bosnia and Herzegovina
[2]Faculty of Technical Science,
St. Kneza Milosa 7, Kosovska Mitrovica, Serbia
[3]State University of Novi Pazar - Faculty of Technical Sciences,
St. Vuk Karadzic bb, 36300 Novi Pazar, Serbia
djurdje@beotel.rs

***Abstract*—This paper describes one recursive model of the Phase Locked Loop (PLL) of the second order based on the measurement and processing of the time difference between the input and output periods. The stability and the other conditions, under which the described system can have the properties of a PLL, are investigated using the Z transform analyses. Computer simulation of PLL is introduced in order to give better insight into the PLL characteristics and to confirm the mathematical analyses too. Made analysis shows that PLL is suitable for the wide range of applications. For the corresponding system parameters, PLL possesses the power noise rejection ability. For some other system parameters this PLL possesses the power tracking ability. It can also be used for the measurement of the period of the input signal in the noise environment. The oscilloscope picture of the input and output signals recorded on the realized PLL is presented.**

***Index Terms*—Digital circuits, feedback circuits, frequency locked loops, phase locked loops.**

I. INTRODUCTION

Although the Phase Locked Loop (PLL) and the Frequency Locked Loop (FLL) are closely related systems, the difference between PLL and FLL is not precisely defined in the literature. It is common to find in the literature that PLL is the system that, when in the stable state, reduces both the phase and the frequency difference between the input and output signals to zero. However, the phase difference in PLL applications is not to be obviously zero. It may also be $\pi/2$, $2\pi/3$, π, 2π or any. Because of that it would be useful to define more precisely the phase difference for the stable PLL, identifying the common property for all of them. In other words, the phase difference can be any value, but it has not to depend on the initial conditions of the input and output signals. Therefore, the stable PLL deals with the phase difference, which is not random. It can be also controlled. On the other hand, the stable FLL reduces only the frequency difference between the input and output signals to zero. The stable FLL generates random phase difference depending on the initial conditions. The output frequency of both PLL and FLL can also be, for the stable system, in certain pre-defined relation to the input frequency.

It would be now useful to identify the different classes of both PLL and FLL separately. But this is not the aim of this article. The previous observations enable the better understanding of the approach of PLL described in this article and the existing approaches of PLL and FLL.

Generally, the error as the difference between the input and output signals of FLL and PLL can be generated by the measurement of the phase, the frequency, the amplitude, and the time. The most frequently used PLL belong to the first group. Those PLL based on the measurement of the amplitude and time, are very rare in the literature. On the other hand, the measurement of the time is the easiest and the most precise today. Obviously, the corresponding algorithms for the measurement and processing of time, using electronic circuits, have not been still investigated. These algorithms are to be simple for realizations and widely applicable. Once investigated, this type of PLL and FLL would appear in future as more powerful and more applicable than the others.

In this paper, one new approach to PLL of the second order is described. It is based on the measurement and the recursive processing of the time difference between the input and output signals. The approach of FLL of the first order, described in paper [1], is also based on the recursive processing of the time difference between the input and output signals. References [2]–[4] are based on the measurement of frequency difference between the input and output signals. Nevertheless, they are closely related to PLL described in this article because of the similarity of some hardware parts used in their realizations. The articles [5]–[12] in the field of PLL and FLL represent the wider base of literature. The books [13]–[15] are used for electronics implementation and as mathematical and theoretical base in the development and analyses.

II. MATH DESCRIPTION OF PLL

General case of the time relation between an input signal Sin and an output signal Sop of PLL is shown in Fig.1. Instead of the phase difference, the time difference τ_k is used

Manuscript received June 12, 2013; accepted February 26, 2014.
This article was supported by the Ministry of Science and Technology of the Republic of Serbia under the projects III47016 and TR 35026.

in this math description. The periods TI_k and TO_k as well as τ_k occur at discrete times t_0, t_1,… t_k, t_{k+1}, which are defined by the falling edges of the pulses of Sop, Fig. 1. The natural relation between the variables (1), yields from Fig. 1. The main recursive equation describing PLL is given by (2), where "a" and "b" are the system parameter of PLL. The physical meaning of "a" and "b" will be cleared in the part, which describes the realization of PLL:

$$^{2}_{k+1} = ^{2}_{k} + TI_k - TO_k, \quad (1)$$

$$TO_{k+1} = a(^{2}_{k+1} - ^{2}_{k}) + b^{2}_{k+1}. \quad (2)$$

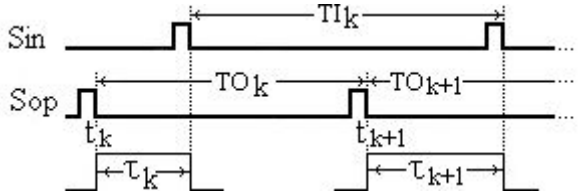

Fig. 1. The input and output variables of PLL: TI_k, TO_k and τ_k.

According to (1) and (2), PLL has two output variables, which describe the behaviour of PLL in the function of TI(k). The output variables are $\tau(k+1) = f[TI(k)]$ and $TO(k+1) = f[TI(k)]$.

To analyse the conditions under which the described system possesses the properties of PLL, let us find the Z transform of respectively (1) and (2):

$$z^{2}(z) - z^{2}_{0} = ^{2}(z) + TI(z) - TO(z), \quad (3)$$

$$zTO(z) - zTO_0 = az^{2}(z) - az^{2}_{0} - a^{2}(z) + bz^{2}(z) - bz^{2}_{0}, \quad (4)$$

where TO_0 and τ_0 are the initial values of TO(k) and τ(k).

Changing τ(z) from (3) into (4), it can be found out

$$TO(z) = TI(z)\frac{(a+b)z - a}{z^2 + z(a+b-1) - a} + R_1(z), \quad (5)$$

where

$$R_1(z) = \frac{^{2}_{0}zb + z(z-1)TO_0}{z^2 + z(a+b-1) - a}. \quad (6)$$

Changing TO(z) from (5) to (3), it can be calculated

$$^{2}(z) = TI(z)\frac{z}{z^2 + z(a+b-1) - a} + R_2(z), \quad (7)$$

where

$$R_2(z) = \frac{^{2}_{0}[z^3 + z^2(a-1) - za] - (z-1)zTO_0}{(z-1)[z^2 + z(a+b-1) - a]}. \quad (8)$$

III. ANALYSES OF CONDITIONS FOR PLL

To investigate the conditions under which the described system has the properties of PLL, let us suppose that the step input is TI(k) = TI = constant. Changing the Z transform TI(z) = TI*z/(z-1) into (5) and using the final value theorem, it is possible to find the final value of the output period TO_∞ = lim TO(k) if k→∞, using TO(z)

$$TO_\infty = \lim[TO(k)]_{k\to\infty} = \lim[(z-1)*TO(z)]_{z\to 1} = TI. \quad (9)$$

Changing now TI(z) = TI*z/(z-1) into (7) and using the final value theorem, it is possible to find the final value of the time difference τ_∞ = lim τ(k) if k→∞, using τ(z)

$$^{2}_{\infty} = \lim ^{2}(k)_{k\to\infty} = \lim[(z-1)^2 (z)]_{z\to 1} = TI / b. \quad (10)$$

According to (9) and (10), it follows that the described model possesses the properties of PLL. Equation (9) suggests that for the stable PLL the output frequency is equal to the input frequency. Equation (10) also proves that the time difference for the stable PLL, does not depend on the initial conditions and it can be controlled by the system parameter "b". Note that, in comparison with the conventional PLL, instead of the output frequency and the phase difference between Sin and Sop, the output period TO(k) and the time difference τ(k) are used in this analyses.

However, the expressions (9) and (10) are valued only if PLL is the stable system. PLL is stable system if the poles $|z_1| < 1$ and $|z_2| < 1$, where z_1 and z_2 are the zeroes of the polynomial $z^2 + z(a + b-1)-a$ in (5) and (7), i.e.

$$z_{1/2} = \frac{-(a+b-1) \pm \sqrt{(a+b-1)^2 + 4a}}{2}. \quad (11)$$

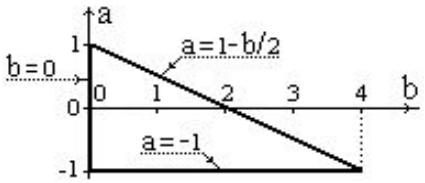

Fig. 2. The region of parameters "a" and "b" for the stable PLL.

The conditions $|z_1| < 1$ and $|z_2| < 1$ define the region in the plane of parameters "a" and "b", where PLL is the stable system. This region, shown in Fig. 2, is located between three mathematical straight lines defined by a = -1, b = 0 and a = 1-b/2.

IV. REALIZATION OF PLL

The hardware organization of PLL is shown in Fig. 3. PLL consists of two Up-down counters, Programmable Period Generator (PPG), generator of control signals and NAND logic circuits. The functioning of PPG is described in ref. [3].

Let us remember that PPG is based on Up-down counter and that TO of signal Sop is $TO = N_d * t_c$. N_d is the decimal value of binary code N_b and t_c is the period of clock, i.e. $t_c = 1/f_c$. To explain the scheme in Fig. 3, let us transform (2) into $TO_{k+1} = (a + b)\tau_{k+1} - a\tau_k$ and change $a + b = f_{a+b}/f_c$ and $b = f_b/f_c$. Equation (2) will get the suitable form for realization:

$$f_c TO_{k+1} = f_{a+b}{}^{2}_{k+1} - f_a{}^{2}_{k}. \quad (12)$$

It can be seen from (12) that three clock signals S_c, S_{a+b} and S_a with the frequencies respectively f_c, f_{a+b} and f_a are to be used in the realization of PLL shown in Fig. 3. Note that the clock signals S_c, S_{a+b} and S_a are changed in Fig. 3 by their frequencies intentionally. All of three members of (12)

are the ordinary numbers. It follows from (12) that TO_{k+1} is generated by PPG using clock frequency f_c, τ_{k+1} is measured by the frequency f_{a+b} and τ_k is measured using frequency f_a. All these conclusions are applied in the realization of PLL, shown in Fig. 3.

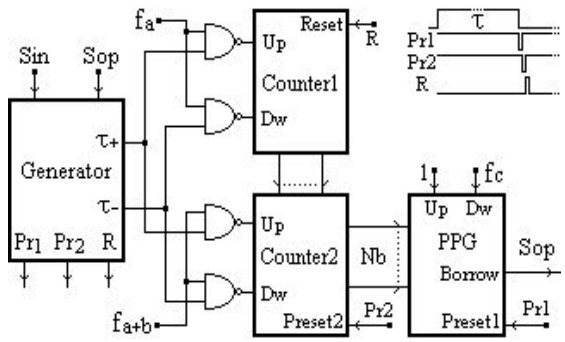

Fig. 3. The functional scheme of PLL of the second order.

The generator of the time differences τ_+, τ_- and control signals Pr1, Pr2 and R, according to its function in PLL, changes the role of a comparator in a standard analog PLL. It generates all outputs using Sin and Sop. Slightly different version of generator is described in ref. [1]. Since the time difference τ can be positive τ_+ and negative τ_- as well, it was necessary to generate them on separate lines and to provide either addition or subtraction, just like in Fig. 3. The relations between time difference τ, Pr1, Pr2 and R are shown in Fig. 3.

The functioning of the generator and PLL is presented in Fig. 4. The picture is made on the realized eight-bit PLL. The voltage waveforms in Fig. 4 are taken when PLL was in the stable state. For this purpose, it was chosen a = 0 (τ_k is not used), b = 1 ($f_b = f_c$). Choosing these parameters, according to (10), τ_∞ = TI.

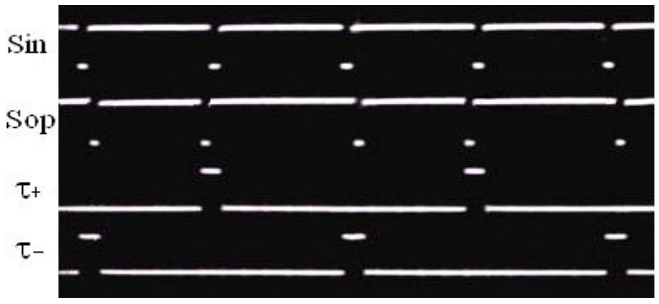

Fig. 4. Generations of Sop, τ_+ and τ_- are visible.

PLL will lock with phase difference 2π, according to (10). The ratio TI/t_c is only about 7. Small ratio between TI and t_c is chosen to enable the visible width of τ_+ and τ_-. The sign of "τ" is changing every period. Periods TO(k) tend to reach TI(k), but that is not possible, because the ratio TI/tc is very small. It can also be seen that whenever two pulses of Sop occur during a period TI, it means that the TI > TO, "τ" is positive and next TO is increased. If two pulses of Sin comes during a period TO, it means that TO > TI, "τ" is negative and next TO is decreased. The previous explanations represent, at the same time, the complete description of functioning of generator. If TI/t_c increases, the widths of τ_+ and τ_- would decrease and tend to zero. For the stable PLL the content of UP-down counter 2 represents the measured TI and, at the same time, the output period TO, since TO = TI.

Every "τ" is measured instantaneously in both counter 1 and counter 2. Measuring "τ" counter 2 generates TO_{k+1}. Counter 1 memorizes "τ" for the next calculation of period TO_{k+1}. Pulses Pr1, Pr2 and R, shown in Fig. 3, provide the functioning of PLL. As soon as the calculation of TO is finished, pulse Pr1 presets the content of counter 2 to PPG. Immediately after that, pulse Pr2 presets the content of counter 1 into counter 2. At last pulse R resets counter 1, preparing it for the next measurement of τ_k.

V. Simulation and Application of PLL

The simulation of FLL functioning has two important aims. The first one is to discover additional properties of PLL and its possible efficient applications. The second one is to enable better insight into the physical procedure and meaning of the variables described, as well as to prove the mathematical analyses described. All discrete values in simulations are merged to form continuous curves.

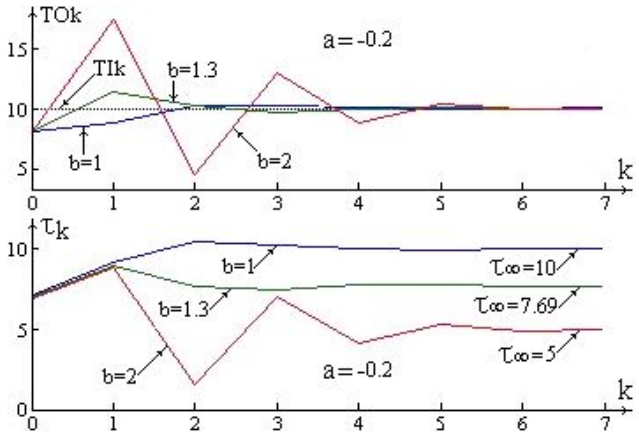

Fig. 5. TO(k) tends to TI and τ(k) tends to TI/b.

The simulation of the output period TO(k), and the time difference τ(k) for TI(k) = 10 time units (t.u.), according to (2) and (1) and for a = -0.2 and different "b", are shown in Fig. 5. The initial conditions are TO_0 = 8 t.u., τ_0 = 7 t.u. Note that time unit can be, μsec, msec or any other, assuming the same time units for TI, TO and τ. The output periods TO(k) tend to TI(k) and τ(k) tends to τ_∞ = TI/b. The simulation results prove the correctness of (9), (10) and all previous mathematical analyses.

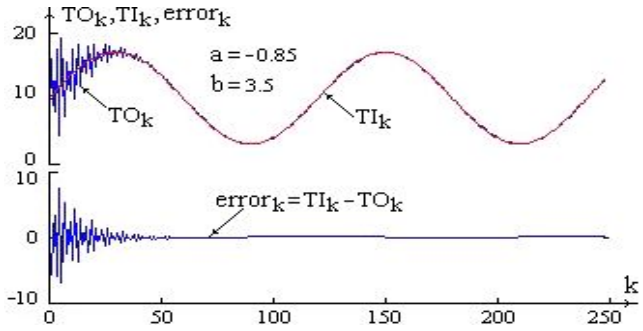

Fig. 6. The tracking error of the sinusoidal signal is very small.

The simulation of TO(k) and error(k) = TI(k) - TO(k) for TI(k) = 10 t.u. + 7*sin[(2π/120)*k] t.u. is shown in Fig. 6. It

can be seen that, excepting the transient state of the locking procedure, the output TO tracks the input TI with very small error, regardless that sinusoidal signal changes intensively the value and sign of the mathematical coefficient direction.

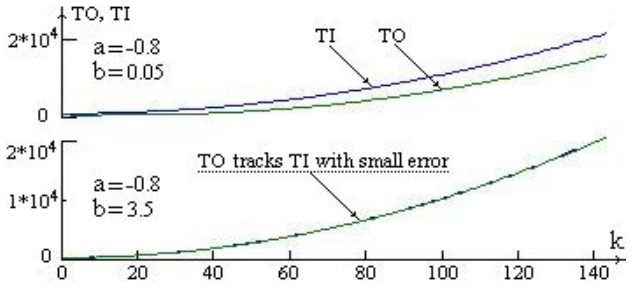

Fig. 7. The tracking of the rapidly growing input for different "b".

The illustration of high tracking performance of PLL is demonstrated in Fig. 7. The output TO tracks the rapidly growing input $TI(k) = (200 + k^2)$ t.u. for a = -0.8 = constant. It can be seen that for small b = 0.05, the tracking error is visible, but for b = 3.5, the tracking error is very small.

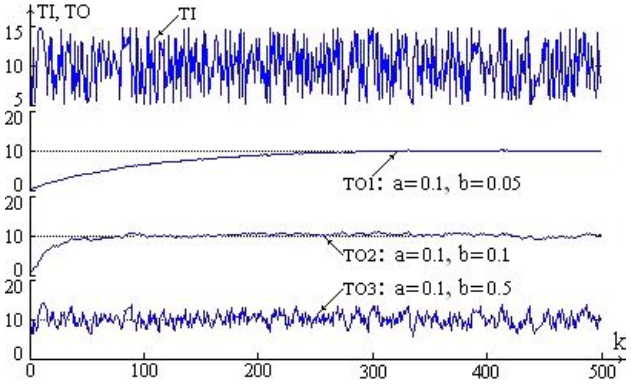

Fig. 8. For the lower "b" noise rejection is better, but PLL is slower.

To illustrate the noise rejection performance of PLL, the transient and stable state of TO(k) is shown in Fig. 8. The input period TI(k) is the step of 10 t.u., which is strongly corrupted by uniform distributed noise. The amplitude of noise is 10 t.u. peak to peak. Three outputs TO_1, TO_2 and TO_3 are generated for the same input TI, the same a = 0.1 and for the different parameters "b", which are shown in Fig. 8. It can be seen from Fig. 8 that PLL possesses power noise rejection ability. The lower "b" provides better noise rejection, but it makes the longer transient state of PLL.

VI. CONCLUSIONS

The description and illustrations of the realized PLL of the second order represent a new approach to the design of PLL in both theoretical and practical sense. In comparison with the existing PLL described in the literature, this PLL represents one fundamentally different approach to theory, construction, methods of description, processing of signals and way of analysis. It also represents a novelty in the way of measurement of error and in the way of functioning and realization of PLL components. For instance the error and the output of PLL, which are usually respectively phase and frequency, are changed by the time difference and the output period. The input frequency is changed by the input period. All the measurement of the phase, the amplitude and the frequency difference in the existing approaches of PLL are changed by the measurement of time. Note that the time measurement is more convenient, easier and more precise in the comparison with the measurement of the phase, the frequency or the amplitude.

The description and illustrations of PLL also showed that PLL is widely applicable. PLL possesses the power tracking ability if the parameters "a" and "b" are close to the values "a" $\rightarrow$ -1 and "b" $\rightarrow$ 4. However if "a" $\rightarrow$ 0 and "b" $\rightarrow$ 0, PLL possesses the power noise rejection ability. At last, PLL is the fastest if "a" = 0 and "b" = 1. In this case PLL takes only two steps to reach the stable state.

It is obvious that, depending on the field of application, one should carefully choose the parameters of PLL, making the trade-off of them, to adapt PLL to the specific application. The analysis of PLL properties should be continued in order to expand the area of its application.

REFERENCES

[1] D. M. Perisic, A. Zoric, D. Babic, D. D. Perisic, "Recursive PLL of the first order", *Electrical Review*, no. 7, pp. 50–53, 2013.

[2] D. M. Perisic, A. Zoric, S. Obradovic, D. D. Perisic, "FLL as digital period synthesizer based on binary rate multiplier control", *Electrical Review*, no. 1a, pp. 145–148, 2013.

[3] D. M. Perisic, A. Zoric, S. Obradovic, P. Spalevic, "Application of frequency locked loop in consumption peak load control", *Electrical Review*, no. 1b, pp. 264–267, 2012.

[4] D. M. Perisic, A. Zoric, S. Obradovic, D. D. Perisic, "Pulse rate averaging based on digital frequency locked loop", in *Proc. Int. Scientific Conf. (UNITECH 2011)*, TU-Gabrovo, Gabrovo Bulgaria, vol. 1, 2011, pp. I-192–I-195.

[5] A. Raicevic, B. Popovic, "PLL as the frequency synthesizer with continuous phase divider", *Elektronika ir Elektrotechnika*, no. 5, pp. 47–50, 2009.

[6] D. Abramovitch, "Phase-locked loops: a control centric tutorial", *Proc. American Control Conf.*, 2002, vol. 1, pp. 1–15.

[7] M. Pastor, J. Dudrik, "Grid-tied 15-level cascade inverter with predictive current control", *Elektronika ir Elektrotechnika*, vol. 18, no. 9, pp. 19–22, 2012. [Online]. Available: http://dx.doi.org/10.5755/j01.eee.18.9.2798

[8] Q. X. Guo, Y. W. Wu, R. H. Gu, "Phase locked loop and simulation methods for grid interfaced converters", *A Review, in Electrical Review*, no. 4, pp. 182–187, 2011.

[9] N. R. Dean, K. A. Rane, "Digital frequency-locked loop system for capacitance measurement", *IEEE Trans. Instrumentation and Measurement*, vol. 62, no. 4, pp. 777–784, 2013. [Online]. Available: http://dx.doi.org/10.1109/TIM.2013.2240092

[10] D. Jovcic, "Phase locked loop system for FACTS", *IEEE Trans. Power System*, vol. 18, no. 3, pp. 2116–2124, 2003. [Online]. Available: http://dx.doi.org/10.1109/TPWRS.2003.814885

[11] L. Joonsuk, B. Kim, "A low noise fast-lock phase-locked loop with adaptive bandwith control-solid-state circuit", *IEEE Journal*, vol. 35, no. 8, pp. 1137–1145, 2000.

[12] J. T. Curran, G. Lachapelle, C. C. Murphy, "Improving the design of frequency locked loops for GNSS receivers", *IEEE Trans. Aerospace and Electronic Systems*, vol. 48, no. 1, pp. 850–868, 2012. [Online]. Available: http://dx.doi.org/10.1109/TAES.2012.6129674

[13] G. Bianchi, *Phase-Locked Loop Synthesizer Simulation*, Nc-Hill, Inc: New York, USA, 2005.

[14] R. Vich, *Z Transform Theory and Application (Mathematics and Applications)*, Ed. Springer, 1987.

[15] B. D. Talbot, *Frequency Acquisition Techniques for Phase Locked Loops*, Wiley-IEEE Press, 2012. [Online]. Available: http://dx.doi.org/10.1002/9781118383285