Power Balancing Mechanism and Controller Design for the Single-Phase Cascaded H-bridge Multilevel DSTATCOM

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***Abstract*—The power balancing mechanism and the effective voltage balancing control algorithm are presented for the single-phase cascaded H-bridge multilevel DSTATCOM. The dc voltage balancing control for CHB-DSTATCOM is splitted into the average voltage controller and the voltage balancing controller, which are designed to regulate the active power flow between the CHB-DSTATCOM with the grid and to regulate active power flow among each inverter units, respectively. The effectiveness of the control algorithm is validated by the simulation results.**

***Index Terms*—Cascade H-bridge, multilevel, DSTATCOM, power quality, power balancing control, Matlab/Simulink**

I. INTRODUCTION

Due to the proliferation of power-electronic equipment, the amount of harmonic currents flowing into electrical distribution networks is growing rapidly in recent decades. These nonlinear loads draw non-sinusoidal currents from the distribution networks, which causes interference to the sensitive loads connected at the point of common coupling (PCC) and limits the available electrical supply [1].

Recently, the multilevel and multi-cell voltage source inverters (VSI) are increasingly used for the power quality conditioners [2]. These multilevel inverters, which benefit from several advantages such as low switching ripple, low conduction losses and small *dv/dt*, effectively improve the bandwidth of the compensators [3]. Due to its modularity and flexibility of manufacturing, the cascaded H-bridge (CHB) multilevel inverter topology is appreciated for high-power power quality conditioning applications. However, restricted by the limited switching frequency of the power semiconductors, achieving dc capacitor voltage balancing and sufficient controller bandwidth is complicated [2], [3].

The design guidelines for CHB-DSTATCOM have not been addressed in the previous literatures. This paper aims to cover this gap. The theoretical analysis for the power balancing among the H-bridge modules is presented. A novel dc-link voltage balancing technique is proposed by splitting the dc-link voltage control task into two parts, namely, the average voltage controller (AVC) and the voltage balancing controller (VBC). The simulation results of the CHB-DSTATCOM for power quality compensation is presented, which validates the validity and effectiveness of the devised algorithm.

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II. SYSTEM DESCRIPTION OF THE CHB-DSTATCOM

Fig. 1 shows the circuit diagram of the single-phase multilevel cascaded H-bridge (CHB) DSTATCOM. Each H-bridge inverter consists of four IGBTs and anti-parallel diodes, and the dc-link capacitors and their equivalent resistances. In Fig. 1, v_{sa} denotes the grid voltage at the point of common coupling, L and r_L indicate the coupling inductance and its equivalent resistance, $v_{dc,i}$ and R_{Ci} denote the dc-link capacitor and its equivalent parallel resistance for the ith H-bridge, v_{Hi} and v_{HN} denote the output voltage of the ith H-bridge and the synthesized multilevel voltage, and i_c indicates the output current of the CHB-DSTATCOM [2]–[4].

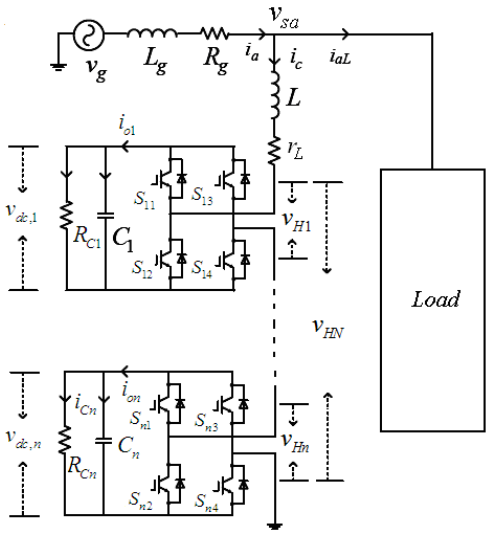


Fig. 1. The circuit diagram of the cascaded DSTATCOM based on n-block H-bridge modules.

According to the Kirchhoff's Law, we get [2], [3]

$$\dot{i}_c = \frac{1}{L}\left[v_{sa} - r_L i_c - \sum_{i=1}^{n} f_i v_{dc,i}\right], \dot{v}_{dc,i} = \frac{1}{C_i}\left(f_i i_c - v_{dc,i}/R_{Ci}\right), i = 1,2,...,n, \quad (1)$$

where f_i denotes the switching function of the ith H-bridge inverter, and f_i can be represented as

$$f_i = S_{i1} \times S_{i4} - S_{i2} \times S_{i3}, i = 1,2,...,n, \quad (2)$$

where S_{ik} (i=1, $\cdots n$; k=1, $\cdots 4$) $\in \{0, 1\}$ denotes the switching states of the kth IGBT for the ith H-bridge inverter, and we have f_i={-1;0;1}, corresponding to the charging and discharging process of the dc-link capacitors. When f_i=±1, the dc-link capacitor of the ith H-bridge undergoes charging or discharging process. When f_i=0, there is no charging or discharging process for the dc-link capacitor of the ith H-bridge. The voltages v_{Hi} and v_{HN} can be denoted as

$$v_{Hi} = f_i v_{dc,i}, v_{HN} = \sum_{i=1}^{n} v_{Hi}, i = 1,2...,n. \quad (3)$$

III. POWER BALANCING CONTROLLER DESIGN METHODOLOGY

Fig. 2 shows the vector diagram of the output voltages of each inverter unit and the injection current. The fictitious d-q reference frame is set up based on the vectors of the DSTATCOM current $\vec{I}_c$ and the grid voltage $\vec{V}_{sa}$.

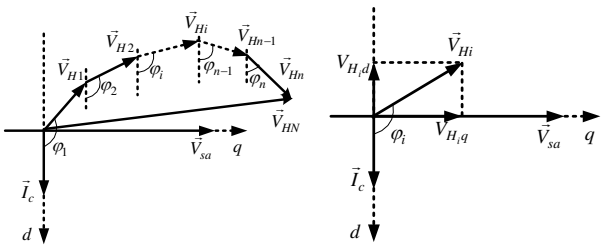


Fig. 2. Phasorial representation of the individual H-bridge voltage and the injection current.

The variables $\vec{V}_{Hi}$ and φ_i denote the output voltage vector of the ith H-bridge and the phase angle between the nearby voltage vectors, and $\vec{V}_{HN}$ denotes the vector of the fundamental component of the synthesized multilevel voltage, hence the ac-side output active and reactive power of the ith H-bridge inverter unit are derived as

$$P_i = V_{H_i} \cdot I_c \cdot \cos\varphi_i = V_{H_i d} \cdot I_c, Q_i = V_{H_i} \cdot I_c \cdot \sin\varphi_i = V_{H_i q} \cdot I_c. \quad (4)$$

It can be deduced from (4) that, the d-axis and q-axis components of the output voltage are proportional to the fundamental active and reactive power injection of the ith H-bridge. Notably, the reactive current flowing across each inverter module is identical, thus the q-axis component of the output voltage of each inverter must be identical in order to equally distribute the reactive power among the inverter units, hence we get

$$V_{H_i q} = V_{HNq}/n, i = 1,2,...,n. \quad (5)$$

On the other hand, it can be observed from Fig. 2 and (4) that the total active power P_{total} is equally distributed among the H-bridge units when the d-axis components of the inverter output voltages are equally distributed, i.e., we have

$$P_i = P_{Hav} = P_{total}/n, i = 1,2,...,n, \quad (6)$$

where P_{Hav} the averaged active power of each H-bridge inverter, and the d-axis projection of inverter output voltages V_{Hid} can be denoted as

$$V_{Hid} = V_{Hdav} = V_{HNd}/n, \quad (7)$$

where V_{Hav} indicates the averaged output voltage of each H-bridge inverter.

Since the equivalent switching losses of each H-bridge inverter are different and the dc-link capacitances are not necessarily same, the active power sharing of the individual H-bridge unit may not be same during dynamic process, hence the active power for the ith inverter P_i is denoted as

$$P_i = V_{H_i d} \bullet I_c = (V_{Hdav} + \Delta V_{H_i d}) \bullet I_c = P_{Hav} + \Delta P_i = P_{total}/n + \Delta P_i, \quad (8)$$

where ΔP_i indicates the difference of the active power and averaged active power for the ith H-bridge inverter P_i and P_{Hav}, respectively. In case of $\Delta P_i \neq 0$, the output voltage for the ith H-bridge inverter needs to be modified, thus the d-axis component of the active power difference ΔV_{Hid} can be derived as

$$\Delta V_{H_i d} = (P_i - P_{Hav})/I_c. \quad (9)$$

In order to ensure the total active power P_{total} generated by each inverter units remain constant, the active power difference must be zero. Further, the sum of the d-axis components of active power differences should also be zero. Hence, we get

$$\sum_{i=1}^{n} \Delta P_i = 0, \sum_{i=1}^{n} \Delta V_{H_i d} = 0. \quad (10)$$

Based on the analysis of (4)–(10), the dc-link averaged active power control and reference current generation block diagrams can be devised, as shown in Fig. 3. Notably, the block diagram in Fig. 3 is used for synthesizing the average reference voltage to adjust the active power flow between the CHB-DSTATCOM with the grid.

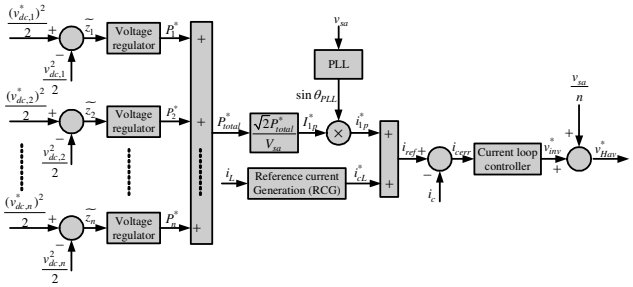


Fig. 3. The block diagram of dc-side average active power control and reference current generation.

Fig. 4 shows the block diagram of the voltage balancing controller, which is responsible for active power balancing among the individual H-bridge units, thus generates the difference voltage reference.

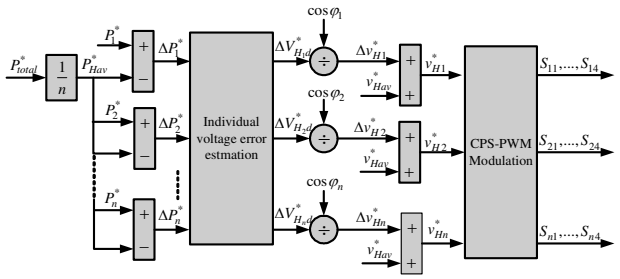


Fig. 4. The block diagram of the dc-link voltage balancing strategy of the CHB-DSTATCOM.

Obviously, the generating of reference active power P_i^* is the critically important; hence the derivation of this quantity is outlined herein. From Fig. 1, the dc-link power flow equation for each H-bridge is denoted as

$$P_i^* = C_i \dot{z}_i + \frac{2z_i}{R_{Ci}}, i = 1,2,...,n, \tag{11}$$

where $z_i = v_{dc,i}^2 / 2$, $\dot{z}_i = v_{dc,i}\dot{v}_{dc,i}$. (11) denotes the typical first-order filter, which belongs to the linear time-invariant (LTI) system, where P_i^* indicates the actual control signal, i.e., the output of the voltage regulator in Fig. 3.

In order to derive the power balancing regulator, we define the intermediate variable ζ_i, and the following equations are obtained:

$$\begin{cases} \dot{P}_i^* = K_{Ii}\tilde{z}_i - K_{Pi}\zeta_i, \\ \dot{\zeta}_i = -b_i\zeta_i - a_i\dot{\tilde{z}}_i, \end{cases} \tag{12}$$

where $\tilde{z}_i \triangleq z_i^* - z_i$, $z_i^* = (v_{dc,i}^*)^2/2$, $v_{dc,i}^*$ indicates the dc-link reference value for the ith inverter, and the parameters K_{Pi}, K_{Ii}, a_i, b_i need to be designed. The derivative of P_i^* is obtained as

$$\ddot{P}_i^* = K_{Ii}\dot{\tilde{z}}_i - K_{Pi}\dot{\zeta}_i. \tag{13}$$

From (12) and (13), we get

$$\ddot{P}_i^* = K_{Ii}\dot{\tilde{z}}_i - K_{Pi}(-b_i\zeta_i - a_i\dot{\tilde{z}}_i). \tag{14}$$

Substituting (12) into (14), we get

$$\begin{aligned} \ddot{P}_i^* &= K_{Ii}\dot{\tilde{z}}_i + K_{Pi}a_i\dot{\tilde{z}}_i + b_i(-\dot{P}_i^* + K_{Ii}\tilde{z}_i) = \\ &= (K_{Ii} + K_{Pi}a_i)\dot{\tilde{z}}_i + b_iK_{Ii}\tilde{z}_i - b_i\dot{P}_i^*. \end{aligned} \tag{15}$$

Let $\tilde{z}_i$ and P_i^* be the input and output of the voltage regulator, the second order integration of (15) can be derived as

$$P_i^* = \frac{K_{Ii}}{s}\tilde{z}_i + \frac{K_{Pi}a_i}{s+b_i}\tilde{z}_i. \tag{16}$$

(16) can be rewritten as

$$P_i^* = \frac{K_{Ii}}{s}\tilde{z}_i + \frac{K_{Pi}}{s+\tau_i}\tilde{z}_i, i = 1,2,...,n, \tag{17}$$

where K_{Pi} and K_{Ii} indicate the proportional and integral constant of the ith voltage regulator, τ_i denotes the time constant. The active current reference i_{1p}^* can be derived as

$$i_{1p}^* = I_{1p}^* \sin\theta_{PLL} = \frac{\sqrt{2}P_{total}^*}{V_{sa}}\sin\theta_{PLL} = \frac{\sqrt{2}\sum P_i^*}{V_{sa}}\sin\theta_{PLL}, \tag{18}$$

where V_{sa} denotes the RMS values of v_{sa}, and θ_{PLL} indicates the phase angle obtained from PLL, which is synchronized with the fundamental component of the grid voltage [2]. On the other hand, the reactive and harmonic component of the load current can be derived from the RCG block, hence the total reference current is derived and the averaged voltage reference can be derived from the current regulator [3], [4].

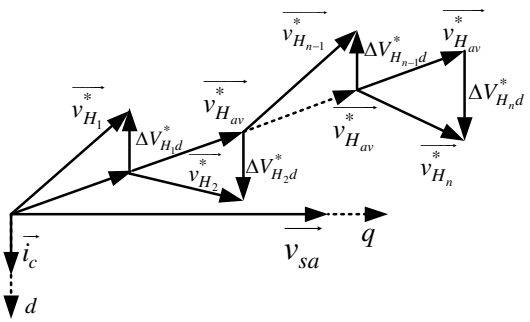


Fig. 5. The vectorial analysis of the voltage balancing scheme for the CHB-DSTATCOM.

In order to achieve dc-link voltage balancing when the dc-link capacitor and equivalent switching losses are different, the difference between the averaged active power P_{Hav}^* and the individual active power P_i^* of the ith H-bridge is utilized to derive the control block diagram (Fig. 4). The d-axis projection ΔV_{Hid}^* is converted back to the direction of the vector v_{Hi}, hence we get

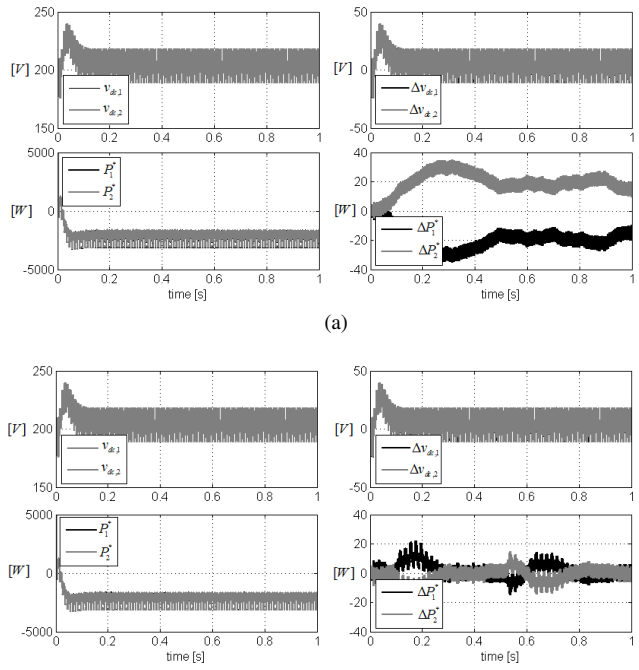
$$\Delta v_{Hi}^* = \Delta V_{Hid}^* / \cos\varphi_i, \tag{19}$$

where φ_i denotes the phase angle between the vectors of v_{Hi} and i_{Lq}. Notably, the phase angle φ_i is constant when the load is decided. The modulation signal v_{Hi}^* is formed by adding the output of voltage balancing controller to the output of average voltage controller.

Fig. 5 shows the vectorial diagram of the voltage balancing control scheme. Notably, the voltage balancing can be ensured when (10) is satisfied. The obtained signals are used to synthesize the phase-shifted PWM signals to drive the IGBTs S_{i1}~S_{i4} [2], [3].

IV. SIMULATION RESULTS AND DISCUSSIONS

To validate the effectiveness of the control algorithms, the two-block CHB-DSTATCOM is simulated using Matlab/Simulink [2]–[4]. The grid voltage is 220V, the dc parameters are: C_1=C_2=2000μF, the coupling inductance L=1.2mH, and the diode rectifier load is connected, with the current limiting inductance of 2mH, and the RC-type load with R=10Ω, C=10000μF is connected to the rectifier. The target dc-link voltage is set as 200V.



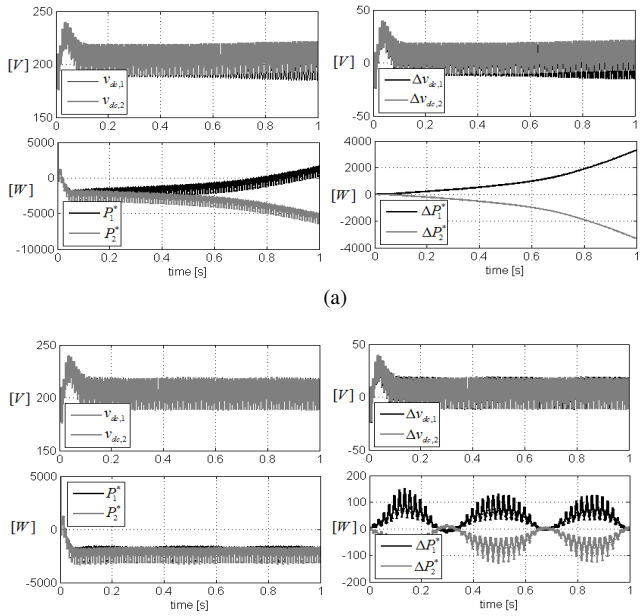
(a)

(b)

Fig. 6. The individual and average dc-link voltages, and the active power reference under homogeneous H-bridges scenarios: (a) only the average active power regulator is enabled; (b) both the dc-link average active power regulator and the voltage balancing controller are activated.

Fig. 6 The individual and average dc-link voltages, and the active power reference under homogeneous H-bridges scenarios. In Fig. 6, the dc-link equivalent resistances are R_{C1}=R_{C2}=3.9kΩ. The dc-link voltages and active powers, and the differences between the references and the actual values in the dc-link voltages and active powers are given for the two cases. In the first case, only the average voltage controller is activated, and in the second case, both average voltage controller and the voltage balancing controller are activated, as shown in Fig. 6(a) and Fig. 6(b), respectively. It shows that the dc-link voltages and the dc-link active powers converge to the preset values under the two cases. Besides, the difference in the active power converges to zero when the voltage balancing controller is active, as shown in Fig. 6(b).

Fig. 7 shows the simulation results of the DSTATCOM for reactive and harmonic compensation when the dc-link resistances are R_{C1}=0.78kΩ, R_{C2}=3.9kΩ. Notably, Fig. 7(a) shows the case when only the average voltage controller is enabled, and Fig. 7(b) shows the case when both the average voltage controller and voltage balancing controller are activated. It can be observed from Fig. 7(a) that the dc-link difference voltages $\Delta v_{dc,1}$, $\Delta v_{dc,2}$ and the active power differences diverge, indicating the dc-link voltages diverge when only average voltage controller is enabled. However, when the voltage balancing controller is enabled, the voltage differences converge to zero, and the dc-link active powers are controlled to the constant value of -3500W, with the fluctuation of ±2.8%, as shown in Fig. 7(b).



(a)

(b)

Fig. 7. The individual and average dc-link voltage, active power reference under different dc-link parallel resistors scenarios: (a) only with dc-side average active power regulator; (b) with both the dc-side average active power regulator and the voltage balancing controller.

V. CONCLUSIONS

The power balancing mechanism is analysed for the single-phase cascaded H-bridge multilevel DSTATCOM. The dc voltage balancing control for CHB-DSTATCOM is splitted into the average voltage controller and the voltage balancing controller, which are designed to regulate the active power flow between the CHB-DSTATCOM with the grid and to regulate active power flow among each inverter units, respectively. The validity of the devised control algorithm is validated by the simulation results.

The presented CHB-DSTATCOM can be widely applied for power quality conditioning applications in industrial distribution networks and the renewable energy resources, such as wind power, photovoltaic (PV) systems, etc.

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