A 0.49 mm^2 CMOS Low-Power TVCO Achieving FoM of 190.36 dBc/Hz for 5G New Radio Application

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***Abstract*—This paper describes the implementation of low-power, low-phase-noise (PN), and robust startup tailless class-C voltage-controlled oscillator (TVCO) for 5G new radio (NR) technology. It features dual gate voltage control source biasing to generate fast startup and differential signal amplitude balancing, thus eliminating the requirement of the conventional tail current source, which introduces more parasitic capacitance that affects the oscillation frequency, phase noise, and power consumption. The TVCO is fabricated in 180 nm complementary metal-oxide semiconductor (CMOS) technology, oscillating at 2.59 GHz 5G NR carrier frequency with an output voltage swing of 1.7 V and low-phase-noise of -122 dBc/Hz at 1 MHz offset with supply voltage headroom of 0.7 V. Without additional features added, the TVCO consumes very low-power and a small die area of 0.98 mW and 0.49 mm^2, respectively. The achieved figure of merit (FoM) is 190.36 dBc/Hz.**

***Index Terms*—5G NR; Class-C; LC VCO; Tail current source; Flicker noise.**

I. INTRODUCTION

The 5G new radio (NR) technologies are currently the cutting-edge high-data rate wireless communication transmission system due to their low latency characteristics [1]. The frequency bands involved for 5G are divided into two different spectrums: sub-6 GHz and mmWave [2]. High-data rate transmission consumes substantial power [3]–[8]. As the developments are rapid for 5G NR radio systems, the voltage-controlled oscillator (VCO) has been identified as one of the power-hungry blocks, and research works focus on achieving optimal balance performance in terms of high energy efficiency, low-phase-noise, and operating bandwidth [9]–[19]. The inductor-capacitor (LC) VCO is a preferred solution to attain the operating bandwidth for the 5G NR radio system. Due to its power-hungry nature, operating the LC VCO in Class-C mode is quite prevalent [15], [16]. However, these Class-C oscillators suffer phase noise and startup due to low biasing, which was intended to reduce the VCO power consumption. Other efforts to reduce the power consumption of the VCO are near the threshold biasing mechanism [17], the use of the inversion metal-oxide semiconductor (IMOS) varactor [18], and the active load [19]. However, the trade-off between phase noise and power consumption remains eminent. The main contributor to VCO phase noise and output voltage swing is the tail current source [20]–[23]. The tail current source adds additional parasitic components to the VCO circuit besides the source coupled pair (XCP) transistors. Nevertheless, it is popular, as it ensures a balance oscillation between two differential outputs.

The functionality of low-power VCO with balanced output and fast startup is vital to protect the efficiency of the overall 5G NR transceiver system [24], [25]. Therefore, this work proposes a tailless Class-C voltage-controlled oscillator (TVCO) to reduce the phase noise and power consumption trade-off. A comprehensive analysis has been performed to determine the oscillation frequency and flicker noise, including the parasitic effects, followed by the figure of merit (FoM) calculation, which defines the trade-off between phase noise and power consumption. A dual gate voltage control source is implemented to ensure balanced output for differential amplifiers.

This paper is organized as follows. Section II describes the mode of operation with the analysis of the proposed TVCO, followed by Section III, which represents the flicker noise analysis of the proposed architecture. Next, Section IV represents the simulation and measurement results, and conclusions are drawn in Section V.

II. PRINCIPLE OF OPERATION

The TVCO schematic is illustrated in Fig. 1. It consists of a high-Q LC tuner, cross-coupled pair n-type metal-oxide semiconductor (nMOS) M_1 and M_2, each having its respective gate controllers V_{C1} and V_{C2}. V_{C1} and V_{C2} play an essential role in ensuring fast startup. The L_1, C_{var1}, and C_{var2} represent the resonant tank tuned under tuning voltage,

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V_{TUNE} adjusted in the range of 0.1 V–1.8 V. The location of the parasitic capacitances C_{gd} (gate-drain), Cgs (gate-source), and Cdb (drain-bulk) are also included for theoretical analysis. Without the conventional tail current source, the parasitic capacitances are reduced, thus improving the output voltage swing and reducing the phase noise of the low-power Class-C VCO.

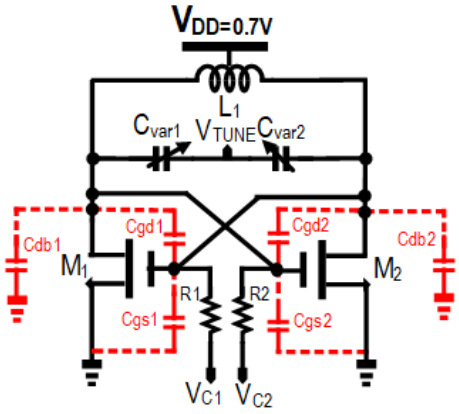

Fig. 1. Schematic of the TVCO.

Figure 2 illustrates the small signal model of the TVCO. With the aid of an external voltage source, antisymmetrical nodal analysis is performed to determine the true oscillation frequency, $\omega_{OSC,}$ which includes parasitic capacitances.

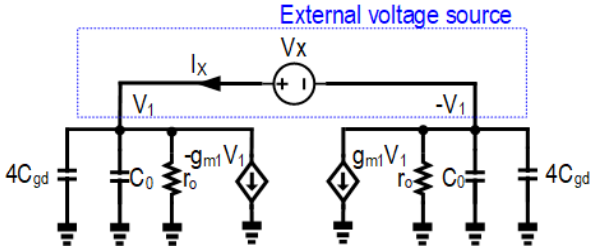

Fig. 2. Small signal model of the TVCO.

The total parasitic capacitances of the tailless XCP VCO are given as

$$C_o = C_{db} + C_{gs}. \tag{1}$$

Since V_1 and $-V_1$ are antisymmetrical nodes, the input admittance Y_{IN} can be computed as

$$Y_{IN} = \frac{i_x}{v_x} = -\frac{g_m}{2}\left(1-\frac{1}{g_m ro}\right)+\frac{1}{2}j\omega\left(C_{db}+C_{gs}+4C_{gd}\right). \tag{2}$$

Figure 3 illustrates the simplified TVCO model where R and C_{XCP} represent the real and imaginary of (2). From this, the oscillation frequency ω_{OSC} is determined as

$$\omega_{osc} = \frac{1}{\sqrt{L\left(C_{Var}+C_{XCP}\right)R}}, \tag{3}$$

where R and C_{XCP} are given in (4) and (5), respectively:

$$R = -\frac{2}{g_m}\left(1-\frac{1}{g_m ro}\right), \tag{4}$$

$$C_{XCP} = 2\left(C_{db}+C_{gs}+4C_{gd}\right). \tag{5}$$

Inserting (4) and (5) into (3) results in the true oscillation frequency, given in (6)

$$f_{OSC} = \frac{1}{2\pi\sqrt{-\frac{2}{g_m}\left(1-\frac{1}{g_m ro}\right)L\left(C_{Var}+2\left(C_{db}+C_{gs}+4C_{gd}\right)\right)}} \tag{6}$$

with $f_{OSC,}$ the figure of merit (FoM) of the TVCO is given as

$$FoM = L(\Delta f) - 20\log\left(\frac{f_{OSC}}{\Delta f}\right)+10\log\left(\frac{P_{diss}}{mW}\right), \tag{7}$$

where L is the phase noise in Δf offset frequency, and P_{diss} is the power dissipation.

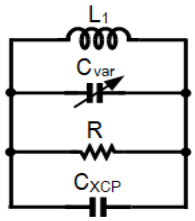

Fig. 3. Simplified model of the TVCO.

Figure 4 shows the comparison of startup G_m between conventional Class-C and TVCO. The TVCO has a higher G_m for all three process corners than the conventional Class-C VCO due to the reduced parasitic capacitance at the gate of M_1 and M_2.

The dual gate biasing method manoeuvres the $Cgs_{1,2}$ as such, it works as part of a low-pass filter (LPF) once integrated with resistor $R_{1,2}$. The $R_{1,2}$-$Cgs_{1,2}$ LPF too significantly reduces the high-frequency noise and hence contributes to fast startup. Accordingly, a balance amplitude swing is obtained.

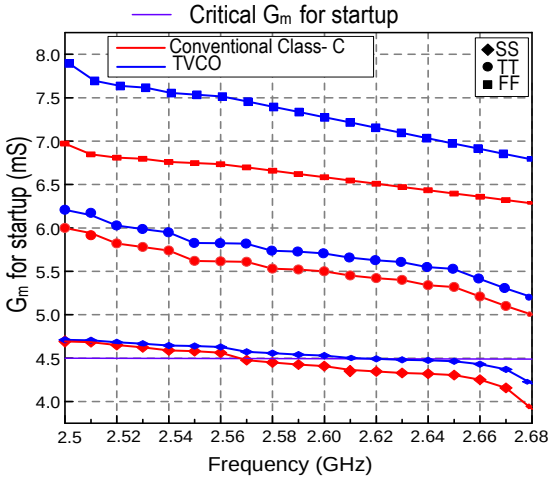

Fig. 4. Simulated small signal Gm versus frequency at different process corners (SS, TT, FF) for a conventional Class-C VCO and TVCO.

III. TVCO FLICKER NOISE ANALYSIS

Figure 5 illustrates the simplified half small signal of the flicker (1/f) noise model of TVCO.

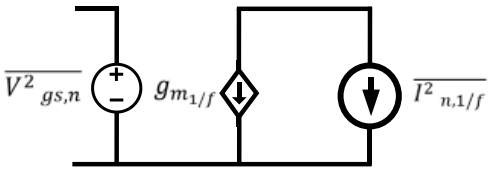

Fig. 5. Small signal of the 1/f noise model of the TVCO.

The noise voltage at the $M_{1,2}$ gate is given as

$$\overline{V^2}_{gs,n} = \frac{K}{C_{OX}WL}\left(\frac{1}{f}\right), \tag{8}$$

where K is the complementary metal-oxide semiconductor (CMOS) process constant

$$\mathrm{K} = \frac{q^2 D_t(E_F)KT}{\ln(\tau_2/\tau_1)}, \tag{9}$$

where q is the elementary charge, $D_t(E_F)$ is the active trap density, K is the Boltzmann constant, τ_1 and τ_2 is the trapping time, and T is the temperature in Kelvin.

The *1/f* noise transconductance of $M_{1,2}$ is given as:

$$g^2_{m,1/f} = \frac{\overline{I^2_{n,1/f}}}{\overline{V^2_{gs,n}}}, \tag{10}$$

$$\overline{I^2_{n,1/f}} = g^2_{m,1/f} \times \frac{K}{C_{ox}WL} \times \frac{1}{f}. \tag{11}$$

The total noise current from 1 kHz to 1 MHz is solved as:

$$\overline{I^2_{n,1/f(tot)}} = \frac{Kg^2_{m,1/f}}{C_{ox}WL} \times \int_{1KHz}^{1MHz} \frac{1}{f} df, \tag{12}$$

$$= \frac{Kg^2_{m,1/f}}{C_{ox}WL} \times \left[\ln f\right]_{1KHz}^{1MHz}, \tag{13}$$

$$\overline{I^2_{n,1/f(tot)}} = \frac{6.91Kg^2_{m,1/f}}{C_{ox}WL}, \tag{14}$$

$$g_m = \mu_n C_{ox} \frac{W}{L}\left(V_{gs} - V_{th}\right). \tag{15}$$

Inserting (15) into (14) results in

$$\overline{I^2_{n,1/f(tot)}} = 6.91K\mu_n^2 C_{ox} \frac{W}{L}\left(\frac{V_{GS} - V_{TH}}{L}\right)^2. \tag{16}$$

Equation (16) reveals that the *1/f* noise is highly dependent on the device size (*W/L*) and the gate to source voltage, V_{GS}. Hence, in our work, we reduced the *1/f* noise by lowering the V_{GS} and increasing the device length (*L*) without trading off the area of the chip. Therefore, the *1/f* noise is subsequently decreased, resulting in a lower flicker upconversion to $1/f^2$ (20 dB/dec) and $1/f^3$ (30 dB/dec), thus improving the overall phase noise performance of the TVCO.

Figure 6 illustrates the simulated output waveform of conventional Class-C and TVCO, where the imbalance amplitude is triggered by uneven gate biasing to form a Class-C core operation. Class C's amplitude imbalance and distortion during the triode region generated more flicker noise. With the dual gate control aided in TVCO, a more balanced amplitude waveform and zero distortion have been produced, thus reducing the *1/f* noise. The balanced signal amplitude at their zero-crossing point provides a better phase noise (PN) improvement, becoming less sensitive to injected noise than the Class-C core.

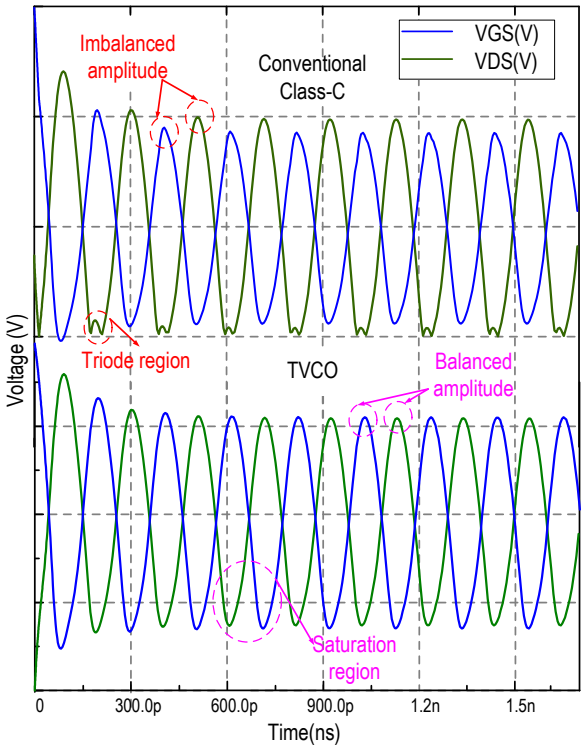

Fig. 6. The simulated transient waveform of the TVCO without and with dual gate voltage biasing mechanism.

IV. SIMULATION AND MEASUREMENT RESULTS

Figure 7 illustrates the micrograph of the TVCO manufactured in the 180 nm radio frequency (RF) CMOS technology process that occupies the core area of 0.49 mm^2, including the bond pads. The measurement setup of the proposed architecture is shown in Fig. 8.

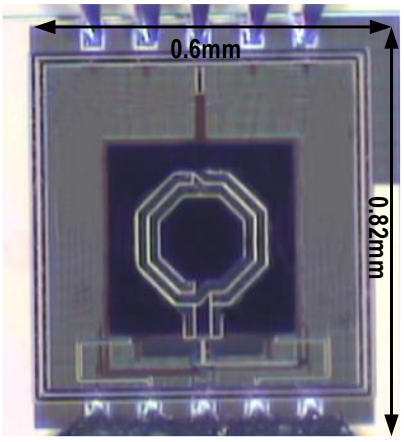

Fig. 7. Photomicrograph of the proposed architecture.

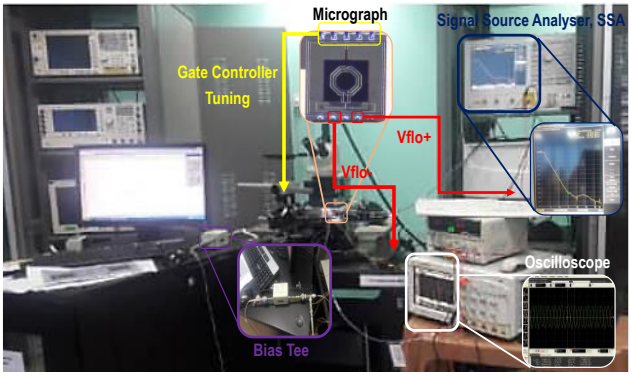

Fig. 8. Measurement setup of the proposed architecture.

Figure 9 plots the result of the simulated and measured PN at 2.59 GHz with a supply voltage headroom of 0.7 V, achieving -122 dBc/Hz in the measured result. A slight drop of 2 dB compared to the simulated result has been observed.

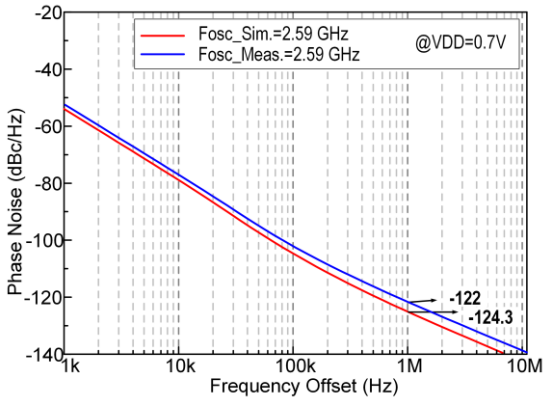

Fig. 9. Simulated and measured PN at center carrier 5G NR frequency, 2.59 GHz.

Figure 10 illustrates the phase noise measured in the operating bandwidth of the TVCO. The corresponding phase noise at 2.5 GHz, 2.59 GHz, and 2.67 GHz is -122.5 dBc/Hz, -122 dBc/Hz, and -120.97 dBc/Hz, respectively. Figure 11 depicts the PN and power consumption (P_{DC}) of the TVCO across the tuning voltage. The highest achieved PN is -119.5 dBc/Hz with a corresponding P_{DC} of 1.3 mW, while the lowest achieved is -122.5 dBc/Hz with a P_{DC} of 0.17 mW. Hence, a minimum trade-off performance between PN and P_{DC} has been achieved. The corresponding frequency across V_{TUNE} is shown in Fig. 12. The simulated carrier frequency shows 2.53 GHz to 2.69 GHz, and the measured shows 2.5 GHz to 2.67 GHz across 0.1 V to 1.8 V tuning voltage, V_{TUNE}. Figure 13 depicts the thermal analysis from -25 ºC to 125 ºC of the TVCO at 2.59 GHz.

The best-case performance is at -25 ºC, which is -125.1 dBc/Hz, whereas the worst case is at -117.87 dBc/Hz. At the standard temperature of 27 ºC, the phase noise is 122 dBc/Hz. The simulated differential output signal of the TVCO shown in Fig. 14 illustrates the startup time taken when the V_{C1} and V_{C2} values are under the condition of 500 mV. Under this condition, M_1 and M_2 are dynamically tuned at the sweet spot between the current-limited and voltage-limited region, achieving its fastest startup at 1.5 ns.

Figure 15 plots the simulated and measured output voltage waveforms at the drain of M_1 and M_2. It can be observed that the simulated and measured startup time of the TVCO is 1.5 ns and 2.5 ns, with the corresponding output voltage swing of 1.8 V and 1.7 V, respectively. Figure 16 illustrates the measured FoM and PN across V_{TUNE}. At V_{TUNE} of 700 mV, which corresponds to 2.59 GHz, the FoM and PN achieved are 190.36 dBc/Hz and -122 dBc/Hz, respectively. Table I compares the performance parameters of the proposed TVCO with those obtained in previous reports. The proposed TVCO achieves the highest FoM at a low supply voltage of 0.7 V, which is essential for low-power 5th Generation New Radio Application (5G NR).

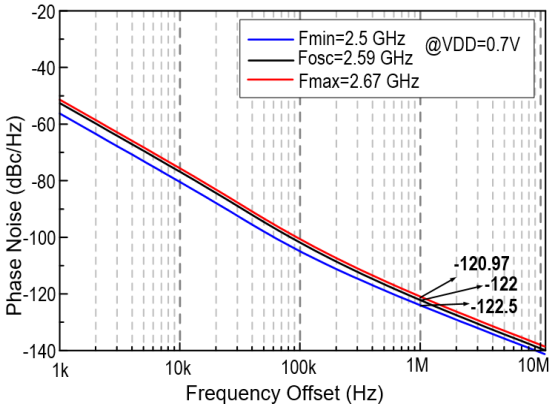

Fig. 10. Measured phase noise at Fmin = 2.5 GHz and Fmax = 2.67 GHz.

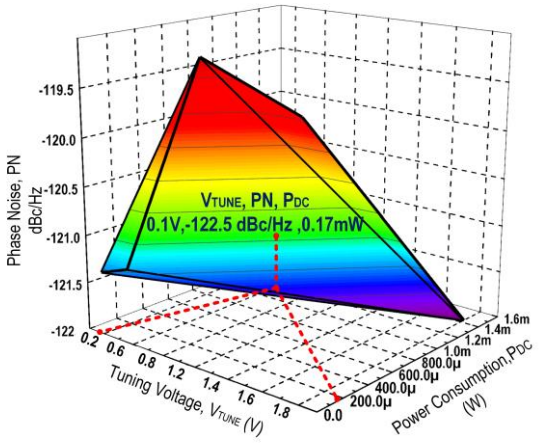

Fig. 11. Phase noise (PN) and power consumption (P_{DC}) in V_{TUNE}.

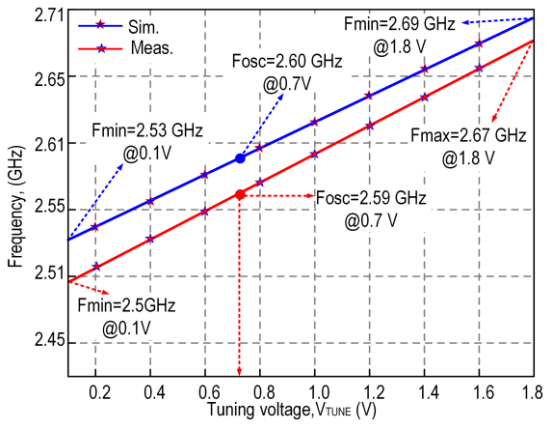

Fig. 12. Simulated and measured frequencies across V_{TUNE} of the TVCO.

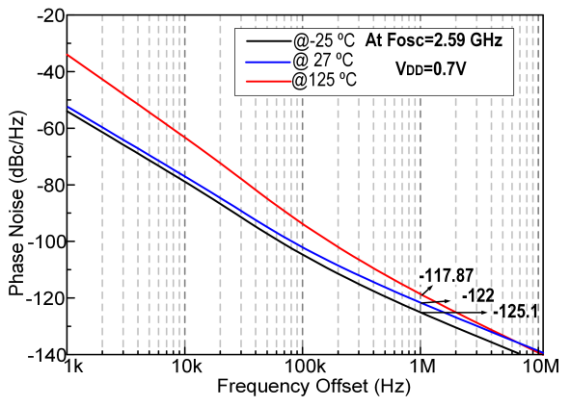

Fig. 13. Phase noise versus temperature at Fosc = 2.59 GHz.

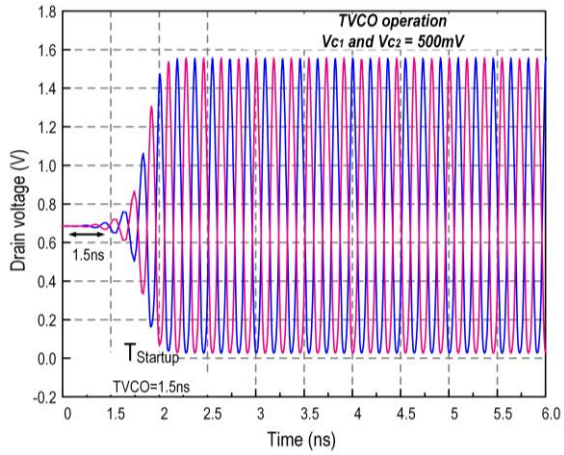

Fig. 14. Simulated TVCO startup time.

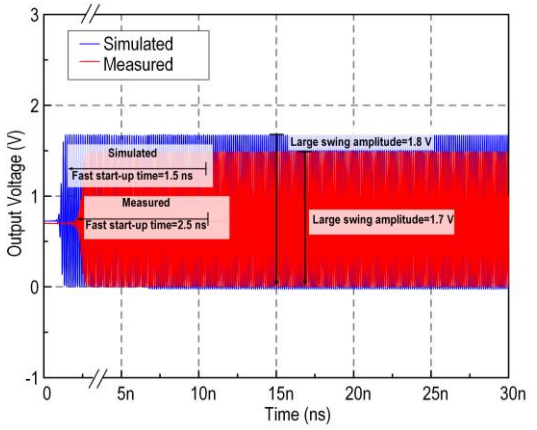

Fig. 15. Startup time for the simulated and measured architecture.

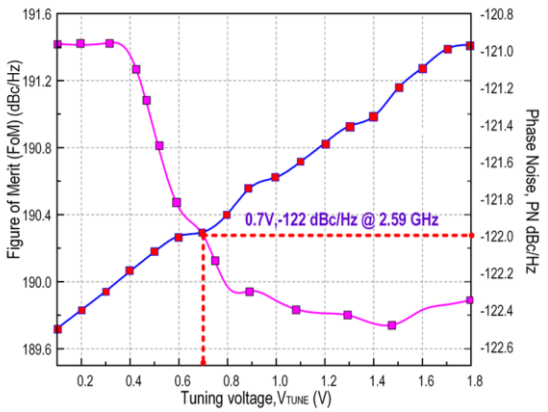

Fig. 16. Figure of merit (FoM) and phase noise (PN) at 1 MHz offset across tuning voltage, V_{TUNE}.

TABLE I. PERFORMANCE COMPARISON WITH OTHER VCOS.

Ref.	Tech. (nm)	V_{dd}, V	f_{OSC}, GHz	TR (GHz)	Phase Noise, dBc/Hz @1MHz	P_{diss}, mW	FoM, dBc/Hz
[9] (S)	45	1	1.8	1.1–1.8	-98.37	1.8	176.69
[10] (S)	180	1.8	4	4	-116.8	1.0	188.9
[11] (S)	180	1.8	1.7	1–2.4	-110	37.8	158.84
[12] (M)	180	1.825	4.55	4.3–4.8	-105.8	0.9	181
[13] (M)	180	1.8	2.4	2.05–2.75	-119.5	18	174.6
[14] (S)	65	1.8	5.89	4.48–5.89	-124.1	15.96	188
[15] (M)	180	1.8	5	4.1–5	-124.7	7.2	190.25
[17] (M)	130	0.5	2.4	2.1–2.8	-115.7	0.25	189.32
[18] (M)	40	0.34	5.19	4.14–6.23	-109.1	0.82	185.0
[19] (S)	180	1.8	4.15	3.8–4.5	-75.6	2.06	145.17
[26] (M)	90	1.2	1.77	1.72–1.83	-112	3.96	171
[27] (M)	65	0.6	5.71	5.07–6.35	-111	0.42	189.9
[28] (M)	65	0.5	5.96	5.94–5.97	-98	0.69	174.11
This work (M)	180	0.7	2.59	2.5–2.67	-122	0.98	190.36

Note: (S) - Simulated, (M) - Measured.

V. CONCLUSIONS

This paper introduces a tailless 2.5 GHz to 2.67 GHz Class-C LC VCO (TVCO) topology. Theoretical and systematic analysis that determines operation and true oscillation frequency that includes intrinsic parasitic capacitance components is shown. The simulation and measured results showed that a reduced trade-off between phase noise and power consumption was achieved with the proposed TVCO. With the exclusion of the conventional tail current source and dual gate biasing mechanism, this architecture performs better than the traditional Class-C VCO obtaining the phase noise at -122 dBc/Hz at 1 MHz offset under a low supply voltage and power consumption of 0.7 V and 0.98 mW, respectively. The measurements obtained with the TVCO showed a superior FoM performance at 190.36 dBc/Hz compared to other LC VCOs from previous reports. Hence, the TVCO suits the 5G NR

technology applications comfortably.

CONFLICTS OF INTEREST

The authors declare that they have no conflicts of interest.

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