Topology Synthesis of the Multi-Tapped Meander Delay Line using Monte Carlo Method

R. Pomarnacki, A. Gurskas, V. Urbanavicius
Department of Electronic Systems, Vilnius Gediminas Technical University,
Naugarduko str. 41-422, LT-03227 Vilnius, Lithuania, phone: +370 5 2744753
raimondas.pomarnacki@el.vgtu.lt

***Abstract*—The algorithm for synthesis of the multi-tapped meander delay line (MTMDL) topology is proposed in this article. The algorithm is based on search of construction parameters of the MTMDL according to Monte Carlo method. Proposed algorithm was realized as software and tested on 14 nodes computer cluster. Experimental synthesis of lines has shown adequacy of the suggested algorithm. It has been shown that increasing number of nodes in the cluster, synthesis is executing faster and parallel part of the algorithm approaches to 90 percent of total algorithm. It is revealed that the maximal efficiency of the algorithm is achieved when the number of cluster nodes reaches the number of all issued synthesis processes.**

***Index Terms*— Circuit topology, delay lines, integrated circuit synthesis, microwave devices, parallel algorithms.**

I. INTRODUCTION

Delay lines are widely used for analog signal processing [1], analog-to-digital converters [2], signals synchronization [3], and many other devices [4], [5].

Principle of operation and a design of delay lines are very differ. For example active delay lines: lines which use delay of signals in digital logic elements [2], the active lines using reactive properties of networks elements (e.g. varactors) [6], ultrasonic delay lines [7]. Passive delay lines are also used broadly: delay lines created using lumped elements [8], optical delay lines [4], etc. Among all variety of delay lines the meander microstrip lines are diverged due to their small sizes and weight, and good design fitness for the modern manufacturing [1], [3], [9].

Design of the typical meander microstrip multi-tapped delay line (MTMDL) is presented on Fig. 1. It consists of dielectric substrate with one side covered by a solid conductive layer and the signal conductor of the meander form, having intermediate contact pins for tap of a signal with the specified fixed step of a delay, on the other side.

To achieve asked electrical characteristics of the MTMDL with the minimal deviations is possible only at careful designing the MTMDL and precision synthesis of its topology. Synthesis of the MTMDL topology is a procedure of finding of its constructive dimensions and parameters according to the asked electric characteristics of this MTMDL. Synthesis problems are of particular interest for creating CAD systems for microwave devices in general, and many researches were intensively solving the problems in the past decade [7], [8], [10], [11]. E.g. Wilson and Atkinson [6] for SAW delay lines designing use a method of the pulse characteristic which is realized in MathCAD® system, and concurrence of the simulated and measured characteristics of the delay lines have achieved within the limits of 20 %.

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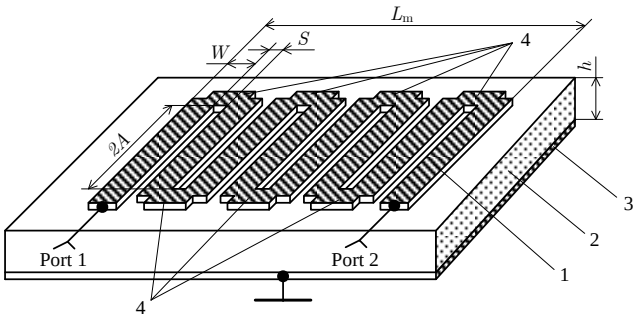

Fig. 1. The design of the meander multi-tap microstrip delay line: 1 – strips of the meander conductor; 2 – dielectric substrate; 3 – conductive shield; 4 – intermediate taps.

The example of use of a method of equivalent circuits for delay line design is presented in [8]. Jurjevas and Martavicius for modeling meander delay lines with additional inter-digital shields had used a method of multiconductor lines. The error of synthesis here can be less than 10 %. The similar technique of synthesis of meander microstrip delay lines and multilayer helical delay lines in article [10] is submitted. For optimization of synthesis process, the influence functions of design parameters on electric characteristics of the delay line here are found. For reduction of distortions of a delayed signal it is offered in paper [11] to use genetic algorithm optimizing a technique of topology of the meander microstrip lines and helical delay lines.

A survey of literature reveals that there is no well-established systematic design technique for synthesis of the MTMDL. In the absence of such a technique, delay lines are typically designed using extensive software simulations where high-frequency simulators (mostly commercial) are used for choosing the required design parameters for a good coverage.

In this paper we propose an original parallel synthesis technique of the MTMDL. This algorithm demonstrates rather fast computational efficiency and good accuracy.

II. PARALLEL SYNTHESIS ALGORITHM OF THE MTMDL USING MONTE CARLO METHOD

Generally the algorithm of topology synthesis of the MTMDL is executed sequentially. Mathematical background of such algorithm is analysis of the MTMDL based on quasi-TEM model of a multiconductor microstrip line which is presented in [12].

The Monte Carlo method has been chosen to make it possible to use parallel calculation during analysis processes instead of sequential approach. This method allows us generating arrays of values of primary selected topology parameters to obtain an array of calculated electrical characteristics of the MTMDL executing parallel processing.

To reduce synthesis time construction parameters of the MTMDL has been distributed among computers (nodes) of the parallel system. In this case, every node will have different initial parameters of the MTMDL for which searched electrical characteristics should be calculated.

Main characteristics of the MTMDL are follows: bandwidth DF, number of meander steps N, delay time at low frequencies t_d and characteristic impedance at low frequencies Z_0.

Characteristic impedances at quasi-TEM approach could be found knowing capacitances per unit length of the conductors of the multiconductor microstrip line that is used as a model of the MTMDL

$$Z_0 = 1 \Big/ \left(c_0 \sqrt{CC^{(a)}} \right), \tag{1}$$

where c_0 is the velocity of light in free space; C is the capacitance per unit length of a conductor of the MTMDL; $C^{(a)}$ is the capacitance per unit length of the same conductor when the substrate in the line is replaced by air ($\varepsilon_r = 1$). Delay time t_d is calculated knowing meander altitude $2A$ and number of steps of the meander N.

The software algorithm of the MTMDL synthesis is presented in Fig. 2. This algorithm uses "master-slave" parallel programming paradigm. The algorithm consists of 15 steps:

1. Asked electrical characteristics, their tolerances, ranges of construction parameters and common parameters of the MTMDL are entered: the relative permittivity ε_r and the height h of the dielectric substrate; range of width of microstrip conductors W_{min}, W_{max} and the range of spaces between them S_{min}, S_{max}; range of the meander altitude $2A_{min}$, $2A_{max}$; common parameters like a size of the analysis area x and y, which are needed for quasi-TEM analysis of the MTMDL; asked characteristic impedance Z_0 and its tolerance δ_Z; nominal delay time t_d at low frequencies and its calculation tolerance δ_t; step of delay time Δt_d; nominal bandwidth ΔF and its tolerance $\delta_{\Delta F}$.
2. Microstrip width $W^{(P)}$ values are randomly generated with equal probability over initial selected range $W_{max} - W_{min}$. The number of generated values is equal to the number of processes P, which is defined at the algorithm start-up.
3. Values of characteristic impedances $Z^{(P)}$ are calculated in parallel in all nodes according to microstrip width $W^{(P)}$ values generated at step 2.
4. If one of the calculated values of the characteristic impedance meets the condition

$$\min\left(\left| Z^{(P)} - Z_0 \right| / Z_0 \right) <= \delta_Z , \tag{2}$$

algorithm goes to the step 6, if not – algorithm goes to the step 5.

5. A combination of the nearest value of characteristic impedance $Z^{(P)}$ to its asked value Z_0, found at step 4, is fixed. This fixed microstrip width $W^{(P)}$ is a starting point to the next series of parallel calculations. The only difference from initial series is that normal (Gauss) distribution is used for the new $W^{(P)}$ set. Going to step 3 where new characteristic impedance values $Z^{(P)}$ will be calculated.

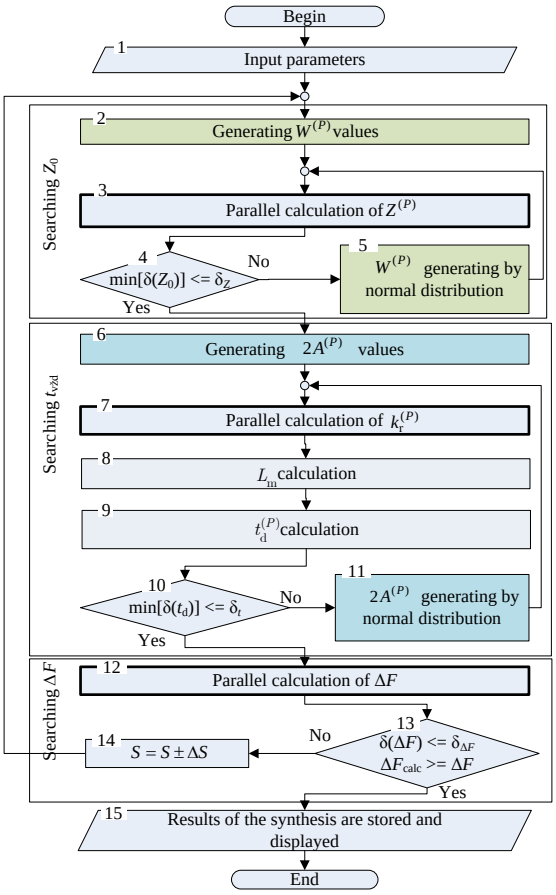

Fig. 2. Flowchart of the parallel synthesis algorithm of the multi-tapped microstrip delay line.

6. Meander altitude $2A^{(P)}$ values are randomly generated over all given range with equal probability.
7. Values of retard factor $k_r^{(P)}$ are calculated using obtained values of meander altitude $2A^{(P)}$.
8. Length of the MTMDL is calculated according to the following equation

$$L_m = N \cdot (W + S) - S . \tag{3}$$

9. A delay time of the MTMDL is calculated according to the following equation

TABLE I. RESULTS OF INVESTIGATION OF THE MTMDL SYNTHESIS ALGORITHM.

No. of experiment	Asked electrical characteristics				Calculated electrical characteristics			Topology of the MTMDL[1]			
	Z_0, Ω	t_d, ns	ΔF, GHz	Δt_d, ns[2]	Z_{0calc}, Ω	$t_{d\,calc}$, ns	ΔF_{calc}, GHz	W, mm	S, mm	$2A$, mm	L_m, mm
3	120	3	1	0.06	119.95	3.01	1.01	0.11	0.80	8.41	44.7
8	50	5	1	0.10	49.09	4.92	1.01	0.73	2.20	10.71	144.3
14	50	1.5	3	0.03	48.60	1.47	2.95	0.73	1.60	3.36	114.9

[1] MTMDL microstrip width W variations range is from 0.1 mm to 1.3 mm, step ΔW = 0.1 mm; space between microstrips S variation range is from 0.1 mm to 2 mm, step ΔS = 0.1 mm; meander altitude $2A$ variation range is from 1 mm to 60 mm, step $\Delta 2A$ = 1 mm. Dielectric substrate permittivity $\varepsilon_r = 9.85$ and substrate altitude $h = 0.5$ mm.

[2] Delay time of one step of the MTMDL, which is used for calculate the number of steps of the MTMDL $N = 50 = \text{const}$.

$$t_d^{(P)} = \left(L_m \cdot k_r\right)/c_0 . \quad (4)$$

10. If one of the calculated values of the delay time meets condition

$$\min\left(\left|t_d^{(P)} - t_d\right|/t_d\right) <= \delta_t , \quad (5)$$

then calculations continues at the step 12, if not – algorithm goes to the step 11.

11. A combination of delay time $t_d^{(P)}$ and corresponding altitude $2A^{(P)}$ is fixing, where $t_d^{(P)}$ is the closest value to the asked t_d. Fixed altitude $2A^{(P)}$ is a starting point to the next series of parallel calculations. At this point normal (Gauss) distribution is used for new $2A^{(P)}$ set. Going to step 7 where new retard factor values will be calculated.
12. Parallel calculation of the bandwidth ΔF_{calc}.
13. If one of two conditions are satisfied:

$$\min\left(\left|\Delta F_{calc} - \Delta F\right|/\Delta F\right) <= \delta_{\Delta F} , \quad (6)$$

$$\Delta F_{calc} >= \Delta F, \quad (7)$$

then algorithm continues at the step 15, if not – at the step 14.

14. Space between microstrips is increased and algorithm goes to the beginning of the algorithm to the step 2.
15. The calculated and asked electrical characteristics and synthesized construction parameters of the MTMDL are shown and stored.

III. EXPERIMENTAL SYNTHESIS OF THE MTMDL TOPOLOGY

The proposed algorithm for synthesis of the topology of the MTMDL, was investigated in the following order. Initially, adequacy of functioning of algorithm was checked. Next, the error of results of synthesis of the MTMDL was tested.

Electrical characteristics of the experimentally synthesized MTMDL topology were varied during computer experiment. Experimental MTMDL synthesis results are presented in Table I. It is seen in Table I that the largest error of electrical characteristics of synthesized MTMDL not exceed 3 %.

The error of synthesis of topology of the MTMDL was estimated by comparison of frequency dependence of time delay of the synthesized MTMDL with dependences obtained by a hybrid method of the MTMDL analysis and using Sonnet® software (Fig. 3). In both cases the mistake did not exceed 10 %.

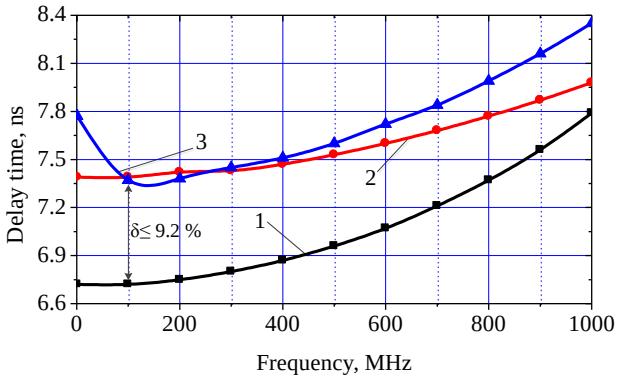

Fig 3. Time delay frequency responses, where 1 is a response, obtained using proposed technique; 2 is a response; 3 is a response, obtained using Sonnet® simulator.

IV. PERFORMANCE OF THE PARALLEL SYNTHESIS ALGORITHM

In order to investigate the performance of the proposed parallel MTMDL synthesis algorithm the experiment was equipped with 14 nodes (CPU – Pentium™ 4, 2.8 GHz; RAM – 512 MB; OS – Fedora 6; the network – Ethernet 1 Gb/s) cluster.

To ensure the continuity of the volume of calculations at different cluster nodes, for all experiments was chosen the same number of processes corresponding to the maximum number of nodes p = 14.

Results of the investigation of algorithm performance are presented in Fig. 4.

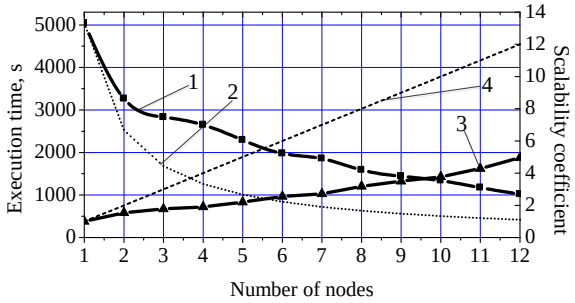

Fig 4. Synthesis algorithm execution time response to the cluster nodes number and scalability: 1 is an execution time of the algorithm, 2 is an ideal execution time, 3 is a scalability coefficient of the algorithm, and 4 is an ideal scalability coefficient.

It should be noted that, MTMDL synthesis execution time using the Monte Carlo method algorithm are random in nature, therefore it sometimes is executed faster and sometimes more slowly under all other equal conditions. Therefore execution of the MTMDL synthesis algorithm was repeated 10 times for each implemented number of nodes in the cluster.

Curves 1 and 2 on Fig. 4 show, that increasing the number of nodes in the cluster, algorithm execution time decreasing in inverse ratio. It is a common feature of all the parallel algorithms. It should be noted, when the number of nodes becomes large enough (in our case the largest number of nodes was 14), the probability to find the optimal design parameter values, with a small number of iterations become very high.

Dependency of the scalability of algorithm from the number of the nodes is also shown in Fig. 4 (curves 3 and 4). It is seen here that when the number of cluster nodes is equal to 12 then scalability coefficient is equal to 4.96. This coefficient allows us to calculate size of a part of operations of algorithm which can be executed in parallel [13]. In our case it reaches 87 % that is very high value.

V. CONCLUSIONS

1. Parallel algorithm of topology synthesis of the multi-tapped meander delay lines (MTMDL), based on Monte Carlo technique for distributed computation, and quasi-TEM model of the microstrip multiconductor line, is proposed in the article.
2. Verification of the proposed algorithm has been done by comparing calculated delay time dependence on the frequency with the same calculations performed with Sonnet® simulator, and other different numerical techniques. Difference was within 10 %.
3. Investigation have shown, that increasing the number of nodes in PC cluster for the proposed MTMDL topology synthesis algorithm, the execution time decreasing by hyperbolic law.
4. It was found that the most efficiency of the MTMDL synthesis algorithm is reached when the number of cluster nodes is closer to the number of processes.

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