Comparative Analysis of High Power Density Bidirectional DC-DC Converters for Portable Energy Storage Applications

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***Abstract*—Bidirectional DC-DC converters are an essential part of modern power systems, such as electric vehicles and renewable energy. The paper presents a comparative analysis of bidirectional DC-DC converters suitable for high power density application without galvanic isolation. It is based on the comprehensive comparative analysis of conduction losses, voltage stress on semiconductors and passive component size. Continuous conduction mode of three widely used bidirectional topologies (cascaded, two-phase interleaved with and without charge-pump) are analysed. Selected analytically calculated evaluation criteria are compared for a wide range of the output voltage level. The best solution is selected for experimental realization based on GaN transistors.**

***Index Terms*—Bidirectional power flow; Circuit analysis; DC-DC power converters; Pulse width modulation converters.**

I. INTRODUCTION

Recent years have seen a drastic increase in the use of Renewable Energy Sources (RESs) and all types of Electric Vehicles (EVs). A power capacity recorded last year was: solar PV capacity increased by 22 %, constituting 227 GW; wind power capacity increased by 14.5 %, amounting to 433 GW [1]. Also, as compared to 2014, in 2015, electric car stock almost doubled, reaching 1.26 million [2]–[4]. Alternative power sources (compact wind turbines or thin-film solar panels) have become a development trend for portable applications [5]–[11]. Flexible PV blanket mounted on any surface [12], [13] will be quite useful in many applications for charging portable electronic devices.

In general, the technologies described require bidirectional power interface with minimum losses between two DC-busses or a DC-bus and an energy storage device (battery, supercapacitor, etc.). For these purposes, Bidirectional DC-DC Converters (BDCs) should be used. In applications with lower step-up or step-down ratio, a common solution is a non-isolated type [14]–[16]. As compared to isolated converters, it provides high efficiency, high power density, and smaller size and lower cost.

Figure 1 compares non-isolated topologies: interleaved topologies (Fig. 1(a) and Fig. 1(b)) and a cascaded topology (Fig. 1(c)). In those topologies, hard switching control limits their efficiency. Commonly, to overcome that problem and exploit the benefits of Zero-Voltage-Switching (ZVS) or Zero-Current-Switching (ZCS), auxiliary circuitry is used. Resonant switching increases efficiency by reducing switching losses; however, it increases the size, cost, complexity and makes tuning more difficult. Other options are special modulation techniques or increasing the frequency and using the parasitic element of the device as resonant elements (e.g. FETs output capacitance C_{oss}). Still, switching limitation of traditionally used Si MOSFETs lies in the range of couple hundreds of kilohertz, which usually is insufficient.

A solution to this problem can be the use of transistor hetero structures as AlGaN/GaN-based advanced materials. Unique properties of these semiconductors (wide band gap, high values of the charge carrier mobility and saturation velocity, high coefficient of thermal conductivity, etc.) have led to the emergence of devices that have record values of power, voltage and current, as well as the operating frequency (1 MHz–2 MHz) [17]–[20]. High switching frequency allows using extremely small passive elements. At the same time, according to [18], losses in the passive elements are becoming more critical and are limiting the switching frequency.

References [21], [22] illustrate the relations of the switching loss and show some important power losses characteristics. Figure 22 in [21] and Fig. 17 in [22] clearly show that the main contribution in total losses of transistors (especially during ZVS/ZCS switching) are made by conduction losses. Thus, topologies with minimum conduction losses are preferable for further investigations.

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This paper provides a comparative analysis of the proposed bidirectional topologies with criteria related to passive volume, voltage stress on semiconductors and conduction losses, to choose a better structure for low-medium power portable applications.

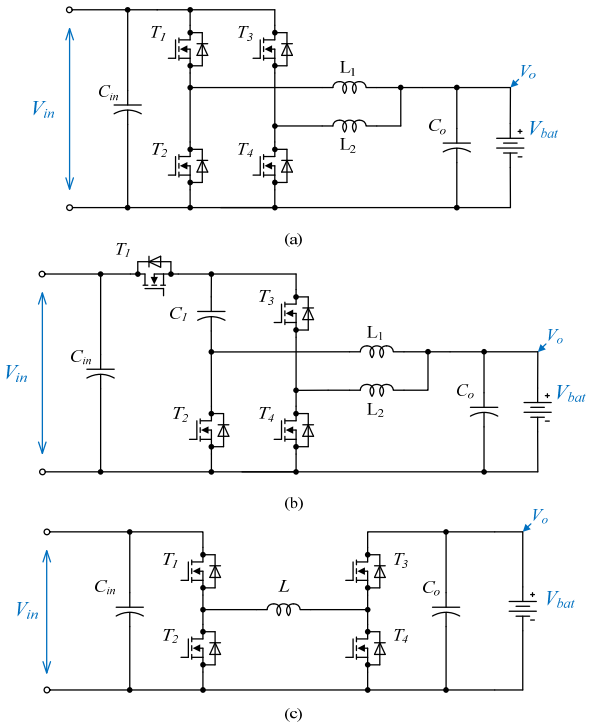


Fig. 1. Proposed topologies for the comparative analysis: a) two-phase interleaved; b) two-phase interleaved charge-pump; c) cascaded.

II. Criteria for Comparative Analysis of Converter Topologies

This section describes the criteria used for the comparative analysis of the presented topologies.

Evaluation criteria are chosen based on the consideration that the topology should have minimum conduction losses, minimum voltage stress on the semiconductor devices and minimum size of passive components [23]–[30]. The main estimated values here should be represented in relative units (p.u.) to neglect the effect of input/output parameters for final comparison. Also, the analysis is made for one power flow direction (buck operating mode) only at constant output power.

To estimate the contribution of power switches, the value of total voltage stress is taken into consideration as one of the criteria

$$T_W = \sum_{i=1}^{N_T} V_{Ti}, \tag{1}$$

where N_T is the number of transistors. The amount of power diodes blocking voltage D_W is not taken into account because all the presented topologies use synchronous rectifications (diodes connected in parallel with switches), as a result, $T_W \cong D_W$.

Conduction losses in semiconductors are expressed as

$$P_{CL} = \sum_{i=1}^{N_T} I_{RMSi}^2 \times R_{DSoni}, \tag{2}$$

where I_{RMSi} is RMS current through the transistor, R_{DSoni} – drain-source on resistance.

Conduction losses include the sum of power transistors and diodes conduction losses: $P_{CL} = P_{TC} + P_{DC}$. But due to synchronous rectification, diodes will be conducted only during the dead time between the control signals. This amount of losses can be neglected without a serious impact on the final calculation results. Thus, $P_{CL} \cong P_{TC}$.

Based on our hypothesis, the relative size of inductors and capacitors is proportional to the stored energy, so maximum energy stored in the inductors is

$$Vol_L \cong E_{LW} = \sum_{i=1}^{N_L} \frac{L_i I_{AVi}^2}{2}, \tag{3}$$

where N_L is the number of inductances in the topology, I_{AV} – average current through the inductor.

Maximum energy stored in the output capacitor

$$Vol_C \cong E_{CW} = \frac{CV_{AV}^2}{2}, \tag{4}$$

where V_{AV} – average voltage on the capacitor.

III. Analysis of the Bidirectional Converters

A. Two-Phase Interleaved Bidirectional DC-DC Converter

The concept of the half-bridge interleaved bidirectional DC-DC converter is proposed and described in [22], [31]–[39]. Figure 2 shows the basic operational modes of an interleaved two-phase converter during the buck state.

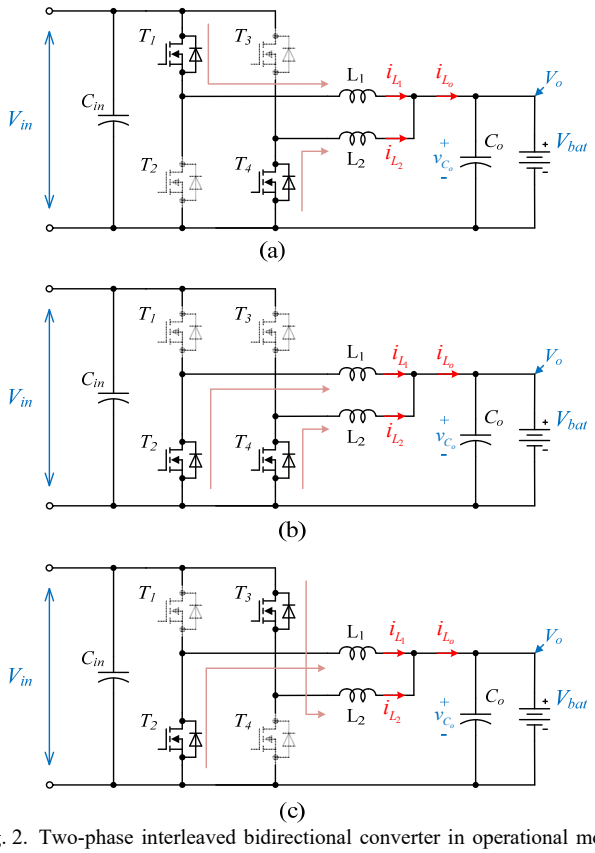


Fig. 2. Two-phase interleaved bidirectional converter in operational mode 1 (a); in mode 2,4 (b); in mode 3 (c).

Linear-ripple approximated waveforms of inductor

currents and output capacitor voltage are shown in Fig. 3. Assuming that the scheme works in the continuous conduction mode (CCM), the dependence between the input DC voltage V_{IN} and the output voltage V_O will be

$$V_O = D \times V_{IN}, \tag{5}$$

where D is duty cycle.

By means of power balance and assuming an ideal converter (energy conversion efficiency $\eta = 100\%$), an average output current can be represented as:

$$P_{IN} \approx P_O = V_O \times I_O, \tag{6}$$

$$I_O = \frac{P_O}{V_O}, \tag{7}$$

where P_{IN} and P_{OUT} are input and output power respectively.

Assuming that the topology phases are equally loaded, the output dc current in each inductor will be

$$I_{L_1} = I_{L_2} = \frac{P_O}{2 \times I_O}. \tag{8}$$

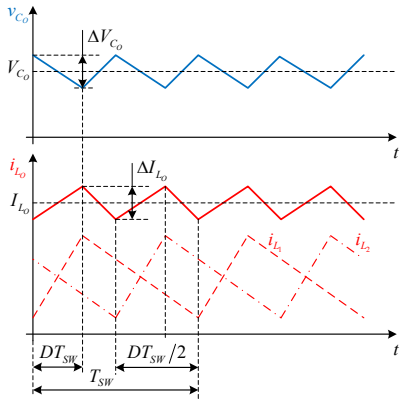


Fig. 3. Capacitor voltage and inductor current waveforms of two-phase interleaved topology.

Inductor current ripple is represented as

$$\Delta I_{L_1} = \int_0^{DT_{SW}} \frac{di_{L_1}}{dt} dt = \frac{(V_{IN} - V_O)}{L_1} \times D \times T_{SW}. \tag{9}$$

Inductance L_1 can be represented by well-known formulas [39], but in our case, it is better to express it through the current ripple factor

$$K_{L_1} = \frac{\Delta I_{L_1}}{I_{L_1}} = \frac{2 \times V_O \times (V_{IN} - V_O)}{L_1 \times P_O} D \times T_{SW}. \tag{10}$$

Thus, inductance is expressed as

$$L_1 = L_2 \geq \frac{2 \times V_O^2 \times (V_{IN} - V_O)}{V_{IN} \times K_{L_1} \times P_O} T_{SW}. \tag{11}$$

A reference condition for calculating relative units for all topologies will be $V_O = V_{IN}/8$. This value is chosen to avoid border conditions and due to schematic limitations of the second topology where the duty cycle D can be only in the range 0...0.5 and the output voltage cannot be higher than $V_{IN}/4$ [40], [41].

Assume that the condition $V_O = V_{IN}/8$ corresponds to one relative unit of the inductance, thus

$$L = \frac{7 \times V_{IN}^2 \times T_{SW}}{256 \times K_{L_1} \times P_O} = 1\, p.u. \tag{12}$$

Inductance is expressed as

$$L_1 = L_2 = L \times \frac{512 \times V_O^2 \times (V_{IN} - V_O)}{7 \times V_{IN}^3}. \tag{13}$$

Average voltage on the output capacitor equals V_O

$$V_{C_O} = V_O. \tag{14}$$

Due to a ripple cancellation effect on the interleaved converters, the ripple voltage behavior of the capacitor differs slightly from the conventional buck converter. Rearranging the equations for the capacitor volt-second balance and the capacitor electrical charge [31], C_O voltage ripple is evaluated as (Fig. 3)

$$\Delta V_{C_O} = \frac{1}{C_O} \int_0^{DT_{SW}} i_{C_O}(t) dt = \\ = \frac{P_O \times (1 - 2 \times D) \times D}{V_O \times C_O} \times D \times T_{SW}. \tag{15}$$

Output capacitor voltage ripple factor is expressed as

$$K_{C_O} = \frac{\Delta V_{C_O}}{V_{C_O}} = \frac{P_O \times (1 - 2 \times D) \times D}{V_O^2 \times C_O} \times D \times T_{SW}. \tag{16}$$

It should be noted that in (15) the coefficient that affects ripple cancellation $(1 - 2 \cdot D) \cdot D$ is correct only for $D \leq 0.5$. For the value $D > 0.5$, this coefficient should be $(1 - 2 \cdot D') \cdot D'$, where $D' = 1 - D$. Thus, the output capacitance value is

$$C_O = \begin{cases} \dfrac{P_O \times (1 - 2 \times D) \times D}{V_O^2 \times K_{C_O}} D \times T_{SW}, & for\ D \leq 0.5, \\ \dfrac{P_O \times (1 - 2 \times D') \times D'}{V_O^2 \times K_{C_O}} D \times T_{SW}, & for\ D > 0.5. \end{cases} \tag{17}$$

For the condition $V_O = V_{IN}/8$, one capacitance relative unit is

$$C = \frac{3 \times P_O \times T_{sw}}{4 \times V_{IN}^2 \times K_{C_O}} = 1\, p.u. \tag{18}$$

Output capacitance is expressed as

$$C_O = \begin{cases} C \times \frac{4}{3} \times \left(1 - 2 \times \frac{V_O}{V_{IN}}\right), \text{ for } D \le 0.5, \\ C \times \frac{4}{3} \times \frac{\left(2 \times V_O - V_{IN}\right) \times \left(1 - \frac{V_O}{V_{IN}}\right)}{V_O}, \text{ for } D > 0.5. \end{cases} \quad (19)$$

Based on Fig. 2, maximum voltage stress on each power switch is

$$V_{T1..T4} = V_{IN}. \quad (20)$$

B. Two-Phase Interleaved Bidirectional DC-DC Charge-Pump Converter

Since for the previous topology, general calculation principles are used, for the second topology, equations will be expressed in a similar manner.

Due to the phase switches T_1 and T_3 connected in series, it can be clearly seen from Fig. 4 that in the buck mode, the duty cycle of the control signals cannot be equal or greater than 0.5 [40]–[46]. Dependence between the input DC voltage V_{IN} and the output voltage V_O will be

$$V_O = \frac{D \times V_{IN}}{2}. \quad (21)$$

As in the previous topology (7), assume that current sharing is ideal, so the inductor DC-current is

$$I_{L_1} = I_{L_2} = \frac{P_O}{2 \times V_O}. \quad (22)$$

For further calculations, the value of the voltage on the charge-pump capacitor C_1 is needed. It can be expressed from the equation system for inductor volt-second balance [42], [46]:

$$\begin{cases} D \times (V_{IN} - V_O - v_{C_1}) + (1 - D) \times (-V_O) = 0, \\ D \times (v_{C_1} - V_O) + (1 - D) \times (-V_O) = 0. \end{cases} \quad (23)$$

The obtained capacitor voltage is $v_{C_1} = V_{IN}/2$. Assuming that the capacitor C_1 is large enough, the voltage v_{C_1} is considered the same during the whole switching period.

Inductor current ripple is

$$\Delta I_{L_1} = \frac{(V_{IN} - V_O - v_{C_1})}{L_1} \times D \times T_{SW} = \frac{(\frac{V_{IN}}{2} - V_O)}{L_1} \times D \times T_{SW}. \quad (24)$$

Current ripple factor for one phase is

$$K_{L_1} = \frac{\Delta I_{L_1}}{I_{L_1}} = \frac{4 \times V_O^2 \times (\frac{V_{IN}}{2} - V_O)}{V_{IN} \times L_1 \times P_O} T_{SW}. \quad (25)$$

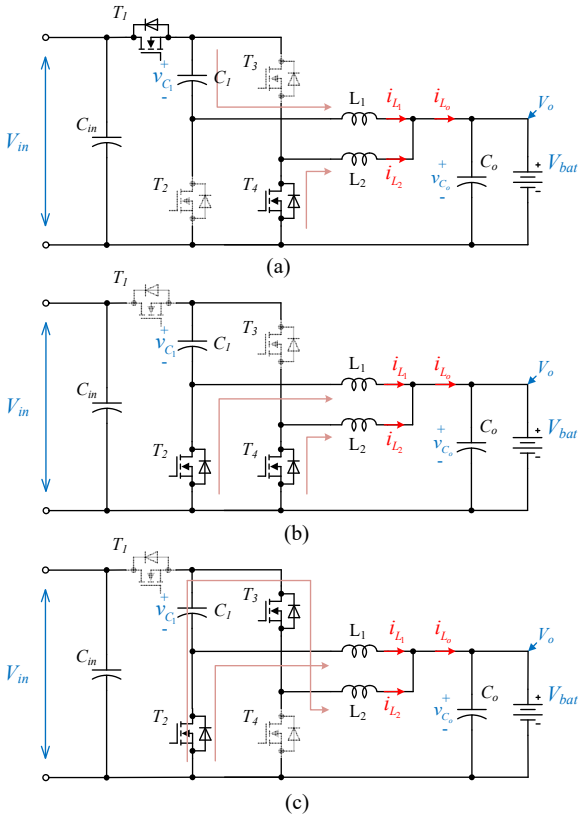


Fig. 4. Two-phase interleaved bidirectional charge-pump converter in operation mode 1 (a); in mode 2,4 (b); in mode (3).

Thus, phase inductance can be expressed as

$$L_1 = L_2 \ge \frac{4 \times V_O^2 \times (\frac{V_{IN}}{2} - V_O)}{V_{IN} \times K_{L_1} \times P_O} T_{SW}. \quad (26)$$

For the condition $V_O = V_{IN}/8$, one inductance relative unit is

$$L = \frac{3 \times V_{IN}^2 \times T_{SW}}{128 \times K_{L_1} \times P_O} = 1\, p.u. \quad (27)$$

The equation for inductance expressed in relative units is

$$L_1 = L_2 = L \times \frac{512 \times V_O^2 \times \left(\frac{V_{IN}}{2} - V_O\right)}{3 \times V_{IN}^3}. \quad (28)$$

Based on equations from [40]-[42], the output capacitor voltage ripple is

$$\Delta V_{C_O} = \frac{1}{C_O} \int_0^{DT_{SW}} i_{C_O}(t) dt = \frac{P_O \times (0.5 - D) \times D}{V_O \times C_O} \times D \times T_{SW}. \quad (29)$$

Taking into account that an average output capacitor voltage should be constant, the voltage ripple factor is

$$K_{C_O} = \frac{\Delta V_{C_O}}{V_{C_O}} = \frac{P_O \times (0.5 - D) \times D}{V_O^2 \times C_O} \times D \times T_{SW}. \quad (30)$$

The equation for the output capacitor is expressed as

$$C_O = \frac{P_O \times (0.5 - D) \times D}{V_O^2 \times K_{C_O}} \times D \times T_{SW}. \quad (31)$$

Based on the condition $V_O = V_{IN}/8$, one relative unit of the capacitance is

$$C = \frac{P_O \times T_{SW}}{V_{IN}^2 \times K_{C_O}} = 1\,p.u. \quad (32)$$

Thus, the equation for the output capacitance is

$$C_O = C \times (2 - 2 \times D) = C \times \left(2 - \frac{8 \times V_O}{V_{IN}}\right). \quad (33)$$

From Fig. 4, the total voltage stress on the semiconductors is:

$$\begin{cases} V_{T1} = V_{T2} = V_{T4} = \dfrac{V_{IN}}{2}, \\ V_{T3} = V_{IN}. \end{cases} \quad (34)$$

C. Cascaded Bidirectional DC-DC Converter

The most universal solution for a bidirectional power flow interface is a cascaded converter [47]–[59]. This topology can provide either step-up or step-down conversion in both directions.

Control strategies for the cascaded converter can vary. There are some modulation techniques that allow achieving ZVS and thus obtain better efficiency [47]–[49]. To simplify the calculations, a simple buck mode will be used: switch T_1 acts as the main power switch, T_2 operates as the main diode, T_3 is always open [55], [57]–[59]. Figure 5 shows basic operation modes of the cascaded converter.

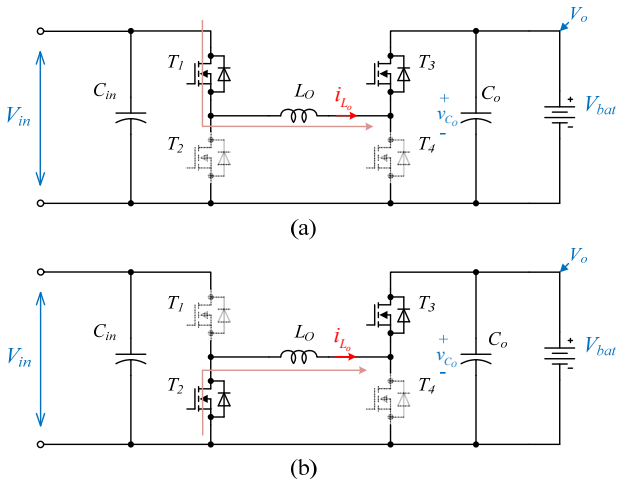


Fig. 5. Cascaded bidirectional converter in operation mode 1 (a) and 2 (b).

The relation between the input and the output voltage in CCM is the same as for a conventional buck converter

$$V_O = D \times V_{IN}. \quad (35)$$

Average current in the inductor is

$$I_{L_O} = \frac{P_O}{I_O}. \quad (36)$$

Inductor current ripple is represented as

$$\Delta I_{L_O} = \int_0^{DT_{SW}} \frac{di_{L_O}}{dt} dt = \frac{(V_{IN} - V_O)}{L_O} D \times T_{SW}. \quad (37)$$

As for the previous two topologies, inductance is calculated through relative units:

$$K_{L_O} = \frac{\Delta I_{L_O}}{I_{L_O}} = \frac{V_O^2 \times (V_{IN} - V_O)}{L_O \times P_O \times V_{IN}} T_{SW}, \quad (38)$$

$$L_O \geq \frac{V_O^2 \times (V_{IN} - V_O)}{V_{IN} \times K_{L_O} \times P_O} T_{SW}, \quad (39)$$

$$L = \frac{7 \times V_{IN}^2 \times T_{SW}}{512 \times K_{L_O} \times P_O} = 1\,p.u., \quad (40)$$

$$L_O = L \times \frac{512 \times V_O^2 \times (V_{IN} - V_O)}{7 \times V_{IN}^3}. \quad (41)$$

Assuming that the output capacitor voltage ripple changes linearly, the output capacitor in relative units is represented as:

$$\Delta V_{C_O} = \frac{1}{C_O} \int_0^{DT_{SW}} i_{C_O}(t) dt = \\ = \frac{P_O \times (1 - D) \times D}{V_O \times C_O} \times D \times T_{SW}, \quad (42)$$

$$K_{C_O} = \frac{\Delta V_{C_O}}{V_{C_O}} = \frac{P_O \times (1 - D) \times D}{V_O^2 \times C_O} \times D \times T_{SW}, \quad (43)$$

$$C_O = \frac{P_O \times (1 - D) \times D}{V_O^2 \times K_{C_O}} \times D \times T_{SW}, \quad (44)$$

$$C = \frac{7 \times P_O \times T_{SW}}{8 \times V_{IN}^2 \times K_{C_O}} = 1\,p.u., \quad (45)$$

$$C_O = C \times \frac{8}{7} \times (1 - D) = C \times \frac{8}{7} \times \left(1 - \frac{V_O}{V_{IN}}\right). \quad (46)$$

Maximum transistor voltages are:

$$\begin{cases} V_{T1} = V_{T2} = V_{IN}, \\ V_{T3} = 0, \\ V_{T4} = V_O. \end{cases} \quad (47)$$

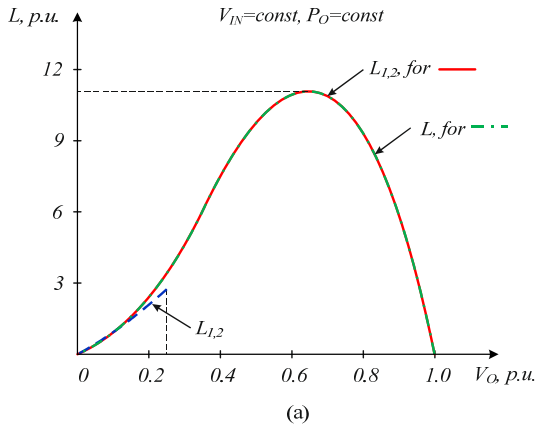
IV. Summarized Comparative Analysis of the Selected Topologies

To sum up the calculation results from Section III, the criteria are used for comparison in all topologies mentioned above. Figure 6 shows the curves for passive elements estimated in relative units, as a function of output voltage. Final formulas are received for the CCM operation mode based on (1)–(4) and placed in Table I. Radar diagrams

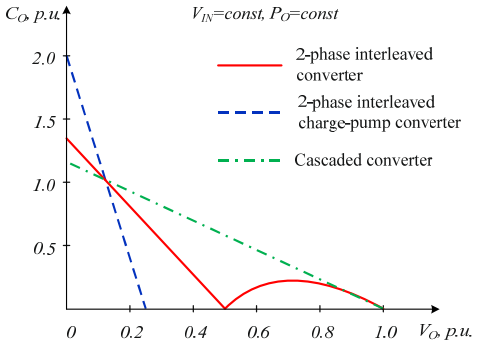
depicted in Fig. 7 are built at constant output power by using such formulas for three different cases: $V_O = 0.1 \cdot V_{IN}$, $V_O = 0.2 \cdot V_{IN}$, and $V_O = 0.4 \cdot V_{IN}$.

It should be noted that the length of different spokes (T_W, P_{CL}, E_{LW}, and E_{CW}) reflects normalized calculated data.

No diagram for an interleaved charge-pump converter is shown in Fig. 7(c) because of the limitations described above.



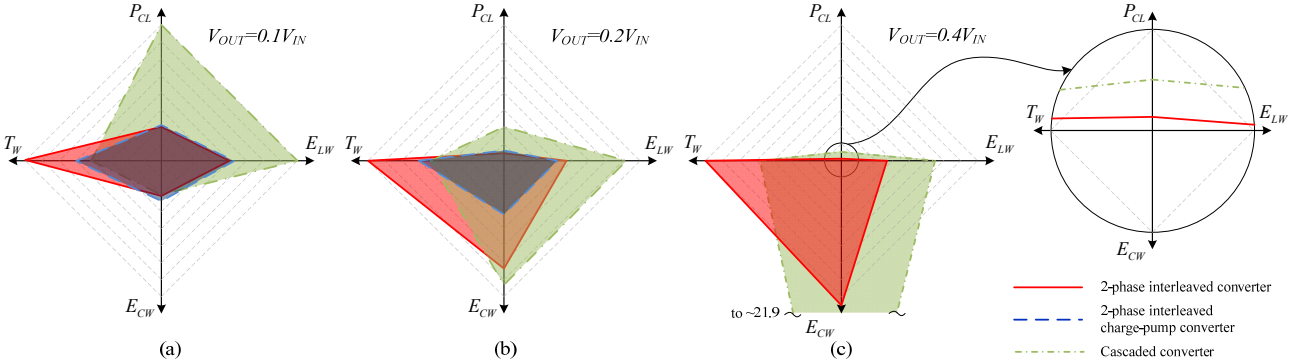
(a)



(b)

Fig. 6. Comparison of passive elements: inductance (a); output capacitance (b).

The comparative analysis showed that the characteristics of conduction losses, the volume of inductive components and the capacitor typical of a cascaded converter are worse than those of other topologies analysed in the paper. As compared to a similar charge-pump topology, the two-phase interleaved bidirectional DC-DC converter has larger total voltage stress on power switches, whereas the conduction losses and the volume of the inductor are similar.



(a) (b) (c)

Fig. 7. Comparative analysis in terms of weighted criteria at constant output power: for $V_{OUT} = 0.1 \cdot V_{IN}$ (a); for $V_{OUT} = 0.2 \cdot V_{IN}$ (b); for $V_{OUT} = 0.4 \cdot V_{IN}$ (c).

TABLE I. SUMMARIZED COMPARISON RESULTS AT CONSTANT OUTPUT POWER.

Criteria	Topologies		
	Two-phase interleaved bidirectional converter (Fig. 1(a))	**Two-phase interleaved bidirectional charge-pump converter (Fig. 1(b))**	**Cascaded bidirectional converter (Fig. 1(c))**
Total voltage stress	$T_W = 4 \times V_{IN}$	$T_W = 2{,}5 \times V_{IN}$	$T_W = 2 \times V_{IN} + V_O$
Conduction losses	$P_{CL} = 2 \times \left(I_{L_1}^2 + \frac{\Delta I_{L_1}^2}{12} \right) \times R_{DSon}$	$P_{CL} = (2+D) \times \left(I_{L_1}^2 + \frac{\Delta I_{L_1}^2}{12} \right) \times R_{DSon}$	$P_{CL} = 2 \times \left(I_{L_o}^2 + \frac{\Delta I_{L_o}^2}{12} \right) \times R_{DSon}$
Maximum energy stored in the inductors	$E_{LW} = 2 \times L \times \frac{64 \times P_O^2 \times (V_{IN} - V_O)}{7 \times V_{IN}^3}$	$E_{LW} = 2 \times L \times \frac{64 \times P_O^2 \times \left(\frac{V_{IN}}{2} - V_O \right)}{3 \times V_{IN}^3}$	$E_{LW} = L \times \frac{256 \times P_O^2 \times (V_{IN} - V_O)}{7 \times V_{IN}^3}$
Maximum energy stored in the capacitor	$E_{CW} = C \times \frac{2 \times \left(1 - 2 \times \frac{V_O}{V_{IN}} \right) \times V_O^2}{3}$	$E_{CW} = C \times \frac{\left(2 - 8 \times \frac{V_O}{V_{IN}} \right) \times V_O^2}{2}$	$E_{CW} = C \times \frac{4 \times \left(1 - \frac{V_O}{V_{IN}} \right) \times V_O^2}{7}$

On the other hand, a charge-pump converter has a limitation because its output voltage cannot exceed $V_{IN}/4$. It restricts the use of such topology in real applications. In the context of further work, the results obtained will be used to choose an appropriate converter topology for low-medium power portable applications.

V. BIDIRECTIONAL DC-DC INTERLEAVED CONVERTER EXPERIMENTAL PROTOTYPE

To verify the proposed comparison method, the models of two converters were analysed in PSIM software. Two-phase interleaved charge pump topology was eliminated due to the

limitation on the input to the output voltage relationship. Therefore, models of two-phase interleaved and cascaded topologies were studied in charge and discharge modes with DC-link voltage 12 V and battery voltage 7.2 V. It was concluded that the results observed have a very good correlation with those theoretically received.

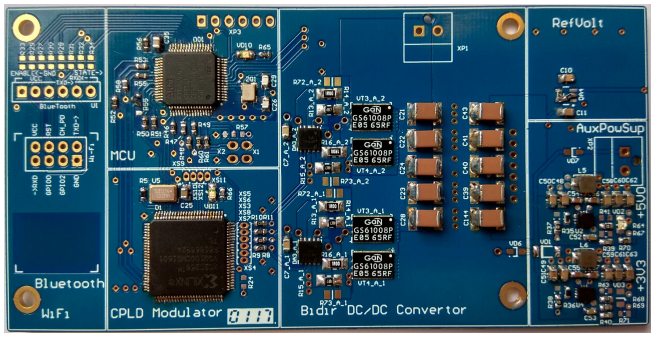
Finally, the conventional bidirectional interleaved DC-DC converter was accepted as the best solution. Figure 8 shows the developed 100 W prototype (top view) along with thermal images.

GaN-based transistors GS61008P from GaN Systems were used as a switching device in the experimental prototype. The power source chosen was 2 series connected $LiFePO_4$ 18650 cells from A123 Systems with a cutoff voltage from 2 V till 3.6 V and nominal voltage 3.3 V. Prototype parameters are presented in Table II. To reduce conduction losses and decrease overall volume, custom-made inverse coupled inductors were used. The control system is a combination of MCU (STM32F410R8) for data processing and control and CPLD (XC2C256-7VQ100C) for high-frequency PWM generation.

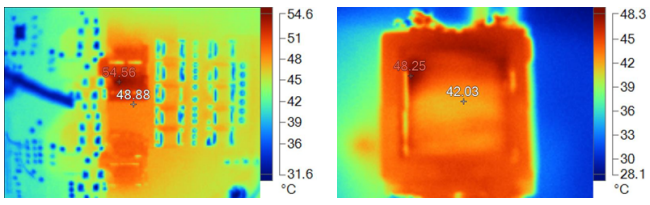
Switching frequency of the two cases was tested: 500 kHz and 800 kHz. Figure 9 shows the voltage and current diagrams across the transistor and the inductor, correspondingly. It should be noted that the voltage spike across the GaN transistors is present. It can be explained by zero deadtime set in the control system in order to minimize conduction losses of GaN transistors.

TABLE II. PARAMETERS OF THE EXPERIMENTAL PROTOTYPE.

Parameter	Value
Input voltage, V_{IN}	4..7.2 V
Output voltage, V_O	12 V
Maximum input current, I_{IN}	15 A
Maximum output power, P_{Omax}	100 W
Switching frequency, f_{SW}	500 kHz
Magnetic inductance, L_S	350 nH
Coupling coefficient,	-0.4
Input/output capacitors, C_{IN}/C_O	110 µF
GaN transistors	GS61008P
Transistor drivers	LM5113



(a)



(b) (c)

Fig. 8. Developed 100 W prototype (top view) of the bidirectional interleaved converter (a) and thermal images under full load condition transistors (b), an inductor (c).

To estimate total power losses in the converter and prove the right choice of the topology, efficiency was measured by the precision power analyser Yokogawa WT1800 (Fig. 10).

Rough total losses distribution in the converter during maximum load operation is illustrated in Fig. 11. It should be noted that the efficiency analysis does not include losses in the control system, which are about 0.54 W. Conduction losses were calculated using the measured current, the duty cycle and the on-state transistor resistance obtained from the datasheet.

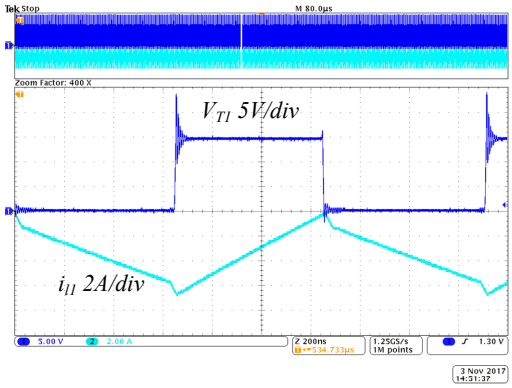


Fig. 9. Voltage waveform across the transistor and current waveform across the inductor.

Resistive-based current sensor losses were measured in the same way. Calculation of the switching losses of the transistor was obtained using the numerical values from the transistor datasheet and measured by the oscilloscope Tektronix MSO4043B with passive probes and current probe Tektronix TCP0030A with a bandwidth no less than 100 MHz. Coupled inductor losses were found by subtracting losses of the switches and the current sensor from the total losses. Obtained results were verified with the help of temperature analysis measured by a thermal imaging camera Fluke Ti10. Theoretically, received results show good correlation with those of the thermal analysis.

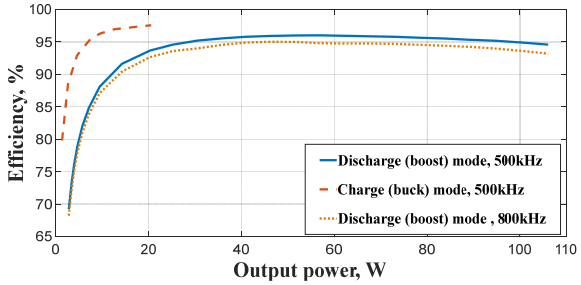
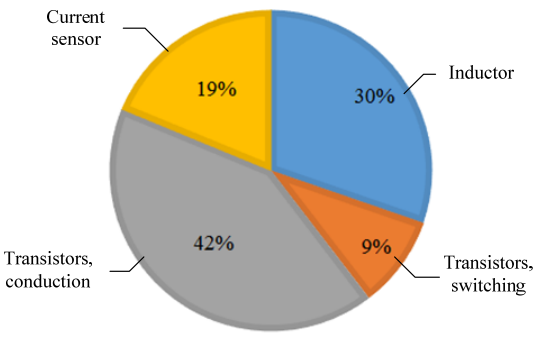


Fig. 10. Overall efficiency of the two-phase interleaved bidirectional converter.



5.83W total losses

Fig. 11. Power losses distribution in the converter at maximum load.

VI. CONCLUSIONS

This paper proposes comprehensive comparative analysis in order to define the optimal topology for the bidirectional DC-DC converter for low power energy storage applications. Focus in the analysis was concentrated on four parameters: conduction losses, voltage stress, the volume of inductive, and capacitance elements (reflected by maximum energy stored in such components).

Based on proposed approach it is shown that a conventional bidirectional buck-boost interleaved converter can be considered as one of the most suitable solutions. In addition, it was experimentally proven that in combination with modern semiconductor devices, very high efficiency and power density can be achieved.

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