Control of AC/DC Modular Multilevel Converter

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***Abstract*—In recent years, a special attention is paid to grid connected multilevel converters. These converters have specific use in industry in a high power, medium-voltage and high-voltage applications. This paper presents new control algorithm for single-phase AC/DC modular multilevel converter with target application as a traction converter connected directly to trolley wire. The proposed control strategy presents resonant controllers for converter current control with fundamental frequency adaptation. The fundamental frequency estimation and voltage synchronization is based on Second Order General Integrator Phase Locked Loop (SOGI-PLL). Furthermore, this paper presents robust voltage balancing technique for multilevel converter based on energy calculation of DC-link capacitances. It provides voltage balancing of multilevel converter cells with unbalanced load. The resulting control algorithm has low total harmonic distortion of converter trolley current even under unbalanced load condition. The algorithm was experimentally verified on the low voltage laboratory prototype with 3 H-bridge cells.**

***Index Terms*—AC/DC converter; Adaptive resonant controller; Modular multilevel converter.**

I. INTRODUCTION

The objective of this research is to develop a modular multilevel converter used as AC/DC converter for traction application. The multilevel converters have become indispensable in high-voltage high-power applications. The main domain of medium-voltage and high-voltage multilevel rectifiers are smart grids and new power grid networks (area of grid connected converters). The multilevel inverters are used as a controlled source for high power drives and high-voltage inverters for energy transfer.

The common medium and high-voltage converter topologies are neutral point clamped, flying capacitor and cascaded h-bridge (CHB) converters. The other popular types are based on hybrid topology [1]. In recent years, the most attention is paid to multilevel converters based on CHBs.

The CHBs used as an input AC/DC converter for traction converter with medium-frequency transformer are well described in [2]–[4]. The CHB converters used as a grid connected converters are presented in [2]–[10]. This topology is favourite choice also in many other industrial applications such as power electronics transformers (PET) [3], [5], [6], [10] or voltage-source inverters [7]. Furthermore, the single-phase multilevel rectifiers are often used as primary converters in AC electric traction.

The control algorithms for CHBs commonly consist of three basic parts: output current control, total DC-link voltage control and voltage balancing control of individual H-bridge cells. The paper presents novel algorithm for CHB rectifier control focused on system robustness with voltage amplitude and frequency adaptation on AC side and voltage balancing method compensating load imbalance on DC sides.

For output current control are common hysteresis control [11] or PWM based control techniques. The hysteresis control is simple and robust however, it leads to various switching frequency and wide noise bandwidth. For this reason, PWM techniques dominate in high power applications. For three phase systems, the most popular control algorithm with PWM modulation are based on a vector control theory (called d,q or PQ control) [12], [13]. Nowadays, the popular topic in scientific community is model predictive control. However, these types of controllers are computationally demanding and depend on a predictive model accuracy. The model predictive current control of CHB topology achieves good behavior under symmetrical load, but it does not provide adequate control during non-symmetrical load (HB cells are loaded by different power).

The proposed solution is intended for single-phase trolley wire system. In single phase systems, the most popular current controllers are PR (proportional-resonant) regulators. The main disadvantage of this controller is fixed narrow band frequency. The resonant frequency is set to nominal frequency of AC trolley wire voltage (50 Hz in this case). However, the fundamental frequency fluctuates in range of 48.5 Hz to 51.5 Hz in central Europe. This can cause phase shift between required current and actual current which was controlled by a fixed PR controller. For this reason, frequency adaptation for current resonant controller is used in the study.

Manuscript received 16 February, 2018; accepted 30 July, 2018.

This paper has been financed by Ministry of Education, Youth and Sports of the CR under the RICE – New Technologies and Concepts for Smart Industrial Systems, project No. LO1607.

A suitable and precise synchronization method is very important for reference current calculation in grid connected converters. For synchronization of three phase converters, the most popular methods are phase locked loops with Clarke and Park transformation. However, the Clarke transformation is not suitable in single phase systems. The common synchronization methods in single phase systems are based on discrete Fourier transform or on single phase PLL methods. The advantage of PLL over DFT methods is in grid fundamental frequency fluctuation resistivity. The SOGI-PLL (second order general integration phase locked loop) is used in this case. This synchronization is robust and accurate [14].

The voltage balancing of multilevel converters (CHB, FC etc.) plays crucial role, especially in unbalanced load condition [13], [15], [16]. The proper balancing method ensures the high voltage DC-link distribution over all converter power cells and semiconductors. This paper introduces voltage balancing method based on direct energy calculation. This energy is calculated for each HB during one period (0.02 s).

II. PROPOSED CONTROL

The control algorithm is shown in Fig. 1. The presented control algorithm can operate under non-symmetrical load condition. This can cause voltage imbalance, which must be compensated by voltage balancing block. The individual DC voltages U_{HB1}, U_{HB2}, U_{HB3} are controlled to average required voltage $U_{HBw}/3$. The total DC-link voltage ΣU_{HB} is controlled to value U_{HBw} by standard linear PI (proportional-integral) controller. The output of the voltage controller forms amplitude of required current i_w. The converter current is regulated by adaptive PR controller. The output signal u_{v_PR} is summed with feedforward signal u_{v_ff}. The SOGI PLL voltage synchronization is used to obtain an actual voltage phase and frequency to form required current i_w, feedforward voltage u_{v_ff}, adaptive PR controller (ω_{PLL}). Modulation for each HB is solved separately by PS-PWM according to voltage balancing block.

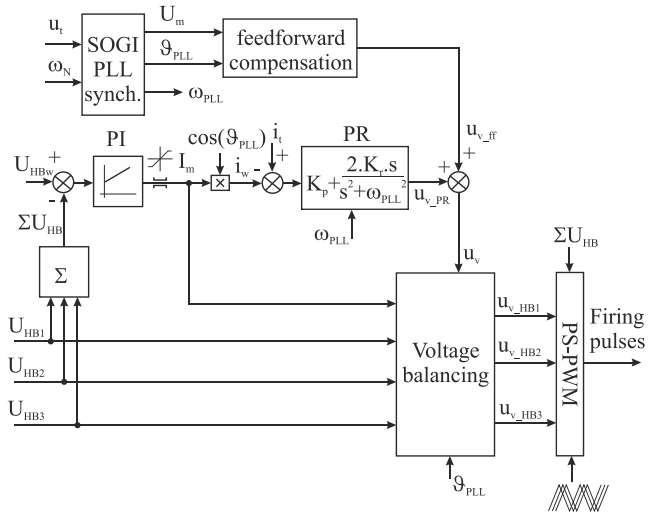

Fig. 1. Proposed control of AC/DC modular multilevel converter.

The Fig. 2 presents connection of SOGI-PLL synchronization circuit. This type of synchronization is a popular technique described in technical articles [14], [17], where it is used for both single-phase and three-phase systems. The main influence of gain K_{SOGI} is hook time of PLL, on the other hand high gain decrease SOGI-PLL filtering effect.

The SOGI-PLL synchronization is composed of PLL part and SOGI part. The PLL part is based on Park's transformation, where the real and imaginary voltage parts (u_α, u_β) are input signals. The active and reactive parts of rotating reference frame (u_q, u_d) are calculated according to (1) and (2). The PI controller (PI cont.) controls reactive voltage part (u_d) to zero value by signal $\Delta\omega$ correction. The resulted angular velocity ω_{PLL} is used for calculation of voltage position ϑ_{PLL}.

The SOGI part provides resistance to AC voltage (u_{ac}) noise and interference. This resistance is ensured by double integration of input signal. Result of the first integration is real voltage part and result of the second integration is imaginary voltage part. These voltage signals (u_α, u_β) are used for calculation of voltage magnitude U_m:

$$u_q = u_a \times \cos(\vartheta_{PLL}) + u_\beta \times \sin(\vartheta_{PLL}), \quad (1)$$

$$u_d = u_\beta \times \cos(\vartheta_{PLL}) - u_a \times \sin(\vartheta_{PLL}). \quad (2)$$

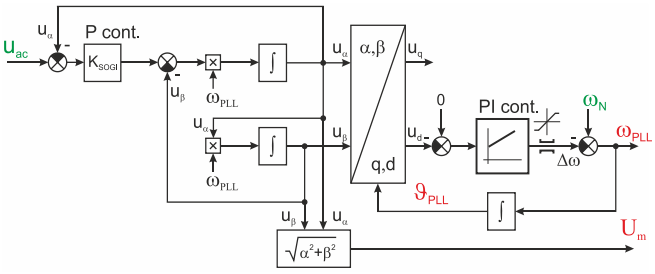

Fig. 2. Single-phase SOGI-PLL synchronization used for AC voltage.

The adaption to voltage frequency fluctuation is benefit of proposed control with adaptive resonant controllers. The SOGI-PLL reaction to step change of voltage frequency from 50 Hz to 48 Hz is shown in Fig. 3.

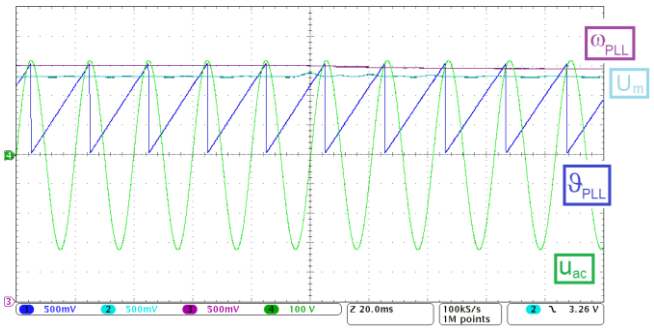

Fig. 3. SOGI-PLL reaction to change of frequency from 50 Hz to 48 Hz ch1: voltage position ϑ_{PLL}, ch2: PLL evaluated amplitude U_m, ch3: PLL evaluated angular frequency ω, ch4: input voltage signal u_{ac}.

The adaptive resonant controller uses information about voltage frequency directly from SOGI-PLL (ω_{PLL}). The output of resonant controller is supplemented by the sinewave limiter as a shown in Fig. 4. The multilevel converter reaction to change of voltage frequency from 50 Hz to 51 Hz is shown in Fig. 5. During this transient is

current i_t shifted against voltage u_t (approximately three period). Proposed algorithm is well resistant against voltage drops. The trolley's voltage step change from 230 V to 207 V is shown in Fig. 6.

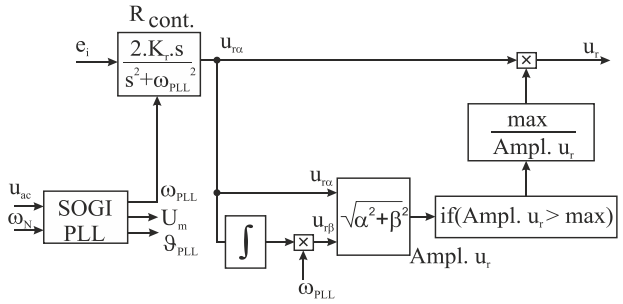

Fig. 4. Adaptive resonant controller with sinus limiter in detail.

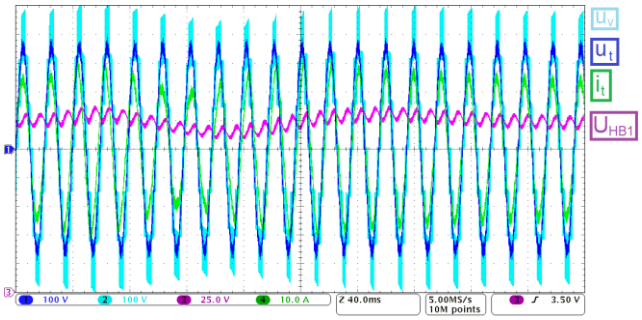

Fig. 5. Converter transient under step change of frequency from 50 Hz to 51 Hz, ch1: trolley voltage u_t, ch2: voltage at converter ac terminals u_v, ch3: DC-link voltage at first HB U_{HB1}, ch4: trolley current i_t.

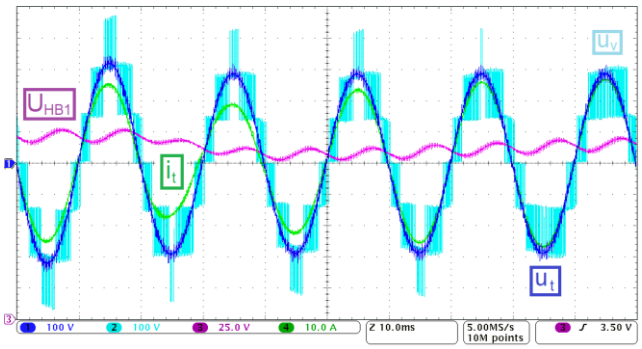

Fig. 6. Converter transient under step change of trolley voltage from 230 V_{RMS} to 207 V_{RMS}, ch1: trolley voltage u_t, ch2: voltage at converter AC terminals u_v, ch3: DC-link voltage at first HB U_{HB1}, ch4: trolley current i_t.

The voltage balancing block is based on power equality by (3). If the voltage on each cell is equal to the average voltage, then the power of AC side is equal to DC side power. For the different voltage, it is possible to calculate the difference of the modulation signal by using (4).

The balancing voltage change is allowed just once per period to suppress the effect of the second harmonic at the DC-link:

$$\frac{U_m \times I_m}{2} = U_{HB1} \times i_{HB1} + U_{HB2} \times i_{HB2} + U_{HB3} \times i_{HB3}, \quad (3)$$

$$u_{vHB} = u_v \times \left(1 + \frac{3.50 \times C \left(U_{HBaverage}^2 - U_{HB}^2 \right)}{\left(U_m \times I_m \right)} \right). \quad (4)$$

In Fig. 7 is shown behaviour under steady-state condition and symmetrical load. The voltage at multilevel AC terminals u_v has 7 levels leads to low current ripple. A phase shifted pulse width modulation (PS-PWM) ensures regular switching of each HB cell. However, during non-symmetrical load Fig. 8. The HB cell switching is not regular. That is caused by balancing block influence and resulted current ripple is higher. The voltage u_v changes rapidly across different voltage levels. The resulting THDi increase form 1.05 % to 3.34 %.

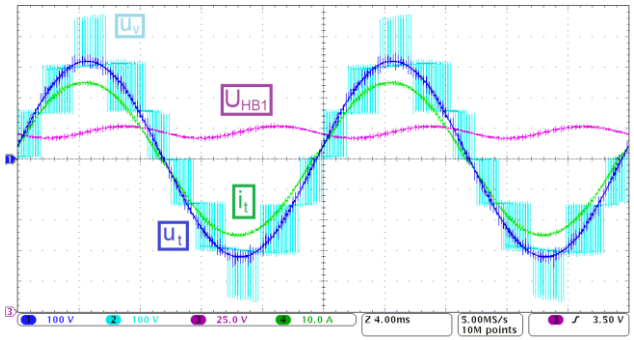

Fig. 7. Converter under steady-stay condition – symmetrical load 4 kW (HB1 1.33 kW, HB2 1.33 kW, HB3 1.33 kW), current THDi = 1.05 %, ch1: trolley voltage u_t, ch2: voltage at converter ac terminals u_v, ch3: DC-link voltage at first HB U_{HB1}, ch4: trolley current i_t.

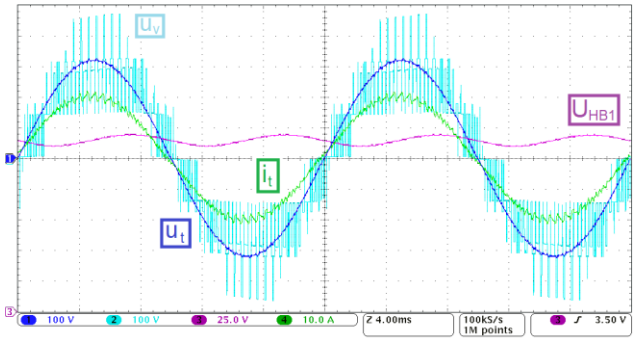

Fig. 8. Converter under steady-stay condition – non-symmetrical load (HB1 1.33 kW, HB2 0.66 kW, HB3 1.33 kW), current THDi = 3.34 %, ch1: trolley voltage u_t, ch2: voltage at converter ac terminals u_v, ch3: DC-link voltage at first HB U_{HB1}, ch4: trolley current i_t.

In Fig. 9 is shown the multilevel converter behaviour after voltage balancing block start. The voltage difference of individual HB DC-link voltages is significantly reduced, even if 25 % non-symmetry load is applied to second HB. The voltage difference between voltage U_{HB1} and U_{HB3} is caused by different capacitor value (manufactory tolerances). This difference is fully compensated.

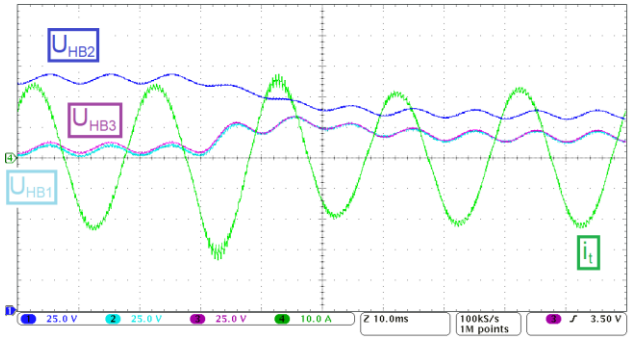

Fig. 9. Converter under non-symmetrical load (HB1 1.33 kW, HB2 1 kW, HB3 1.33 kW), after start of voltage balancing, ch1: DC-link voltage at second HB U_{HB2}, ch2: DC-link voltage at first HB U_{HB1}, ch3: DC-link voltage at third HB U_{HB3}, ch4: trolley current i_t.

The single phase multilevel converter has been tested on developed low-voltage prototype with rated power 4 kW, Fig. 10. The voltage source u_t is emulated by programmable power source California, which allows precise setting of voltage magnitude U_m and voltage frequency ω. The multilevel converter itself is composed of 3 HB cell, where the load of each cell can be set separately. The multilevel converter PWM carrier frequency for each cell is 1 kHz. A detailed description of modulator used for multilevel converter can be found in [21].

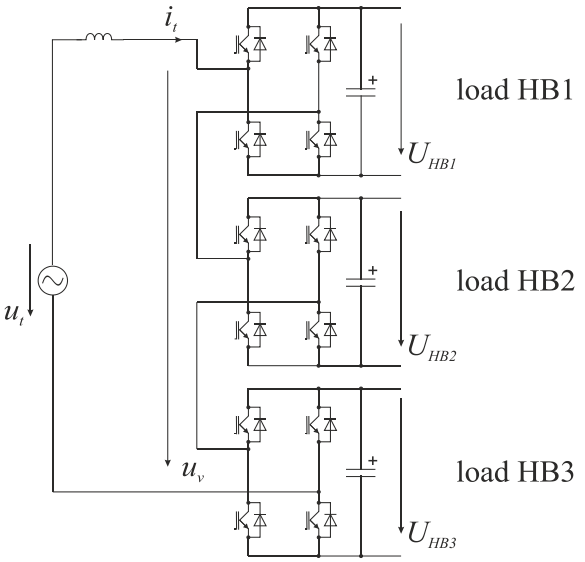

Fig. 10. Single-phase AC/DC Modular Multilevel Converter laboratory prototype with possibility of non-symmetrical loading.

III. CONCLUSIONS

In general, the CHB main benefits are low current harmonic distortion and modular technology. However, the unbalanced load of CHB active rectifier can increase low-frequency current harmonics and total harmonic distortion (THD). This fact can result in failure to meet low-frequency EMC grid standards.

The switching frequency of our laboratory prototype is 1 kHz, which leads to 6 kHz dominant current frequency component of 7-levels CHB. However, current THD analysed up to 2.5 kHz increases with unbalanced load. The current THD under symmetrical load is close to 1 %. On the other hand, 75 % unbalanced load of one cell of CHB increased THD up to 2 %. The current spectrum in this case contains large component on 2 kHz. This frequency equals to two times of switching frequency of CHB.

Proposed CHB control algorithm combines direct current control based on adaptive resonant controllers with an advanced SOGI-PLL synchronization algorithm. The paper presents robust voltage balancing technique for CHB rectifier based on energy calculation. The experimental results show proper function of CHB control algorithm under symmetrical and non-symmetrical loads.

REFERENCES

[1] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, Bin Wu, J. Rodriguez, M. A. Perez, J. I. Leon, "Recent advances and industrial applications of multilevel converters", *IEEE Trans. Industrial Electronics*, vol. 57, no. 8, pp. 2553–2580, 2010. DOI: 10.1109/TIE.2010.2049719.

[2] M. Steiner, H. Reinold, "Medium frequency topology in railway applications", in *European Conf. Power Electronics and Applications*, Aalborg, Denmark, 2007, pp. 1–10. DOI: 10.1109/EPE.2007.4417570.

[3] C. Zhao, D. Dujic, A. Mester, J. K. Steinke, M. Weiss, S. Lewdeni-Schmid, T. Chaudhuri, P. Stefanutti, "Power electronic traction transformer medium voltage prototype", *IEEE Trans. Industrial Electronics*, vol. 61, no. 7, pp. 3257–3268, 2014. DOI: 10.1109/TIE.2013.2278960.

[4] V. Blahnik, Z. Peroutka, J. Molnar, J. Michalik, "Control of primary voltage source active rectifiers for traction converter with medium-frequency transformer", *13th Int. Power Electronics and Motion Control Conf.*, Poznan, Poland, 2008, pp. 1535–1541. DOI: 10.1109/EPEPEMC.2008.4635485.

[5] D. Dujic, Zhao Chuanhong, A. Mester, J. K. Steinke, M. Weiss, S. Lewdeni-Schmid, T. Chaudhuri, P. Stefanutti, "Power electronic traction transformer-low voltage prototype", *IEEE Trans. Power Electronics*, vol. 28, no. 12, 2013, pp. 5522–5534. DOI: 10.1109/TPEL.2013.2248756.

[6] T. Besselmann, A. Mester, D. Dujic, "Power electronic traction transformer: efficiency improvements under light-load conditions", *IEEE Trans. Power Electronics*, vol. 29, no. 8, pp. 3971–3981, 2014. DOI: 10.1109/TPEL.2013.2293402.

[7] E. Babaei, S. Laali, S. Alilu, "Cascaded multilevel inverter with series connection of novel h-bridge basic units", *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, 2014. DOI: 10.1109/TIE.2014.2316264.

[8] G. Buticchi, D. Barater, E. Lorenzani, C. Concari, G. Franceschini, "A nine-level grid-connected converter topology for single-phase transformerless PV systems", *IEEE Trans. Ind. Electron*., vol. 61, no. 8, pp. 3951–3960, 2014. DOI: 10.1109/TIE.2013.2286562.

[9] J. A. Munoz, J. R. Espinoza, C. R. Baier, L. A. Moran, J. I. Guzman, V. M. Cardenas, "Decoupled and modular harmonic compensation for multilevel STATCOMs", *IEEE Trans. Ind. Electron*., vol. 61, no. 6, pp. 2743–2753, 2014. DOI: 10.1109/TIE.2013.2276058.

[10] T. Gajowik, C. Sobol, S. Stynski, M. Malinowski, "Post-fault operation of hybrid DC-DC converter for Solid-State Transformer", *43rd Annual Conf. IEEE Industrial Electronics Society (IECON 2017)*, Beijing, China, 2017, pp. 5373–5379. DOI: 10.1109/IECON.2017.8216931.

[11] M. Khazraei, H. Sepahvand, M. Ferdowsi, K. A. Corzine, "Hysteresis-based control of a single-phase multilevel flying capacitor active rectifier", *IEEE Trans. Power Electronics*, vol. 28, no. 1, pp. 154–164, 2013. DOI: 10.1109/TPEL.2012.2197222.

[12] V. Valouch, M. Bejvl, P. Simek, J. Skramlik, "Power control of grid-connected converters under unbalanced voltage conditions", *IEEE Trans. Industrial Electronics*, vol. 62, no. 7, pp. 4241–4248, 2015. DOI: 10.1109/TIE.2014.2384473.

[13] E. Behrouzian, M. Bongiorno, R. Teodorescu, "Impact of switching harmonics on capacitor cells balancing in phase-shifted PWM-based cascaded HBridge STATCOM", *IEEE Trans. Power Electronics*, vol. 32, no. 1, pp. 815–824, 2017. DOI: 10.1109/TPEL.2016.2535481.

[14] A. Kulkarni, V. John, "A novel design method for SOGI-PLL for minimum settling time and low unit vector distortion", in *39th Annual Conf. IEEE Industrial Electronics Society (IECON 2013)*, Vienna, Austria, 2013. DOI: 10.1109/IECON.2013.6699148.

[15] P. Karamanakos, K. Pavlou, S. Manias, "An enumeration-based model predictive control strategy for the cascaded H-Bridge multilevel rectifier", *IEEE Trans. Industrial Electronics*, vol. 61, no. 7, pp. 3480–3489, 2014. DOI: 10.1109/TIE.2013.2278965.

[16] H. Iman-Eini, J. L. Schanen, S. Farhangi, J. Roudet, "A modular strategy for control and voltage balancing of cascaded H-bridge rectifiers", *IEEE Trans. Power Electronics*, vol. 23, no. 5, pp. 2428–2442, 2008. DOI: 10.1109/TPEL.2008.2002055.

[17] Siyu Gao, M. Barnes, "Phase-locked loop for AC systems: Analyses and comparisons", in *6th IET Int. Conf. Power Electronics, Machines and Drives (PEMD 2012)*, Bristol, UK, 2012, pp. 1–6. DOI: 10.1049/cp.2012.0199.

[18] T. Kosan, M. Jara, V. Blahnik, Z. Peroutka, "A universal configurable sinusoidal modulator for H-bridge based converters implemented in FPGA", *Int. Conf. Applied Electronics (AE 2015)*, Pilsen, Czech Republic, 2015, pp. 111–114.