Novel First Order Current Mode MOS-C Phase Shifters

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***Abstract*—In this work, novel first order MOS-C phase shifter structures are proposed in NMOS and PMOS configurations. Core circuits consist of only three transistors and a single capacitor. The pole frequency of the phase shifters can be easily controlled by the bias voltage. The presented circuits in this work bring advantages such as low power consumption and small chip area when compared to other works including large numbers of active and passive elements in the literature. Furthermore, the proposed circuits are designed with a simple design automation flow that is proper for MOS-Only or MOS-C architectures. It is shown by simulations that the simulation results agree with the theoretical results for a wide frequency range.**

***Index Terms*—All-pass; Current mode; Phase shifter; MOS-Only; MOS-C; Polynomial regression; Design automation.**

I. INTRODUCTION

MOSFET-only (MOS-Only) and MOSFET-C (MOS-C) architectures gain significant interest and importance owing to small chip area, low power consumption and suitability for high frequency applications. In this work, novel MOS-C circuits are presented so that they are proper where low power and small chip area are required. In addition, all-pass functions are widely utilized in the analog signal processing in order to shift or delay the phase of the input signal without changing its amplitude. Hence, the circuits having uniformly all-pass responses are also called phase shifters. This work proposes novel first order current mode phase shifters which can be adjusted electronically.

When the literature is examined in detail, a large number of voltage mode (VM) [1]–[12] or current mode (CM) [12]–[23] all-pass circuits have been presented. However, current mode circuits enjoy some advantages such as high bandwidth, low voltage operation and wide dynamic range when compared having VM circuits [24]. Some published CM all-pass circuits with at least 19 transistors and capacitances are observed in [12]–[20]. Also, [12], [16], [17], [22] contain passive resistances. All-pass filters are proposed in [21] which employ 10 transistors and a capacitor. As for [22], it employs two transistors, two resistors and two capacitors in order to implement an inverting and non-inverting phase shifter. It requires two additional current followers so as to obtain phase shifter functions. The presented CM all-pass filter [23] employs single Z-copy voltage differencing current conveyor (ZC-VDCC) and grounded capacitor. Internal structure of ZC-VDCC in the paper comprises of commercial available components. Therefore, there is a high frequency restriction owing to parasitic impedances and frequency dependent non-ideal gain effects. Table I compares the main performance parameters of the proposed first order CM all-pass filters and the other ones. As far as power consumption and area are concerned, the proposed first order CM phase shifter circuits are better than the previously reported structures excluding [21] in terms of power consumption.

TABLE I. COMPARISON OF THE PREVIOUSLY PRESENTED ALL-PASS CIRCUITS.

References	Topology	# of passive elements	# of transistors[a]	Area[b] (μm^2)	Power Cons. (μW)
[12]	DCCII	1C/3R	24 MOS	490	1300
[13]	ZC-CDTA	1C	34 BJT	NA	NA
[14]	CCCII	1C	19 BJT	NA	NA
[15]	DO-CCII	1C	42 MOS	884.61	NA
[16]	DO-CCII	1C/1R	32 MOS	106	2180
[17]	DX-MOCCII	1C/1R	28 MOS	142.24	NA
[18]	CCCII	1C	34 MOS	149.1	NA
[19]	CDTA	1C	66 BJT	NA	9000
[20]	CDTA	1C	56 BJT	NA	NA
[21]	DO-CF	1C	10 MOS	31.49	266
[22]	IVB	2C/2R	2 MOS	27.04[c]	NA
[23]	ZC-VDCC	1C	CAD	NA	NA
NMOS based AP	MOS only	1C	8 MOS	15.4	760
PMOS based AP	MOS only	1C	8 MOS	20.7	435

Note: NA: not mentioned, CAD: commercially available device, [a]Sum of products of the lengths and widths of each transistor in the CMOS structures, [b]Ideal current source assumed, [c]Excluding current follower for each output. Full nomenclatures of topologies are given in the Appendix A.

Another important difficulty is the long design cycles and suffering from the chain of the computational steps for the

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analog circuit design and MOS circuit applications. This work uses a design automation flow that can be easily employed for MOS-Only and MOS-C designs. Against to convex programming based design automation in [25], [26] and genetic algorithm in [27], this work makes use of a design automation based on a polynomial regressive method which is discussed extensively in [28].

The organization of the paper is as follows: Section II describes the proposed architectures with aforementioned design automation flow. SPICE simulation results are given in Section III. Section IV concludes the paper by significant remarks.

II. The Proposed Phase Shifter Architectures Using the Design Automation Flow

First of all, proposed phase shifters make use of the design automation flow, which is presented in [28] extensively. Hence, design cycle starts with this methodology. The automation cycle described in [28] comprehensively can be shown in Fig. 1. So, this flow is summarized briefly in order to introduce its working principle. In the beginning of the automation, random netlists are generated and AC or/and DC characteristics of them are extracted automatically. The proper ones which have well-functioned characteristics are picked up and sent to the design cycle as a core circuit. After checking whether the designer dependent constraints such as power, cut-off frequency, input or output impedance, quality factor etc, are satisfied, the bias circuit is produced to the core circuit for satisfying DC operation conditions for saturation region operation especially. In this regard, we eliminate the chain of hand calculations and user intervention and reduce the overall design time. Furthermore, sized circuits in the end of automation give simulation results in SPICE, which match to the automation results with high accuracy up to 3 % mean error. Overall automation mechanism is discussed in [28].

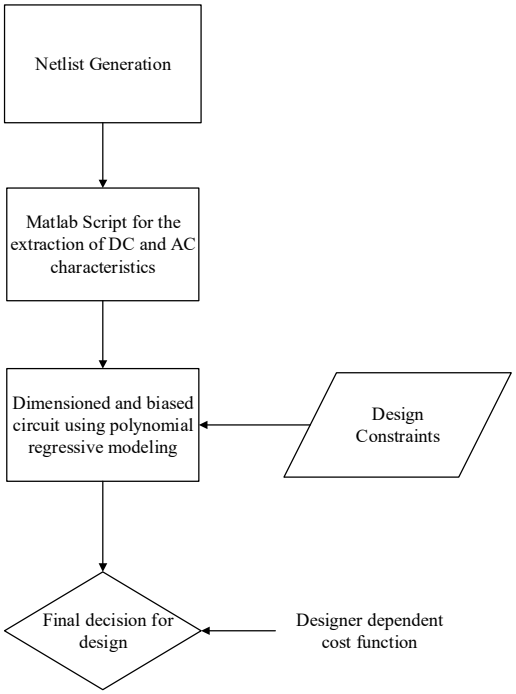


Fig. 1. Used MOS-Only/MOS-C design automation flow [28].

In the end of aforementioned automation cycle, the proposed PMOS and NMOS first order current mode phase shifters are given in Fig. 2(a) and Fig. 2(b), respectively. Core structures consist of three transistors and a capacitor. It is assumed that all transistors are operated in the saturation region.

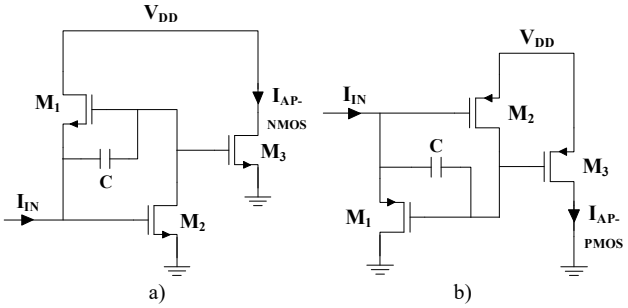


Fig. 2. Proposed first order phase shifters: a) NMOS based; b) PMOS based.

If MOS transistors' dominant capacitors C_{gs} and C_{gd} are omitted with regard to C, the following equations can be given easily:

$$\frac{I_{AP-NMOS}}{I_{IN}} = -\frac{g_{m3}\left(g_{m2} - sC\right)}{g_{m2}\left(g_{m1} + sC\right)}, \tag{1}$$

$$\frac{I_{AP-PMOS}}{I_{IN}} = \frac{g_{m3}\left(g_{m2} - sC\right)}{g_{m2}\left(g_{m1} + sC\right)}. \tag{2}$$

If we assume that $g_{m1} = g_{m2} = g_m$, NMOS phase shifter gives inverting all-pass function and the PMOS one produces non-inverting all-pass output. In this regard, the pole frequency and gain expressions are the same for both of them and given in (3), respectively:

$$\begin{cases} \omega_0 = \dfrac{g_m}{C}, \\ H_0 = \dfrac{g_{m3}}{g_m}. \end{cases} \tag{3}$$

The filters' gain can be tuned by g_{m3}. Taking (1) and (2) into consideration, the phase response of the filters can be calculated as follows, respectively:

$$\Phi(\omega) = \pi - 2\tan^{-1}\left(\omega\frac{C}{g_m}\right), \tag{4}$$

$$\Phi(\omega) = -2\tan^{-1}\left(\omega\frac{C}{g_m}\right). \tag{5}$$

When the core structures in Fig. 2 are examined carefully and the condition ($C_{gs1} >> C_{gs2}$, C_{gs3}) is satisfied, those can be employed without external capacitors. However, it is not matter anymore so that poly1-poly2 layers allow us to use floating capacitance on the chip [29]. Hence, aforementioned floating capacitor shown in Fig. 2 can be integrated into the MOS transistors.

If we take gate-source capacitances of the MOS devices into account, (1) is converted to (6) as follows

$$\frac{I_{AP-NMOS}}{I_{IN}} = \frac{-g_{m3}\left(g_{m2} - s\left(C + C_{gs1}\right)\right)}{g_{m2}\left(\begin{array}{l} g_{m1} + s\left(C_{gs3}\dfrac{g_{m1}}{g_{m2}} + C + C_{gs1}\right) \\ +s^2\left(\dfrac{\left(C + C_{gs1}\right)\left(C_{gs2} + C_{gs3}\right) + C_{gs2}C_{gs3}}{g_{m2}}\right)\end{array}\right)}. \quad (6)$$

In this case, the proposed phase shifters can be evaluated as first order all-pass filters under the following conditions:

$$\begin{cases} C_{gs1} << C, \\ C_{gs3}\dfrac{g_{m1}}{g_{m2}} + C_{gs1} << C, \end{cases} \quad (7)$$

$$\omega^2 << \frac{g_{m1}g_{m2}}{\left(C + C_{gs1}\right)\left(C_{gs2} + C_{gs3}\right) + C_{gs2}C_{gs3}}. \quad (8)$$

In the same way, another important restriction of the proposed filters can be observed in (8) for high frequency operation. So, (9) gives the maximum operating frequency of the proposed phase shifters

$$f_{max} \le \frac{0.1}{2\pi}\sqrt{\frac{g_{m1}g_{m2}}{\left(C + C_{gs1}\right)\left(C_{gs2} + C_{gs3}\right) + C_{gs2}C_{gs3}}}. \quad (8)$$

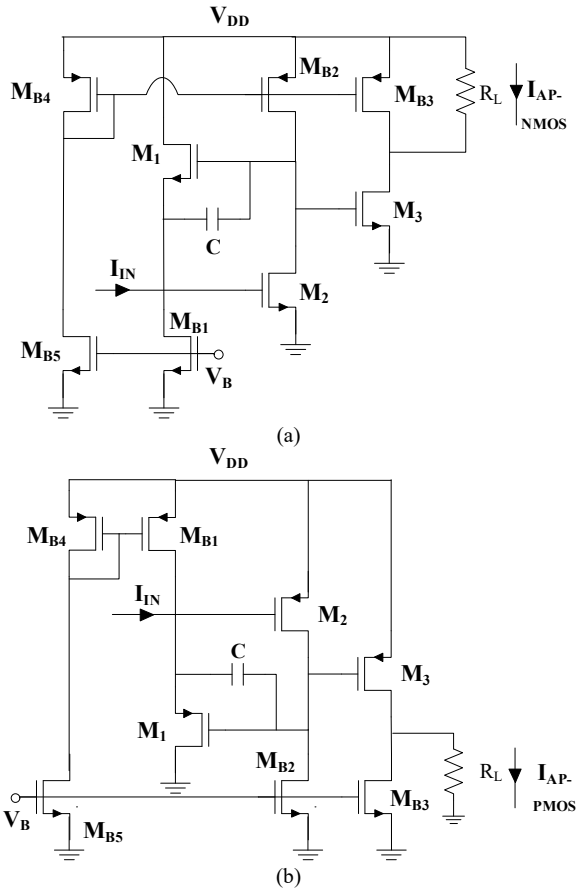


Fig. 3. Proposed first order phase shifters with bias transistors: a) NMOS based; b) PMOS based.

Overall structures are presented in Fig. 3. M_{B1}-M_{B5} are the bias transistors. Dimensions of the devices in 0.18µm Taiwan Semiconductor Manufacturing Company (TSMC) CMOS technology are given in Table II. In addition, the floating capacitor is selected as 5 pF.

In the end of this section, by considering Fig. 3, it is beneficial to clarify dependency between pole frequency and gain of the phase shifters. This dependency is easily eliminated by disconnection of the gate terminal of M_{B3} from V_B voltage port. Hence, phase shifters' gain can be easily tuned with these transistors' gate voltages with no change in pole frequency.

TABLE II. TRANSISTOR DIMENSIONS OF THE PROPOSED PHASE SHIFTERS.

DESIGNS	NMOS Based		PMOS Based	
Transistors	W(µm)	L(µm)	W(µm)	L(µm)
M_1, M_2	3	0.5	8	0.2
M_3	2	0.9	2	0.2
M_{B1}	3	0.4	8	0.5
M_{B2}	10	0.6	5	0.7
M_{B3}	4	0.2	6	0.4
M_{B4}	10	0.2	16	0.3
M_{B5}	3	0.2	8	0.3

III. SIMULATION RESULTS

Simulations have been realized in SPICE environment using 0.18 µm TSMC CMOS process parameters. The supply voltage is selected as 1.8 V. Load resistance is 1 kΩ and bias voltages (V_B) of the NMOS and PMOS structures are 0.65 V and 0.57 V respectively. The bulks of NMOS transistors are connected to ground while the bulks of PMOS transistors are connected to related sources. Meanwhile, power consumptions of them are measured as 760 µW and 435 µW, respectively. In this regard, when Fig. 3 and Table II are taken into account, small signal parameters are measured in SPICE environment as shown in Table III. Calculation parts in the Table are produced at the end of aforementioned automation cycle. Tabulated values show that SPICE results are in compliance with automation results.

TABLE III. THE COMPARISON OF THE SMALL SIGNAL CHARACTERISTICS BETWEEN MEASUREMENT AND AUTOMATION RESULTS.

DESIGNS	NMOS Based		PMOS Based	
Transistors	g_m(µA/V) Meas./Calc.	C_{gs} (fF) Meas./Calc.	g_m(µA/V) Meas./Calc.	C_{gs}(fF) Meas./Calc.
M_1	382/370	9.46/8.31	291/270	10.6/9.2
M_2	301/285	9.06/8.01	278/259	10.5/8.9
M_3	404/385	11.5/9.2	328/311	3.3/3.1

Gain and phase responses of the proposed phase shifters can be observed in Fig. 4. The pole frequency of the NMOS and PMOS shifters are measured as 9.4 MHz and 8.9 MHz for 5 pF floating capacitor. Moreover, the pole frequency is easily controlled by the bias voltage (V_B) for the NMOS phase shifter between 7.18 MHz and 11.4 MHz, whereas it can be changed between 5.88 MHz and 12.15 MHz for the PMOS phase shifter in the same way. Change of the pole frequency versus the bias voltage is depicted in Fig. 5.

To illustrate the performance of the proposed first order phase shifters, time domain analyses are given in the Fig. 6. Total harmonic distortion (THD)'s of the proposed NMOS and PMOS structures are measured as 1.04 % and 3.65 % respectively. In the time domain responses as shown in Fig. 6(a) and Fig. 6(b), phase shifting between input and output signals is measured as 89.4° and 91.6° respectively.

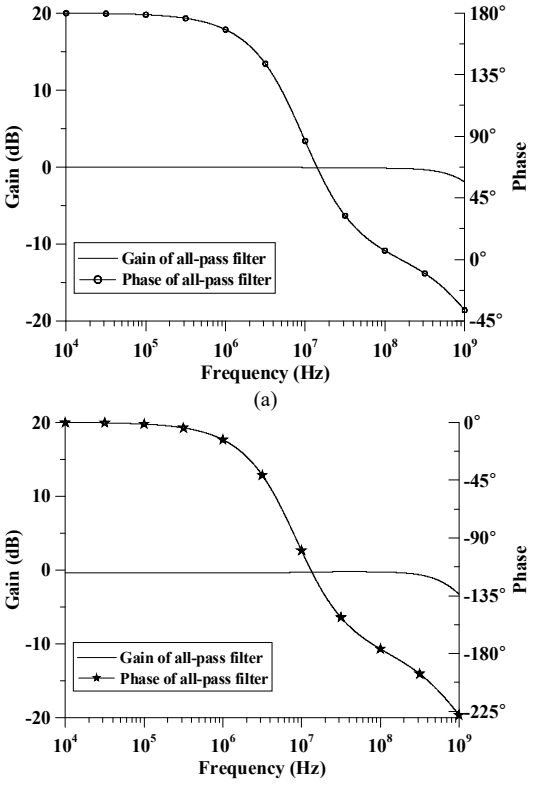


Fig. 4. Proposed first order phase shifters' frequency responses: a) NMOS based; b) PMOS based.

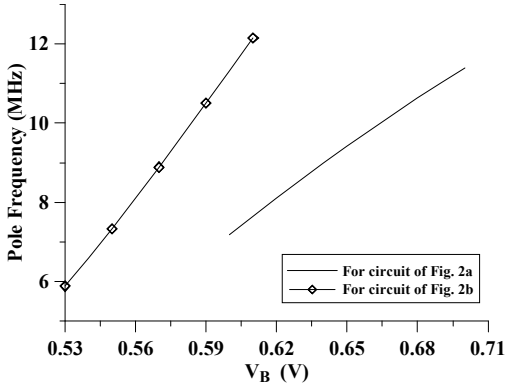
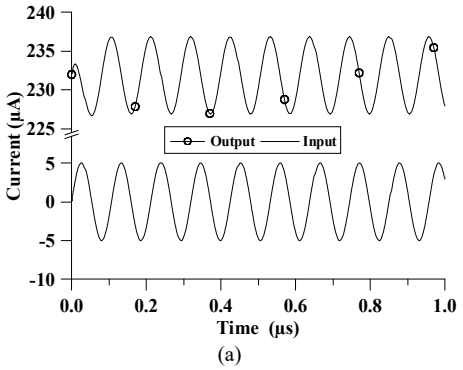


Fig. 5. The dependence of V_B versus pole frequency for the proposed circuits.



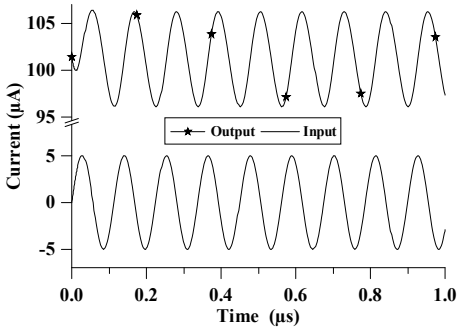


Fig. 6. Time domain analysis of the proposed structures for 10 $\mu A_{p\text{-}p}$ input current signals at the pole frequency: a) NMOS based; b) PMOS based.

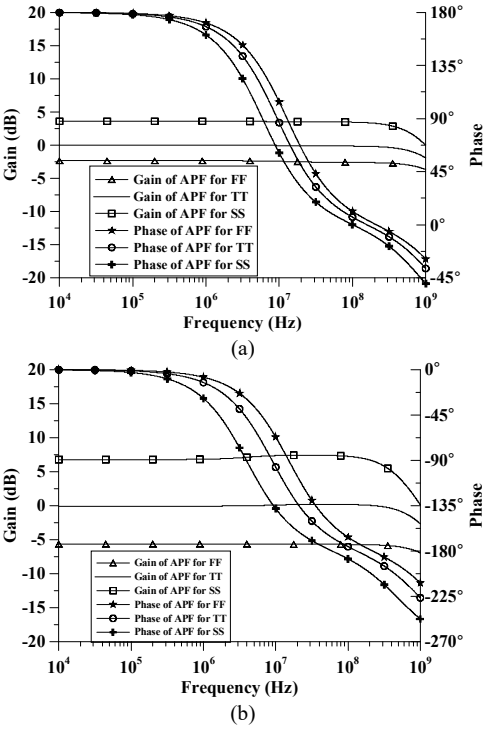


Fig. 7. Corner analyses of the proposed phase shifters with regard to FF, SS and TT transistors: a) NMOS based; b) PMOS based.

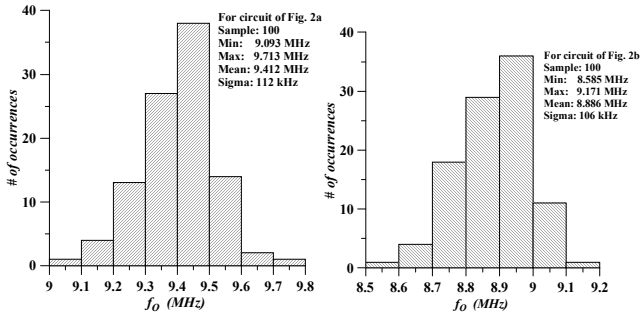


Fig. 8. Monte Carlo simulation for the proposed circuits a) NMOS based, b) PMOS based.

In the last part of this section, corner and Monte Carlo simulations are presented. In the first step, the variation of the phase shifters' gains and phase responses can be observed in Fig. 7 regarding process variations including SS, TT and FF transistors. In the second step, Monte Carlo simulation is given by changing the floating capacitor by 5 %, the effect of this capacitance is underscored. Histogram results of Monte Carlo analysis for the presented first order phase shifter circuits are shown in Fig. 8. For the NMOS based phase shifter; minimum, maximum and standard

deviation of the operating frequency were measured as 9.09 MHz, 9.71 MHz, and 112 kHz respectively whereas they were measured as 8.58 MHz, 9.17 MHz, and 106 kHz respectively for the PMOS based. Overall performance metrics proves that our proposed first order current mode phase shifters bring promising results to the designers.

IV. CONCLUSIONS

In this work, two novel current-mode first order phase shifter architectures are produced with a simple design automation methodology which reduces design time and the chain of the computation cycles. In the end of the automation two core architectures, which consist three transistors and a floating capacitor, are presented. Designers can use NMOS or PMOS type of the phase shifters depending on where the load connection is made. Also, the pole frequency of the shifters can be easily controlled electronically. Furthermore, the proposed phase shifters enjoy main advantages that small chip area, low power consumption and simple circuit structure. Simulation results prove performances of the phase shifters as well.

In addition, automation flow in this work, allows designers to easily construct any kind of circuit based on MOS-Only or MOS-C structure. Also, there will be no user interruption during the entire design cycle. Designers can make use of it in order to obtain different structures with improving of the accuracy between their pre-calculations before simulations and simulators' results.

APPENDIX A

This section indicates full nomenclature of the mentioned active elements in Table I. DCCII: Differential second generation current conveyor, ZC-CDTA: Z-copy current differential transconductance amplifier, CCCII: Second-generation current-controlled current conveyor, DO-CCII: Dual output second generation current conveyor, DX-CCII: Dual-X second generation current conveyor, DX-MOCCII: Dual-X second generation multi output current conveyor, CDTA: Current differential transconductance amplifier, DO-CF: Dual-output current follower, IVB: Inverting voltage buffer.

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