Design of Novel CMOS DCCII with Reduced Parasitics and its All-Pass Filter Applications

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***Abstract*—In this paper, a novel translinear loop based, high performance Complementary Metal-Oxide-Semiconductor (CMOS) second-generation differential current conveyor (DCCII) is introduced. By using super source follower transistors, very low equivalent impedances are obtained at input terminals x_n and x_p. In addition, new voltage-mode (VM) and current-mode (CM) first-order all-pass filters (APFs) are proposed to highlight the performance of the designed CMOS DCCII. The designed CMOS implementation is simulated with HSpice using AMS 0.35 µm real process parameters. It consumes only 1.3 mW power with using ±1.25 V power supply voltages. The simulation results of the proposed CMOS DCII circuit and the experimental results for designed VM APF are in very good agreement with the theoretical ones.**

***Index Terms*—Analog signal processing; all-pass filter; current-mode; voltage-mode; DCCII; reduced parasitic; super source follower; translinear loop.**

I. INTRODUCTION

Numerous well-known advantages of current-mode (CM) circuits such as high bandwidth, greater linearity, low-voltage operation, and wide dynamic range are made them popular in the fields of analog signal processing and integrated circuit design [1]–[5]. In the open technical literature excessive number of CM circuits exist that promote solutions to a wide spectrum of applications. For an instance works [6]–[16] and references cited therein can be mentioned. Over the last decades a significant research was performed in order to design high performance, low-voltage low-power CM circuits mainly due to the requirement of efficient portable electronic systems with long battery lifetime [10]–[23].

From internal structure implementation point of view, the current subtractor (CS) with current differencing capability [24], [25] forms one of the most important sub-stages of recently proposed high-performance CM active building blocks (ABBs) such as current differencing transconductance amplifier (CDTA) [6], [7], [21], current differencing buffered amplifier (CDBA) [8], [16], [20], [22], operational transresistance amplifier (OTRA) [3], [17], or second-generation differential current conveyor (DCCII) [11]–[15]. Although the DCCII element was the first active component in the open literature combining the simplicity of the conventional CCII [1] with current differencing attribute of the conventional CDBA [8], it has not received as much attention as the CDBA yet and up to now only few integrated circuit implementations are available [11]–[14]. In order to show versatility of DCCII and increase its importance for analog signal processing, recently it was used as the main sub-block in a frequency compensation scheme of three-stage amplifier [15]. It is well-known in analog circuit design that reduction of unwanted parasitic terminal capacitance and resistance values increase the bandwidth of a circuit, because of the product of these two quantities form a dominant pole. In accordance with this theory, within this paper a novel CMOS implementation of a low-voltage and low-power high performance DCCII is proposed. The developed internal structure consists of a class AB input stage based on high performance translinear-loop, a CS stage, and a current mirror stage. Compared to previously published CMOS DCCII implementations [11]–[14], here proposed circuit has very low equivalent input impedances at both input x_n and x_p ports and high equivalent impedance at the output port z due to the used source followers with local feedback.

The paper is organized as follows: The description of DCCII, its new CMOS implementation, two all-pass filter (APF) examples including non-ideal analysis are presented in Section II. The presented filter circuits employ grounded capacitors for easy integrated circuit (IC) implementation and they are also cascadable. Experimental and simulation results are given in Section III to verify the operation of the voltage-mode (VM) APF. Finally, conclusions are given in Section IV.

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II. CIRCUIT DESCRIPTION

A. The DCCII and its New CMOS Implementation

The circuit symbol of the DCCII is given in Fig. 1. The current flowing through *z* port is the difference of currents flowing into x_n and x_p ports. The voltage of the high-impedance *y* port is copied to both x_n and x_p ports with unity gain. Using standard notation, port relations of an ideal DCCII can be described by the following hybrid matrix:

$$\begin{bmatrix} v_{xn} \\ v_{xp} \\ i_z \\ i_y \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 \\ 0 & 0 & 1 \\ 1 & -1 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{xn} \\ i_{xp} \\ v_y \end{bmatrix}. \tag{1}$$

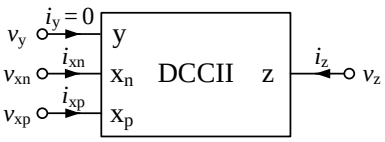

Fig. 1. Circuit symbol of the DCCII.

The novel CMOS structure of the proposed DCCII, which is given in Fig. 2, is based on class AB translinear loop input stage formed by transistors M_1–M_4, while CS and current mirror stages are consist of transistors M_{11}–M_{17}, M_{19}, and M_{18}, M_{20}–M_{24}, respectively. Transistors M_6, M_7 and M_9, M_{10} have equal currents and both pairs serve as DC current sources for the translinear loop. Transistor pair M_2 and M_{11} forms the source follower with local feedback so-called super source follower (SSF) to obtain very small equivalent resistance at port x_n with other SSF pair M_4 and M_{12}. Other SSF pairs of transistors M_{14}, M_{17} and M_{15}, M_{19} are used to obtain very small equivalent resistance at port x_p. Current mirror pairs M_{21}, M_{18} and M_{24}, M_{20} are used to obtain the difference current at output port *z*.

The equivalent resistance seen on port *y* of class AB input stage is equal to

$$R_y = \left(\frac{1}{g_{m1}} + r_{o9}\right) \Big\| \left(\frac{1}{g_{m3}} + r_{o6}\right), \tag{2}$$

where g_{mk} and r_{ok} are transconductance and output resistance of *k*-th MOS transistor, respectively. The equivalent resistance seen on ports x_n and x_p are equal to [25]:

$$R_{xn} = \frac{1}{g_{m11}\left(1+g_{m2}r_{o2}\right)} \Big\| \frac{1}{g_{m12}\left(1+g_{m4}r_{o4}\right)}, \tag{3}$$

$$R_{xp} = \frac{1}{g_{m17}\left(1+g_{m14}r_{o14}\right)} \Big\| \frac{1}{g_{m19}\left(1+g_{m15}r_{o15}\right)}. \tag{4}$$

Finally, the equivalent resistance seen on port *z* can be calculated simply as

$$R_z \cong \frac{r_{18}r_{20}}{r_{18}+r_{20}}, \tag{5}$$

hence, from output resistance of transistors M_{18} and M_{20}.

B. Proposed All-Pass Filter Circuits

As application example for the proposed DCCII, two new first-order APF circuits shown in Fig. 3 are also introduced. Assuming ideal DCCII described by (1) and resistor matching $R_2 = R_3 = 2R_1 = 2R$, transfer functions (TFs) of presented APFs can be expressed as follows:

$$T_{VM}(s) = \frac{V_{out}}{V_{in}} = -\frac{sCR-1}{sCR+1}, \tag{6}$$

$$T_{CM}(s) = \frac{I_{out}}{I_{in}} = \frac{sCR-1}{sCR+1}. \tag{7}$$

Phase response of the TFs (6) and (7) is calculated as:

$$\varphi_{VM}(\omega) = -2\tan^{-1}(\omega CR), \tag{8}$$

$$\varphi_{CM}(\omega) = 180° - 2\tan^{-1}(\omega CR), \tag{9}$$

hence, the VM and CM APFs provide phase shifting between 0 (at $\omega = 0$) to $-\pi$ (at $\omega = \infty$) and π (at $\omega = 0$) to 0 (at $\omega = \infty$), respectively. Moreover, the pole (ω_p) and zero (ω_z) frequencies from TFs can be expressed as

$$\omega_p = \omega_z = \frac{1}{CR}. \tag{10}$$

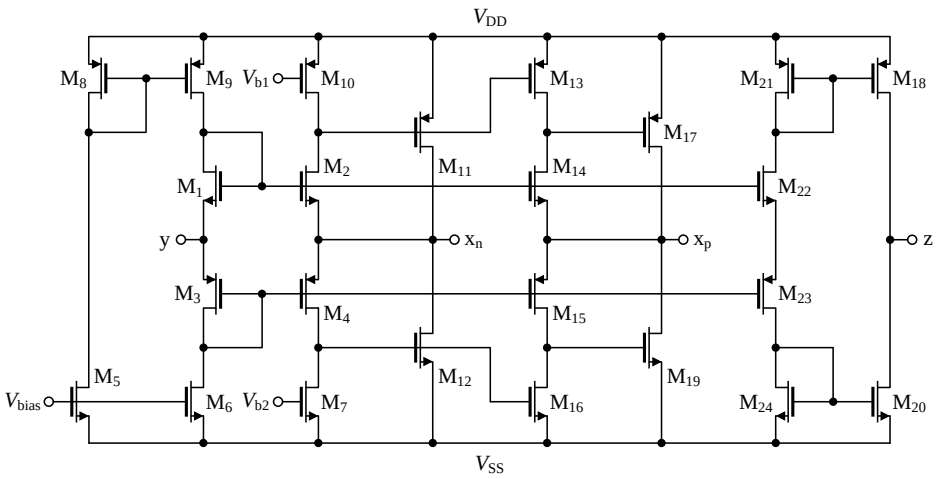

Fig. 2. The proposed high performance CMOS DCCII.

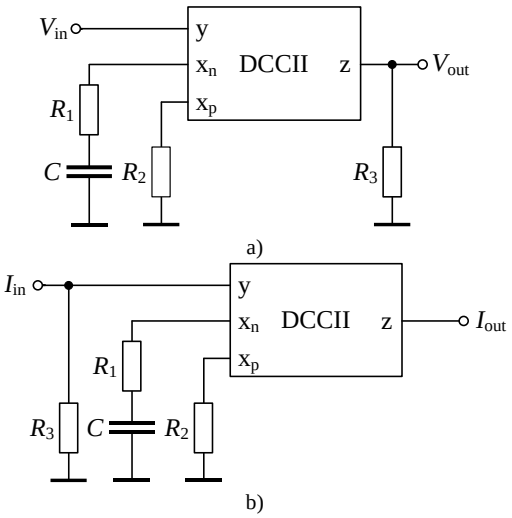

Fig. 3. First-order (a) voltage-mode and (b) current-mode AP filters.

Hence, their sensitivities to passive elements are unity in relative amplitude. The proposed VM APF in Fig. 3(a) has high input impedance and CM circuit in Fig. 3(b) has high output impedance. Hence, both proposed APFs have the advantage of being cascadable, *i.e.* there will be no need for additional voltage buffer or current follower in case of their connection into a voltage- or current-mode signal processing channel, respectively.

C. Non-Ideal Analysis

Considering the non-idealities caused by the physical implementation of the DCCII, its port relations can be described by the following hybrid matrix:

$$\begin{bmatrix} v_{xn} \\ v_{xp} \\ i_z \\ i_y \end{bmatrix} = \begin{bmatrix} 0 & 0 & \beta_n(s) \\ 0 & 0 & \beta_p(s) \\ \alpha_p(s) & -\alpha_n(s) & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{xn} \\ i_{xp} \\ v_y \end{bmatrix}. \quad (11)$$

Here the frequency-dependent non-ideal current gains $\alpha_j(s)$ and voltage gains $\beta_j(s)$ for $j = \{p, n\}$ are ideally equal to unity. Note that, using a single-pole model, they can be defined as:

$$\alpha_j(s) = \frac{\alpha_{oj}}{1 + s\tau_{\alpha_j}}, \quad (12)$$

$$\beta_j(s) = \frac{\beta_{oj}}{1 + s\tau_{\beta_j}}, \quad (13)$$

where α_{oj} and β_{oj} are DC current and voltage gains of the DCCII, respectively. The bandwidths $1/\tau_{\alpha j}$ and $1/\tau_{\beta j}$ depend on the fabrication of the DCCII and on the order of a few Grad/s frequency range in current technologies are ideally equal to infinity. However, at low and medium frequencies *i.e.*, $f \ll (1/(2\pi)) \times \min\{1/\tau_{\alpha j}, 1/\tau_{\beta j}\}$, (12) and (13) turn to $\alpha_j(s) \cong \alpha_{oj} = 1 - \varepsilon_{\alpha ij}$ and $\beta_j(s) \cong \beta_{oj} = 1 - \varepsilon_{\beta vj}$. Here, $\varepsilon_{\alpha ij}$ and $\varepsilon_{\beta vj}$ denote the current and voltage tracking errors whereas $|\varepsilon_{\alpha ij}| \ll 1$ and $|\varepsilon_{\beta vj}| \ll 1$.

Taking into account non-idealities of the DCCII and reanalysing the behaviour of the proposed APFs in Fig. 3, TFs in (6) and (7) convert to

$$T'_{VM}(s) = -T'_{CM}(s) = \\ = -\alpha_{on}\frac{R_3}{R_2} \times \left[\frac{sC\left(\alpha_{op}\beta_{on}R_2 - \beta_{op}R_1\right) - \beta_{op}}{sCR_1 + 1} \right], \quad (14)$$

from which it can be seen that the pole ω_p and zero ω_z frequencies differ and can be given as:

$$\omega'_p = \frac{1}{CR_1}, \quad (15)$$

$$\omega'_z = \frac{\beta_{op}}{C\left(\alpha_{op}\beta_{on}R_2 - \beta_{op}R_1\right)}. \quad (16)$$

Note that the effect of non-ideal gains can be minimized by precision design of DCCII, *i.e.* making current and voltage gains very close to unity.

III. PERFORMANCE VERIFICATIONS

A. Simulation Results

To verify the theoretical studies, the proposed CMOS DCCII implementation shown in Fig. 2 is simulated with HSpice simulation program using AMS 0.35 µm CMOS real process parameters. The aspect ratios of CMOS transistors are listed in Table I. The supply voltages are $V_{DD} = -V_{SS} = 1.25$ V and the biasing voltage sources are set to be $V_{bias} = -0.36$ V, $V_{b1} = 0.24$ V, and $V_{b2} = -0.39$ V.

TABLE I. ASPECT RATIOS OF CMOS TRANSISTORS IN THE DCCII.

Transistor	W/L (µm/µm)
M_1, M_2, M_{14}, M_{22}	50/0.5
M_3, M_4, M_{15}, M_{23}	150/0.5
M_5–M_7, M_{12}, M_{16}, M_{19}, M_{24}	5/0.5
M_8–M_{11}, M_{13}, M_{17}, M_{21}	15/0.5
M_{18}	30/0.5
M_{20}	10/0.5

First of all, the behaviour of the proposed CMOS DCCII was evaluated via AC and transient analyses. The simulation results of the impedance magnitudes on ports x_n, x_p, and z are given in Fig. 4.

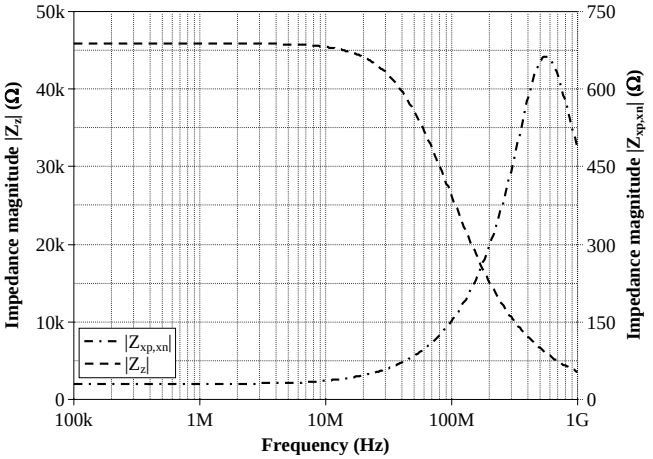

Fig. 4. The impedance magnitudes at x_n, x_p, and z ports.

Obtained resistance values for both x_n and x_p input ports are 30.4 Ω. Note that it is significantly lower than in previously introduced CMOS DCCII structures available in [11]–[14], which *x* port resistances are more than 100 Ω.

The resistance value of *z* port is obtained as 45.9 kΩ, which is sufficiently high. The AC current transfer characteristic is depicted in Fig. 5. The current transfer ratios α_p and α_n are equal to 0.998 and their bandwidths are 325 MHz. The parasitic capacitance appearing between the high-impedance *z* output port and ground has a value 10.2 fF. Similarly, the voltage transfer ratios β_p and β_n are equal to 0.965 and their bandwidths are 330 MHz. The impedance and parasitic capacitance appearing between high-impedance input *y* port and ground are equal to 84 kΩ and 18 fF, respectively. The power consumption of the DCCII is 1.3 mW. Time-domain analyses of the proposed DCCII are also performed. A 1 MHz sinusoidal input current with amplitude of 200 µA peak-to-peak and a 2 MHz pulse input current with amplitude of 200 µA peak-to-peak are applied to x_p and x_n ports, respectively. The performed time-domain simulation esults are illustrated in Fig. 6.

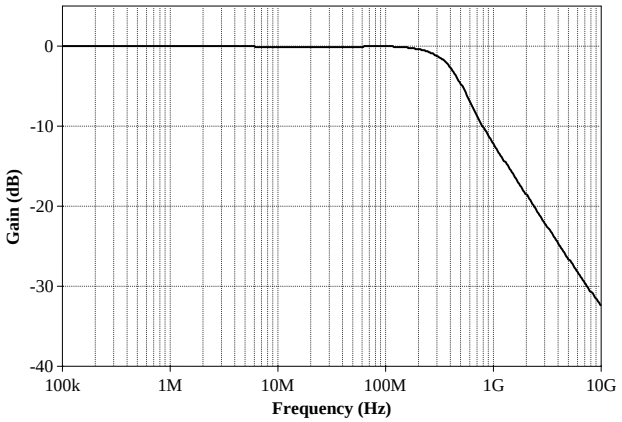

Fig. 5. AC transfer characteristic of current transfers α_p and α_n of the proposed DCCII implementation.

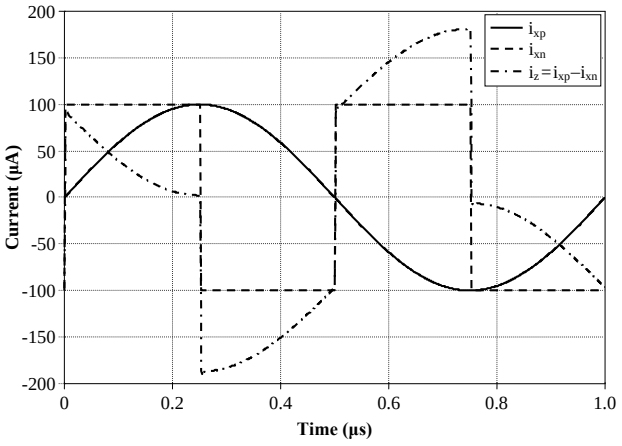

Fig. 6. Time-domain simulation results for sinusoidal input current at x_p port and pulse input current at x_n port and their difference.

In order to verify the workability of the proposed VM APF shown in Fig. 3(a), it was simulated using the proposed CMOS DCCII in Fig. 2. Passive element values are chosen as R_1 = 1 kΩ, $R_2 = R_3$ = 2 kΩ, and C = 500 pF to obtain a phase shift of 90° at pole frequency of f_p = 320 kHz. AC simulation results, *i.e.* ideal and simulated phase and gain responses of the filter are given in Fig. 7. As it can be seen the gain response of the proposed VM APF at f_p is unity and there is also no deviation in phase compared to theory.

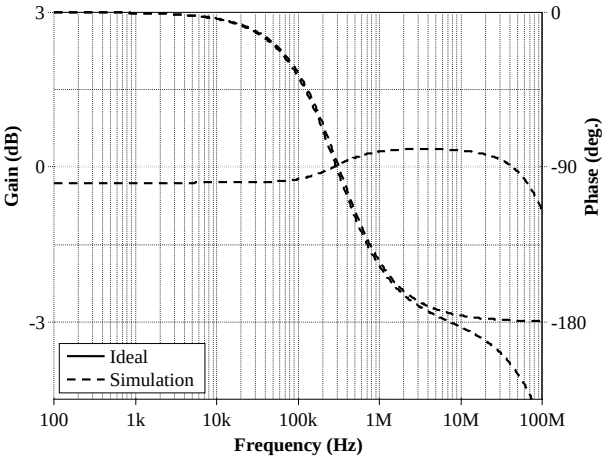

Fig. 7. Ideal and simulated gain and phase responses of the VM first-order AP filter.

B. Measurement Results

Secondly, in order to confirm the theoretical results and examine the proposed VM APF circuit in more detail, its behavior has also been verified by experimental measurements. The circuit in Fig. 3(a) with a pole frequency of $f_p \cong 250$ kHz has been designed with resistor values of R_1 = 0.5 kΩ, $R_2 = R_3$ = 1 kΩ, and capacitor C = 1.3 nF. The DCCII has been realized using two commercially available AD844 ICs of Analog Devices with ±12 V supply voltages [26], as it is shown in Fig. 8. The theoretical and experimental results of the gain and phase responses are depicted in Fig. 9.

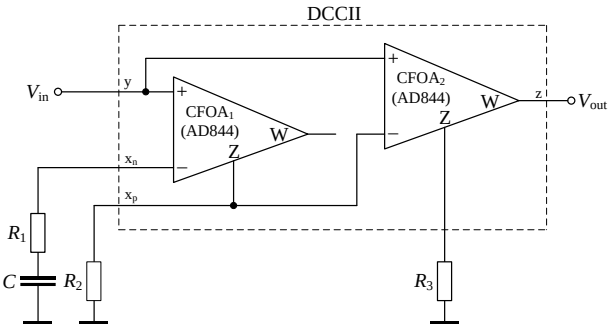

Fig. 8. Realization of the proposed VM APF employing single DCCII via two AD844 ICs for the experiments.

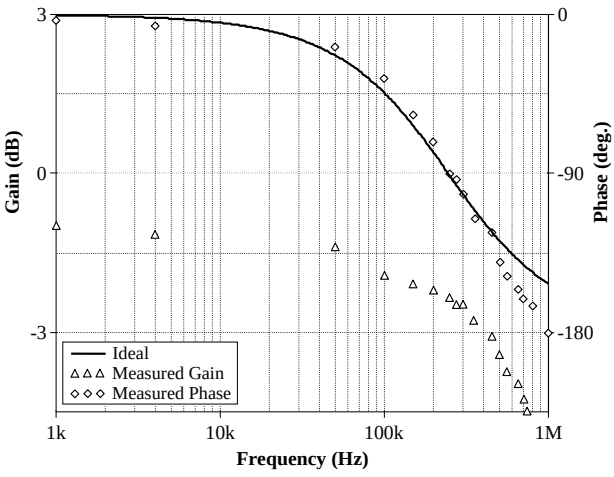

Fig. 9. Experimental phase and gain responses of the proposed VM APF.

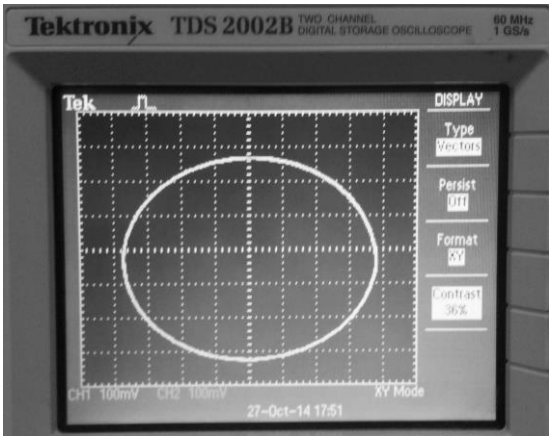

Fig. 10. The photograph of the experimental result for Lissajous pattern at the pole frequency (horizontal and vertical scales are 0.1 V/div.).

Note that at high frequencies the deviations in gain and phase characteristics are affected by the poles of voltage and current gains as well as by the external terminal parasitics of the readily available ICs. Moreover, according to datasheets, the passive element tolerances of selected discrete components are 2 % and 5 %, which may also affect the precision of f_p. In addition, in order to investigate the phase relationship between input and output signals, input and output signals have been applied to the oscilloscope in X-Y mode. The photograph of the experimental result for Lissajous pattern at the f_p is shown in Fig. 10. From the obtained results it can be seen that the proposed solution is in good agreement with the theory.

IV. CONCLUSIONS

In this paper, a new high performance CMOS DCCII is investigated. The proposed circuit has low equivalent input impedances on ports x_n and x_p and high impedance values on ports y and z. As an application example current- and voltage-mode first-order all-pass filters are presented. These circuits have a grounded capacitor for easy IC implementation. Operation of these circuits is verified by computed simulations via HSpice software and by experiments.

REFERENCES

[1] K. C. Smith, A. Sedra, "The current conveyor—A new circuit building block", in *Proc. IEEE*, vol. 56, no. 8, pp. 1368–1369, 1968. [Online]. Available: http://dx.doi.org/10.1109/ PROC.1968.6591

[2] G. Palmisano, G. Palumbo, S. Pennisi, *CMOS Current Amplifiers*. Kluwer Academic Publishers, 1999. [Online]. Available: https://doi.org/10.1007/978-1-4615-5135-5

[3] Y.–S. Hwang, D.–S. Wu, J.–J. Chen, C.–C. Shih, W.–S. Chou, "Design of current-mode MOSFET-C filters using OTRAs", *Int. Journal of Circuit Theory and Applications*, vol. 37, no. 3, pp. 397–411, 2009. [Online]. Available: http://dx.doi.org/ 10.1002/cta.477

[4] R. Senani, D. R. Bhaskar, A. K. Singh, *Current Conveyors: Variants, Applications and Hardware Implementations*. Springer International Publishing, Switzerland, 2015. [Online]. Available: https://doi.org/10.1007/978-3-319-08684-2

[5] F. Lin, P.–I. Mak, R. P. Martins, "Wideband receivers: design challenges, tradeoffs and state-of-the-art", *IEEE Circuits and Systems Magazine*, vol. 15, no. 1, pp. 12–24, 2015. [Online]. Available: http://dx.doi.org/10.1109/MCAS.2014.2385571

[6] D. Biolek, R. Senani, V. Biolkova, Z. Kolka, "Active elements for analog signal processing: classification, review, and new proposals", *Radioengineering*, vol. 17, no. 4, pp. 15–32, 2008.

[7] D. Prasad, D. R. Bhaskar, A. K. Singh, "New grounded and floating simulated inductance circuits using current differencing transconductance amplifiers", *Radioengineering*, vol. 19, no. 1, pp. 194–198, 2010.

[8] A. U. Keskin, E. Hancioglu, "CDBA-based synthetic floating inductance circuits with electronic tuning properties", *ETRI Journal*, vol. 27, no. 2, pp. 239–242, 2005. [Online]. Available: http://dx.doi.org/10.4218/etrij.05.0204.0055

[9] M. Atasoyu, B. Metin, H. Kuntman, N. Herencsar, "New current-mode class 1 frequency-agile filter for multi protocol GPS application", *Elektronika ir Elektrotechnika*, vol. 21, no. 5, pp. 35–39, 2015. [Online]. Available: http://dx.doi.org/10.5755/ j01.eee.21.5.13323

[10] E. Tlelo-Cuautle, *Integrated Circuits for Analog Signal Processing*. Springer-Verlag: New York, 2013. [Online]. Available: https://doi.org/10.1007/978-1-4614-1383-7

[11] H. O. Elwan, A. M. Soliman, "A CMOS differential current conveyor and applications for analog VLSI", *Analog Integrated Circuits and Signal Processing*, vol. 11, no. 1, pp. 35–45, 1996. [Online]. Available: http://dx.doi.org/10.1007/BF00174237

[12] S. Ciftcioglu, H. Kuntman, A. Zeki, "New high performance CMOS differential current conveyor realization", in *Proc. 4th Int. Conf. Electrical and Electronics Engineering (ELECO)*, Bursa, Turkey, 2005, pp. 68–71.

[13] B. Metin, "Canonical inductor simulators with grounded capacitors using DCCII", *Int. Journal of Electronics*, vol. 99, no. 7, pp. 1027–1035, 2012. [Online]. Available: http://dx.doi.org/10.1080/ 00207217.2011.639274

[14] B. Metin, N. Herencsar, K. Vrba "A CMOS DCCII with a grounded capacitor based cascadable all-pass filter application", *Radioengineering*, vol. 21, no. 2, pp. 718–724, 2012.

[15] S. Shahsavari, S. Biabanifard, S. M. H. Largani, O. Hashemipour, "DCCII based frequency compensation method for three stage amplifiers", *AEU – Int. Journal of Electronics and Communications*, vol. 69, no. 1, pp. 176–181, 2015. [Online]. Available: http://dx.doi.org/10.1016/j.aeue.2014.08.011

[16] A. Toker, S. Ozoguz, O. Cicekoglu, C. Acar, "Current-mode all-pass filters using current differencing buffered amplifier and a new high-Q bandpass filter configuration", *IEEE Trans. Circuits and Systems–II*, vol. 47, no. 9, pp. 949–954, 2000. [Online]. Available: http://dx.doi.org/10.1109/82.868465

[17] A. K. Kafrawy, A. M. Soliman, "A modified CMOS differential operational transresistance amplifier (OTRA)", *AEU – Int. Journal of Electronics and Communications*, vol. 63, no. 12, pp. 1067–1071, 2009. [Online]. Available: http://dx.doi.org/10.1016/j.aeue.2008. 08.003

[18] E. Arslan, S. Minaei, A. Morgul, "On the realization of high performance current conveyors and their applications", *Journal of Circuits, Systems, and Computers*, vol. 22, no. 3, 2013. [Online]. Available: http://dx.doi.org/10.1142/ S0218126613500151

[19] S. Minaei, O. Cicekoglu, D. Biolek, N. Herencsar, J. Koton, "Guest editorial: A special issue on low-voltage low-power analog devices and their applications", *Radioengineering*, vol. 22, no. 2, pp. 413–414, 2013.

[20] W. Tangsrirat, K. Klahan, T. Dumawipata, W. Surakampontorn, "Low-voltage NMOS-based current differencing buffered amplifier and its application to current-mode ladder filter design", *Int. Journal of Electronics*, vol. 93, no. 11, pp. 777–791, 2006. [Online]. Available: http://dx.doi.org/10.1080/00207210600711556

[21] F. Kacar, H. H. Kuntman, "A new, improved CMOS realization of CDTA and its filter applications", *Turkish Journal of Electrical Engineering and Computer Sciences*, vol. 19, no. 4, pp. 631–642, 2011. [Online]. Available: http://dx.doi.org/10.3906/elk-1003-467

[22] C. Cakir, S. Minaei, O. Cicekoglu, "Low-voltage low-power CMOS current differencing buffered amplifier", *Analog Integrated Circuits and Signal Processing*, vol. 62, no. 2, pp. 237–244, 2010. [Online]. Available: http://dx.doi.org/10.1007/s10470-009-9350-6

[23] O. G. Sokmen, H. Ercan, S. A. Tekin, M. Alci, "A novel low voltage low power OTA based on level shifter current mirror", *Elektronika ir Elektrotechnika*, vol. 21, no. 2, pp. 39–43, 2015. [Online]. Available: http://dx.doi.org/10.5755/j01.eee.21.2.115011

[24] C. W. Lin, Y. H. Wu, S. F. Lin, "A precise current subtractor design", in *Proc. Int. Conf. Circuits, System and Simulation*, IPCSIT Press, vol. 7, 2011, pp. 82–86.

[25] E. Arslan, "Self-biasing high precision CMOS current subtractor for current-mode circuits", *Advances in Electrical and Computer Engineering*, vol. 13, no. 4, pp. 19–24, 2013. [Online]. Available: http://dx.doi.org/10.4316/AECE.2013.04004

[26] AD844/AD: 60 MHz, 2000 V/μs Monolithic Op-Amp, 2009. [Online] Available at: http://www.analog.com/media/en/technical-documentation/data-sheets/AD844.pdf