

Design of Novel MSK Architectures Using R-F Bit

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Abstract—In this paper, we present two novel reformulations (1) and (20) for MSK (Minimum Shift Keying) modulation technique. By using these novel reformulations, we find an additional switching bit, referred to as R-F bit, and propose a novel MSK architecture. Compared to known prior MSK architectures, our architecture offers significant advantages with respect to power consumption and hardware efficiency. Additionally, a pre-computation technique is used to reduce ram bit utilization (RBU) of the proposed modulator. Considering the whole modulation procedure, this approach reduces the RBU of the proposed architecture by 75%. The experimental results show that our architecture is very suitable for MSK modulation.

Index Terms—R-F bit; pre-computation; MSK; FPGA; NCO.

I. INTRODUCTION

Communication systems develop each passing day and provide the end user broadband transmission. Due to increasing demands, higher data sharing and decrease of power consumption are expected from wireless communication systems [1]. Moreover, the type of modulation technique used also affects these problems [2]. MSK modulation technique is one of the modulation techniques mostly preferred today in MIMO-OFDM systems, 802.15.4 standard, optical and satellite communication due to its high spectral efficiency [3]–[5].

There are two common types of MSK modulator architecture: conventional I-Q parallel MSK, serial MSK. The serial MSK approach was first proposed in [6] to avoid time synchronization of the conventional MSK and minimize the system complexity, and it was provided by using BPSK modulator and bandpass filter. In another paper, serial MSK architecture was designed by considering VCO (voltage controlled oscillator), which can be defined as analog NCO (Numerically Controlled Oscillator) [7]. The VCO-based MSK structure is a fundamental reference for NCO architectures. One of the comprehensive papers offered various NCO structures, such as Cordic-based and ROM-based architectures, for digital modulations [8]. By using these architectures, many NCO-based on MSK structures were proposed in the literature. Authors in [9] utilized

trigonometric functions based Xilinx IP core for minimum resource utilization while ROM-based NCO architectures were designed in [10] and [11].

Due to spectral efficiency of MSK, different architectures were proposed in the literature. To provide energy efficiency, CMOS based MSK was carried out for biomedical applications [12], [13]. In the paper [14] which proposes a different parallel MSK architecture, the combination of FPGA and integrated circuits was presented, and time synchronization and attenuation of the blocks were shown to be very crucial. Moreover, MSK has gained significant attention in the field of optical communication in recent years [4], [15], [16]. The paper [16] uses conventional I-Q MSK modulator while phase modulation based on MSK modulator is presented in [15]. We show that the electrical equivalent of phase modulation-based MSK uses too many samples in the ROM. In [17], FPGA-based binary modulation techniques are designed by executing a NCO block. In order to generate signal with modulation, ROM block stores 256 samples with 16 bits per sample. Therefore, the number of stored bits is 4096 for BASK (Binary Amplitude Shift Keying) and BPSK (Binary Phase Shift Keying) which are among of the simplest modulation techniques. Due to usage of two NCO, the number of bits is equal to $4096 \times 2 = 8192$ for BFSK (Binary Frequency Shift Keying).

The NCO-block was used in many FPGA-based MSK architectures. However, NCO has disadvantages as follows:

1. The change of parameters, such as phase angle resolution, can increase or decrease output pin number of the modulator and sample stored in ROM [10], [17]. It is very important in respect of resource utilization since the number of ram bit is calculated by using the number of output pin and sample.
2. Each NCO consists of phase increment value because same sample repeatedly can be stored in ROM [10] or the change of phase increment value is required to generate signal with different frequencies. However, megacore NCO in Quartus differently works to minimize the number of ram bit as mentioned in Section IV.
3. Output pin bit number can only set from 10 bit to 32 bits in megacore NCO. To observe MSK signal, a specific DAC can be necessary or output pin number can be

decreased by using a division block. The first raises cost and may decrease data rate due to conversion rate of DAC with high bit while second increases resource utilization and may decrease maximum operating frequency of the system.

In this paper, we propose a mux-based architecture, referred to as R-F MSK. Thanks to the proposed structure, the resource utilization is decreased significantly compared to the conventional architecture and NCO based structures. In order to design mux-based architecture, we comprehensively analyze MSK signal at phase transition points by using $g(t)$ pulse signal. Then, we observe two novel reformulations. By using these reformulations, we obtain R-F MSK architecture. In order to further decrease RBU, we propose pre-computation technique for the R-F MSK architecture. Additionally, we prove that the architecture is practicable by observing experimental results.

A. Statement of the Problem

If data bit number is expressed by n in mux based architectures, the signal number can be expressed by 2^n . For instance, while BPSK, BASK and BFSK signals are consisting of 2 different conditions, the number of information bit is 1. Thus, there are some problems in the constitution of this architecture for MSK modulator. The most significant one among these problems is the number of information bit being two despite the formation of MSK signal from eight different signals. Namely, MSK is a signal covering four different phase conditions and two different frequency conditions. Because in mux based architectures, information bits are applied to the selector pin input of the mux block, and thus it is intended to activate the proper signal among the signals applied to data input of mux block. Thus, as the MSK signal consists of eight different signals, it is required for the selector pin bit number of the mux block to be three. Accordingly, the generation of the required third bit (R-F bit) was ensured by using two different mathematical equations (1) and (20) derived in this study.

II. PROPOSED MSK MODULATOR

The R-F architecture has been designed according to the rise and fall condition of I and Q channel weighting signals. The concept of rise is the change of signal from 0 to $\pm V_{max}$. The fall is defined as a decrease of the signal from $\pm V_{max}$ to 0 as considering the opposite of the previous concept. To explain this status, a $g(t)$ pulse (half period sine) is described in Fig. 1.

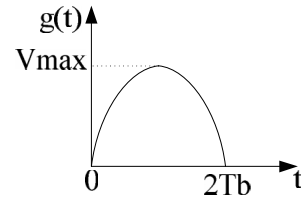


Fig. 1. $g(t)$ pulse.

When Fig. 1 is examined, it is assumed that the magnitude of signal is $V_{max} = 1$ at peak value (at the moment of T_b), and that it is 0 at the moment of $2T_b$ or 0. The change as per time of conventional MSK architecture realized considering the $g(t)$ pulse structure in the figure has been provided in Fig. 2. In Fig. 2, R-F bit forming the basis of R-F MSK architecture is also being seen.

In Fig. 2, data and encoded data bits are shown by using non-italic and italic symbols, respectively. In order to obtain the encoded data bits, the even bits of I channel and Q channel are passed through the not operation. The first bit of data and encoded data bits indicate I channel bit just as the second bit of data and encoded data bits signify Q channel bit. Moreover, R-F bits are represented by using the double quotation marks. The results shown in the Fig. 2 are obtained by using conventional MSK architecture which was defined in [11]. If the figure is examined, ISP, QCP, IFMO, QFMO, ISMO, and QSMO represent weighting signals of I channel and Q channel, output of first multiplication of I and Q channel, output of second multiplication of I and Q channel, respectively.

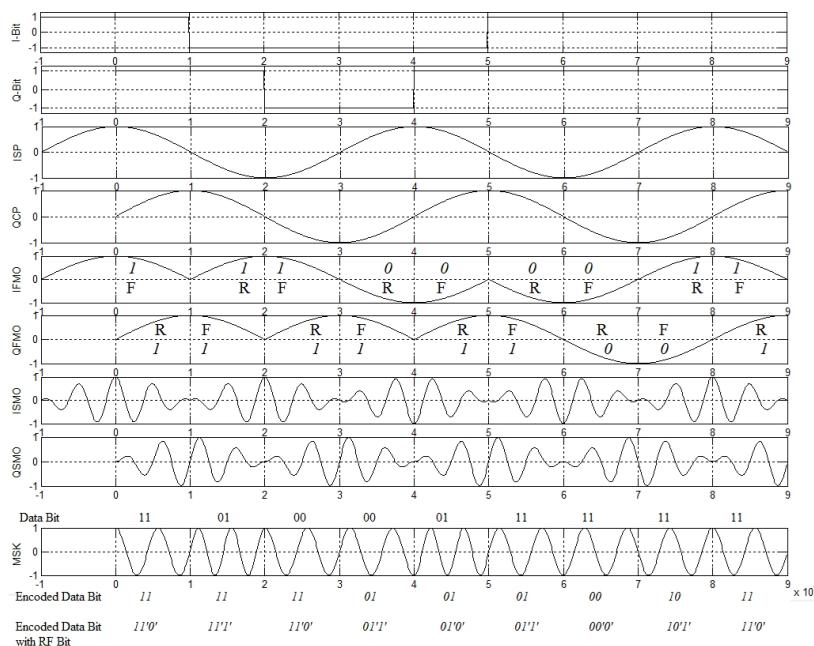


Fig. 2. MSK architecture with R-F bit.

In Fig. 2, if attention is paid, despite receipt of 11 information signals for four times at the 0.5 μs and 0.9 μs time intervals, the phases of the four signals are different from each other. Moreover, if the R-F bits proposed at these time intervals are considered, the generated signals are expressed two times by 110 bits and two times by 111 bits. The coding operation is realized to eliminate this problem. When the coded bits are considered, the signals changing at 0.5 μs and 0.9 μs time intervals can be defined as 011, 000, 101 and 110 respectively. Moreover, the correctness of the claim is revealed that signals at time intervals of 0.3 μs –0.4 μs and 0.5 μs –0.6 μs have the same phase and frequency with each other.

A. Instant Phase Analysis of Proposed MSK Technique

The R-F architecture had been designed according to the rise and fall condition of I and Q channel weighting signals. In our equations, the even bits of information bits are passed through the NRZ (Not Return to Zero) block after passing through the not operation. Finally, information bits are formed into I_k and Q_k . For the $0 \leq q < 1$ and $y, x \in \{0,1\}$, we see that:

$$\phi_k = \frac{\pi}{2}(2+q-I_k)(1-y) + \frac{\pi}{2}(q+1-Q_k)y, \quad (1)$$

$$k \equiv x \pmod{2}, \quad (2)$$

$$y = 1 - x, \quad (3)$$

where ϕ_k is phase value of k -th MSK signal and $k=1,2,3,\dots$. The k -th MSK signal is $(k-1)T_b/2 \leq t \leq kT_b/2$. T_b is the symbol width. In Fig. 2, we assume that k is 1 between 0 μs and 0.1 μs . As seen from (3), y variable gets the values of 1 or 0 as per the bit –to be transmitted- being odd or even. As specified before, a third bit is required in order to constitute a mux based architecture. The third bit come up depending on the y variable as seen from (1) derived in this study.

Proff: In the following equations, all I_k and Q_k represent ± 1 and are coded as explained in Fig. 2. The MSK signal is defined as follows:

$$MSK(t) = I_k g(t) \cos(2\pi f_c t) + Q_k g(t - \frac{\pi}{2}) \sin(2\pi f_c t), \quad (4)$$

$$MSK(t) = I_k \sin\left(\frac{\pi t}{2T_b}\right) \cos(2\pi f_c t) + Q_k \sin\left(\frac{\pi t}{2T_b} - \frac{\pi}{2}\right) \sin(2\pi f_c t). \quad (5)$$

Conditions: There are two conditions: odd k , even $(k-1)$ and even k , odd $k-1$.

Condition 1.1: Of a new equation is written for the odd k values.

When one of the $g(t)$ or $g(t - \pi/2)$ is 1, the other signal is becoming 0. For $t = kT_b$ and odd k numbers, they are 1 and 0, respectively. The $g(t)$ signal reaches the peak value at the moment of kT_b , and the signals multiplied by this signal thus multiplied by 1. Then, MSK signal can be expressed as:

$$MSK(kT_b) = I_k \cos(2\pi f_c kT_b), \quad (6)$$

$$MSK(kT_b) = \cos(2\pi f_c kT_b + \frac{\pi}{2}(1-I_k)), \quad (7)$$

$$MSK(kT_b) = \cos(2\pi f_c kT_b + \frac{\pi}{2}|I_k - 1|). \quad (8)$$

For the $(k-1)$ even numbers, MSK signal at the moment of $(k-1)T_b$ is derived from (5) to be:

$$MSK((k-1)T_b) = Q_{k-1} \sin(2\pi f_c (k-1)T_b), \quad (9)$$

$$MSK((k-1)T_b) = \cos(2\pi f_c (k-1)T_b - \frac{\pi}{2} + \frac{\pi}{2}|Q_{k-1} - 1|). \quad (10)$$

If the final form of (8) and (10) are examined, it is shown that there is a 90 degree phase difference in between these two signals. This condition does not change according to the I_k and Q_k variables having the same or different values. To prove it, we can be defined as:

$$\frac{\pi}{2}|(I_k - 1)| = -\frac{\pi}{2} + \frac{\pi}{2}|Q_{k-1} - 1| + \phi_i, \quad (11)$$

$$\phi_i = \frac{\pi}{2} + \frac{\pi}{2}|I_k - Q_{k-1}|, \quad (12)$$

where ϕ_i indicates the phase difference in between the previous and next signals.

Condition 1.2: Of a new equation is written for the even k values, and MSK signal can be defined as:

$$MSK(kT_b) = Q_k \sin(2\pi f_c kT_b) = Q_k \cos(2\pi f_c kT_b - \frac{\pi}{2}), \quad (13)$$

$$MSK(kT_b) = \cos(2\pi f_c kT_b - \frac{\pi}{2} + \frac{\pi}{2}(|Q_k - 1|)). \quad (14)$$

For odd $(k-1)$ values, the phase of the previous signal can be expressed as:

$$MSK((k-1)T_b) = I_{k-1} \cos(2\pi f_c (k-1)T_b), \quad (15)$$

$$MSK((k-1)T_b) = \cos(2\pi f_c (k-1)T_b + \frac{\pi}{2}(|1 - I_{k-1}|)). \quad (16)$$

It is required to have a phase difference of 90 degrees in between the signals obtained in (14) and (16). To ensure it, ϕ_i is calculated as:

$$\frac{\pi}{2}(|1 - I_{k-1}|) + \phi_i = -\frac{\pi}{2} + \frac{\pi}{2}(|1 - Q_k|), \quad (17)$$

$$\phi_i = -\frac{\pi}{2} + \frac{\pi}{2}(|I_{k-1} - Q_k|). \quad (18)$$

As seen in the (12) and (18), the phase difference in between the two signals depends on the Q channel bit at that moment and previous I channel bit, or on the I channel bit at that moment and previous Q channel bit. As the result of these equations, we write that:

$$\phi_k = \phi_{k-1} + \phi_i, \quad (19)$$

$$\phi_k = \phi_{k-1} + \frac{\pi}{2}(-1)^{k+1} + \frac{\pi}{2}(|I_k - Q_{k-1}|)(1-y) + \frac{\pi}{2}(|Q_k - I_{k-1}|)(y), \quad (20)$$

where φ_{k-1} and φ_k indicate the phases of the previous signal and the signal at that moment, respectively. Equation (20) provides the relationship between previous (φ_{k-1}) and moment (φ_k) phase.

In order to prove (1), we must use (20). Next, we continue the discussion of two cases:

Condition 2.1: For odd k values, y takes 0.

We substitute y into (1), we obtain the final form of the (1) as follows

$$\phi_k = (2 + q - I_k) \frac{\pi}{2}. \quad (21)$$

By substituting y into (20), we have

$$\phi_k = \phi_{k-1} + \frac{\pi}{2} + \frac{\pi}{2} (|I_k - Q_{k-1}|). \quad (22)$$

Then, re-write φ_k in (21) based on (22) as

$$(2 + q - I_k) \frac{\pi}{2} = \phi_{k-1} + \frac{\pi}{2} + \frac{\pi}{2} (|I_k - Q_{k-1}|). \quad (23)$$

The $(k-1)$ value becomes even, and the phase of the signal at that moment can be calculated by substituting $(k-1)$ into (1). Then, y gets 1. From (1), we get

$$\phi_{k-1} = \frac{\pi}{2} (n+1 - Q_{k-1}). \quad (24)$$

Therefore, from (23) and (24), we can get

$$(2 + q - I_k) \frac{\pi}{2} = \frac{\pi}{2} (q+1 - Q_{k-1}) + \frac{\pi}{2} + \frac{\pi}{2} (|I_k - Q_{k-1}|). \quad (25)$$

According to (25), the (1) had provided the phrase in (20).

Condition 2.2: For the even values of k variable,

The y variable takes the value of 1. We can write φ_k as

$$\phi_k = \frac{\pi}{2} (q+1 - Q_k). \quad (26)$$

From definition (20), φ_k and φ_{k-1} given by

$$\phi_k = \phi_{k-1} - \frac{\pi}{2} + \frac{\pi}{2} (|Q_k - I_{k-1}|). \quad (27)$$

By substituting (26) in (27), we have

$$\frac{\pi}{2} (q+1 - Q_k) = \phi_{k-1} - \frac{\pi}{2} + \frac{\pi}{2} (|Q_k - I_{k-1}|). \quad (28)$$

In order to prove (28), we must calculate φ_{k-1} for $(k-1)$ odd numbers. Therefore, φ_{k-1} in (1) can be rewritten as

$$\phi_{k-1} = (2 + q - I_{k-1}) \frac{\pi}{2}. \quad (29)$$

Then, we can rewrite (28) as

$$\frac{\pi}{2} (q+1 - Q_k) = (2 + q - I_{k-1}) \frac{\pi}{2} - \frac{\pi}{2} + \frac{\pi}{2} (|Q_k - I_{k-1}|). \quad (30)$$

The left and right sides of (23) and (30) take the same

values for appropriate q values. This statement proves the accuracy of (1).

B. Frequency Analysis of Proposed MSK Technique

After the realization of the phase analysis of the MSK signal, it is required to perform its frequency analysis. We analyzed frequency status as per R-F bit. In Fig. 3, $g(t)$ and $g(t-T_b)$ pulse series and their definition are given.

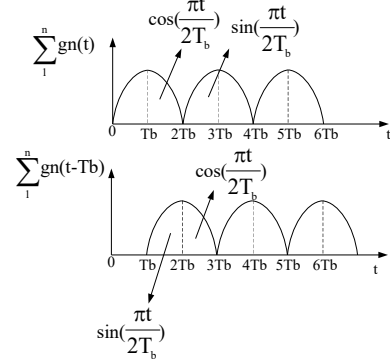


Fig. 3. Change of $g(t)$ and $g(t-T_b)$ signals as per time.

Condition-3.1: For odd k values and $T_b \leq t \leq 2T_b$ interval

The y and R-F bit take 0. Then, MSK signal can be defined as:

$$\begin{aligned} MSK(t) = & I_k \left(\sum_l^n g_n(t) \right) \cos(2\pi f_c t) + \\ & + Q_k \left(\sum_l^n g_n(t - \frac{\pi}{2}) \right) \sin(2\pi f_c t), \end{aligned} \quad (31)$$

$$\begin{aligned} MSK(t) = & I_k \cos\left(\frac{\pi t}{2T_b}\right) \cos(2\pi f_c t) + \\ & + Q_k \sin\left(\frac{\pi t}{2T_b}\right) \sin(2\pi f_c t) = \cos\left(2\pi f_c t \mp \frac{\pi t}{2T_b}\right). \end{aligned} \quad (32)$$

From (32), the frequency of MSK signal is expressed as follows:

$$\begin{cases} f_1 = f_- = f_c - \frac{1}{4T_b}, \\ f_2 = f_+ = f_c + \frac{1}{4T_b}. \end{cases} \quad (33)$$

From which we can see that the frequency changes with I_k and Q_k . The frequency is f_1 if I_k and Q_k are same. Otherwise, the frequency value is f_2 .

Condition 3.2: For even k values and $2T_b \leq t \leq 3T_b$ interval

In this condition, I channel will be multiplied by sine function and Q channel will be multiplied by cosine function at this time interval as shown in Fig. 3. The y and R-F bit take 1. Therefore, we can get the MSK signal as:

$$\begin{aligned} MSK(t) = & I_k \sin\left(\frac{\pi t}{2T_b}\right) \cos(2\pi f_c t) + \\ & + Q_k \cos\left(\frac{\pi t}{2T_b}\right) \sin(2\pi f_c t), \end{aligned} \quad (34)$$

$$MSK(t) = \sin(2\pi f_c t \pm \frac{\pi t}{2T_b}), \quad (35)$$

$$\begin{cases} f_1 = f_- = f_c + \frac{1}{4T_b}, \\ f_2 = f_+ = f_c - \frac{1}{4T_b}. \end{cases} \quad (36)$$

From (35) and (36), we can see that the frequency is f_1 for different values of I_k and Q_k . In the other case, the frequency of MSK signal is f_2 . Therefore, we assert that the *Condition 3.1* and *Condition 3.2* are opposite to each other.

III. HARDWARE ARCHITECTURES OF R-F MSK MODULATOR

In this section, we present the hardware architectures of the reformulated R-F MSK modulators. Based on the proposed reformulations, we can obtain 8 cases in Table I. From the table, we demonstrate that phase and frequency of the MSK signal depend on the Encoded I (E-I), Q (E-Q), and R-F bits. The Fig. 4 illustrates the architecture of the R-F MSK. In this figure, bit separator acts as serial to parallel block; while counter provides address control of the ROM block. As shown in the figure, R-F MSK is completely the same compared with the binary transmission techniques [17]. The ROMs, each of which uses 56×8 and 72×8 bits for generation of two carrier signals with different frequencies, store digital signals with phase $P = P_a$ and frequency $F = F_b$. Depending on E-I, E-Q and R-F bits, the mux provides generation of MSK signal by selecting the output of one of the ROM blocks. In order to reduce the number of stored bits, we use one ROM block of which memory size is $72 \times 8 + 56 \times 8 = 1024$ bits.

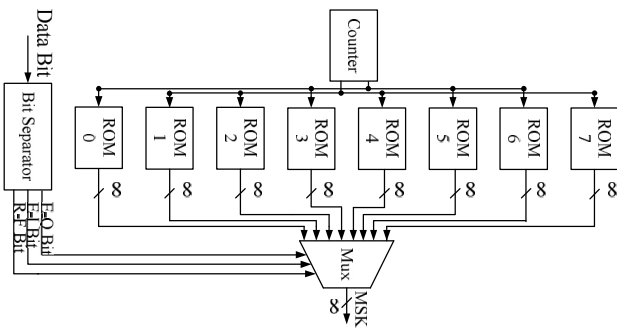


Fig. 4. R-F MSK technique.

Compared with the R-F MSK, this PCRF MSK architecture given in Fig. 5(a) determines phase or frequency of the signal at the beginning of the modulation process by using a pre-computation technique, and it reduces the number of stored samples by 75 %. In the figure, C-1...C-8 represent constant values, y and x are 72 and 127, respectively. Compare with our proposed architectures, and we design some NCO-based MSK architectures by using Small-Rom (S-NCO), Large-Rom (L-NCO), Cordic (C-NCO) and Multiplier (M-NCO) of Quartus. They are alternative architectures in respect of resource utilization.

The SPCRF MSK architecture shown in Fig. 5(c) only stores 45 degrees of the sine waveform like as S-NCO MSK. Compared with PCRF MSK, SPCRF MSK reduces RBU by

25 %. However, it needs more LUTs and register than that of R-F and PCRF MSK. The Inv block executes to obtain negative samples by converting 2's complement form while the Reg block provides synchronization of input signals of the mux. Due to only storing of positive samples and 45 degrees of the sine waveform, C-_{FL}, C-_{FH}, Alternance-f high and low are required for forward and backward counting of the counter block and selecting of alternance. E-I, E-Q, and R-F bits are passed through XOR gates to select frequency of the MSK. This case can be seen from Table I.

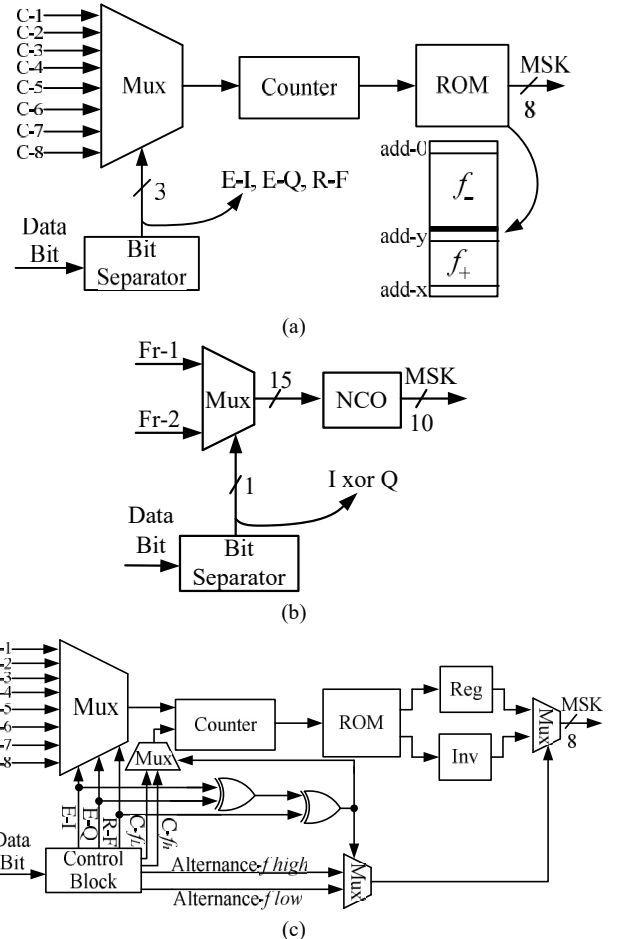


Fig. 5. Precomputation R-F MSK (PCRF MSK) (a); (S, L, C, M)-NCO based MSK (b); Small-Rom Precomputation R-F MSK (S-PC-R-F MSK) (c).

TABLE I. CHANGE OF THE FREQUENCY AND PHASE OF MSK SIGNAL.

R-F Bit	E-I and E-Q bits	Phase and Frequency of MSK Signal	R-F Bit	E-I and E-Q bits	Phase and Frequency of MSK Signal
0	11	$P_1; F_1$	0	10	$P_1; F_2$
0	01	$P_3; F_2$	1	00	$P_4; F_2$
1	01	$P_2; F_1$	0	00	$P_3; F_1$
1	11	$P_2; F_2$	1	10	$P_4; F_1$

IV. RESULTS OF EXPERIMENTAL AND SIMULATION

Several MSK modulator examples are synthesized and mapped on EP4CE22F17C6 FPGA to demonstrate the efficiency of the proposed R-F MSK architectures. We design C-MSK (Conventional MSK), Parallel MSK (P-MSK) and NCO-MSK structures on Quartus to compare architectures since we couldn't find with a comparable implementation study. In order to compare the number of

ram bit, $F_0 = 72$ samples per cycle are used in all implementations without NCO [10]. The synthesis results are summarized in Table II. As shown in the table, the worst resolution is belonging to NCO-MSK [10] although it utilizes more ram bits. This is due to repeatedly writing of samples with same amplitude to the ROM. A similar work is achieved to design BASK, BPSK and BFSK techniques [17]. In the study, RBU is equal to 4096 for BASK and BPSK while it is 8192 for BFSK due to the use of two NCO blocks. However, the authors invert to output of NCO instead of 2's complement like as our architectures as mentioned in Fig. 5(c) to generate BPSK.

We design RPCRF MSK without using ROM block to compare with C-NCO MSK. Then, we store samples into our designed block instead of ROM block of Quartus. To explain results in the table, we group architectures with regard to their design aim such as decreasing of utilization of LUTs or ram bits, and give several remarks as follows: First, we see that the proposed R-F MSK structures utilize fewer resources-especially LUTs and registers resources-while providing approximately equal maximum operating frequency. Second, the lower memory bit usage of our MSK architectures is explained by the fact that our architectures utilize addresses of the ROMs more efficient than that of the other structures. Additionally, NCO-MSK structures (L, C, S and M NCO) in Quartus set RBU or utilization of LUTs and register per changing the parameters. Third, PCRf MSK uses fewer RAM bit and LUT than R-F MSK since the pre-computation technique assists to bring down RBU. The counter shown in Fig. 5 consumes more LUT than the counter shown in Fig. 4. However, LUT utilization is decreased by moving the MUX block before the counter. Fourth, one of the best results is achieved by designing RPCRF MSK structure. Compared with Cordic NCO (C-NCO), it saves LUTs and registers by up to approximately 75 % and 90 %, respectively. In addition, RPCRF consumes 3 times lower power than C-NCO.

Although NCO [10] achieves higher LUT utilization efficiency compared with PCRf and L-NCO, it is clearly shown that the PCRf can save ~20 % and ~40 % energy without performance loss, as compared to NCO [10] and L-NCO, respectively. In addition, L-NCO utilizes more 3 times LUTs and registers than the PCRf.

SPCRf and S-NCO are similar in respect of ram bit

utilization. However, the SPCRf is more successful 50 % with regard to power consumption. The maximum operating frequency of the S-NCO is higher that of the SPCRf.

In Table III, it is given that parameter values of NCO block are selected by us. We select these values according to SNPC (Number of Sample Per Cycle) and output frequency.

TABLE III. PARAMETER VALUES OF NCO.

Parameter	Value of Parameter	Parameter	Value of Parameter
Phase Accumulator Precision	15	Clock Rate	72 MHz
Angular Resolution	7	Desired Frequencies	1-1.25 MHz
Magnitude Precision	10	Real Output Frequencies	0.9997 MHz–2.2502 MHz

Figure 6 shows RBU of different MSK implementations with a $F_0 = 72$, provided that each sample only is used for one time per a period. For L-NCO architecture, the number of the sample stored in ROM is taken as 2^M to minimize RBU. Therefore, the size of ROMs depends on $\log_2(F_0) = M_x$. M_x , which is defined as angular resolution, is calculated by rounding off M_x up to the next integer. For example, when $F_0 = 72$, M_x takes approximately 6.17. Hence, $M = 7$ is used for 72 samples and the number of samples stored in ROM must be 2^7 . Bit length should be at least 10 bits in NCO of Quartus to represent each amplitude sample. Hence, overall the number of ram bit takes $128 \times 10 = 1280$. Due to storing of 45 degrees of the sine waveform, RBU of S-NCO can be calculated as follows: $(2^M) \times 0.25 \times (MP-1)$. In order to obtain the RBU of M-NCO, we re-compile M-NCO architecture at each stage which is shown in Fig. 6. For our architectures, we could use 7 bits to represent 72 or 56 samples; however, we ignore this case and utilize more 1 bit to represent each sample. Moreover, we could non-uniform quantizer but we didn't utilize it to obtain impartial results.

Figure 7 and Fig. 8 show experimental results for the proposed architecture. From these figures, we can see the change of E-I and E-Q bits as per MSK signal. The data bits are 1100011111 while the coded bits are 1111010011. In the figures, the period of the one symbol is 2 μ s. Our clock frequency is selected 126 MHz and our frequencies are 1.75 MHz and 2.25 MHz. As seen in the figures, modulated signal was obtained successfully.

TABLE II. COMPILATION REPORT FOR MSK MODULATOR ARCHITECTURES.

Design	PCRf	L-NCO	NCO [10]	RPCRF	C-NCO	SPCRf	S-NCO	R-F	C [16]	P [15]	M-NCO
LUTs	180	450	162*	256*	1109	286*	536	187*	257	296	569
Reg.	105*	297	113	105*	941	168*	374	99*	163	136	402
Bits	1024*	1280	6144	N/A	N/A	256*	288	4096*	8010	4608	400
Mult.	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	2	N/A	4
f (Mhz)	125.99*	124.86	113.97	115.61	115.34	101.03	111.94*	112.87	106.12	112.21	113.31
F_0	72	72	8	72	72	72	72	72	72	72	72
$P_{dynamic}$ [mW]	13*	22	16	13*	42	16*	25	16*	33	20	27

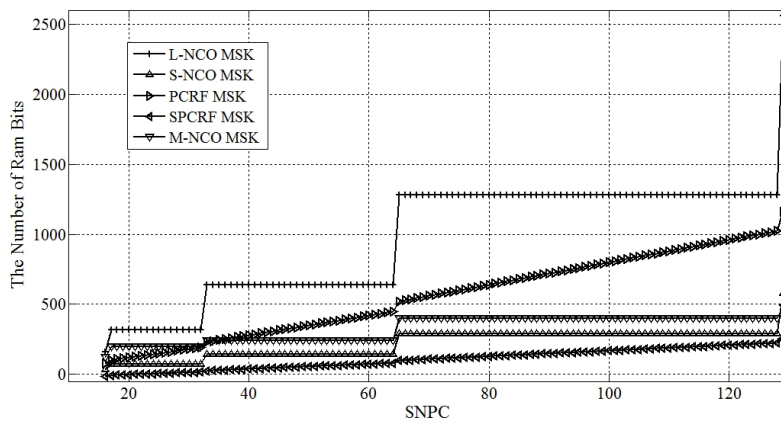


Fig. 6. RBU as per SNPC.

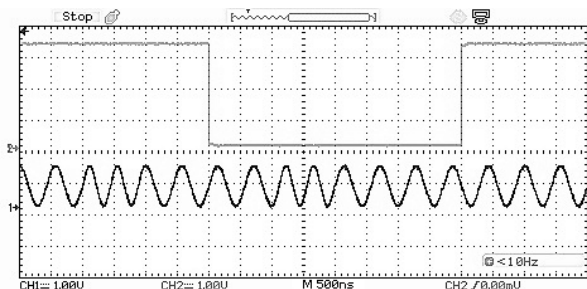


Fig. 7. E-I channel bit and PCRF MSK signal.

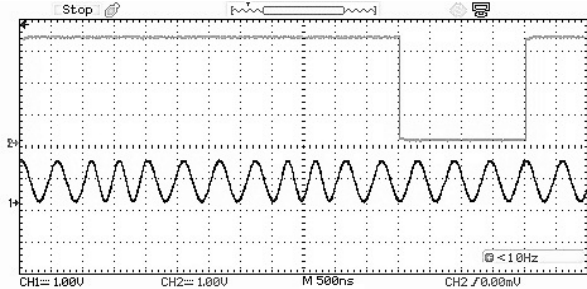


Fig. 8. E-Q channel bit and PCRF MSK signal.

V. CONCLUSIONS

In this paper, the novel reformulations (1) and (20) for the implementation of FPGA-based MSK modulator are proposed. It is being observed from the results of compilation that the proposed R-F MSK architecture has significant advantages in respect of power consumption and hardware efficiency. The resource utilization is further reduced by using pre-computation technique. Additionally, we show that our proposed architecture is practicable.

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