

Serial-Parallel IGBT Connection Method Based on Overvoltage Measurement

Lubos Streit^{1,2}, Dusan Janik^{1,2}, Jakub Talla¹

¹Regional Innovation Centre for Electrical Engineering, University of West Bohemia, Univerzitni 8, Pilsen 306 14, Czech Republic

²Department of Electromechanics and Power Electronics, University of West Bohemia, Univerzitni 8, Pilsen 306 14, Czech Republic
lloyd@rice.zcu.cz

Abstract—This paper deals with a novel method which allows the serial connection of Insulated Gate Bipolar Transistors (IGBTs). The different dynamic characteristics of serially connected IGBTs during turn ON and OFF cause a short-term overvoltage stress in the transistors. In contrary to the commonly used techniques, the presented method reduces additional commutation losses by actively correcting turn ON and OFF delays. The presented method uses overvoltages as measured by a peak detector. The correction circuit doesn't require a high speed Analog-Digital converter (ADC) or high speed computation.

The target power switch unit consists of two serial connected transistors with two identical parallel branches. The well-known 2-level inverter topology equipped with the power switch unit can be connected directly to the high-voltage grid. This converter topology was demanded by our industry partner for 11 MW mining machines. The paper contains a laboratory experiment conducted on a serial-parallel IGBT power switch unit with a tested output power of 1 kW.

Index Terms—Power semiconductor switches, insulated gate bipolar transistors, driver circuits, digital signal processors, field programmable gate arrays.

I. INTRODUCTION

Actual voltage, along with the physical limits of the current of semiconductor power switches, lead to serial and parallel connection of power components or whole power converters in high power applications (*e.g.* STATCOM [1], HVAC and HVDC). This paper describes a possible variant of the implementation of the serial-parallel IGBT switch. It is a power unit with two parallel transistors connected in series to the other two parallel transistors (see Fig. 1).

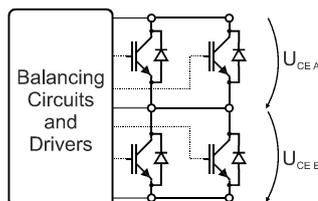


Fig. 1. Serial-Parallel IGBT switch.

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The derating (oversizing) is the most commonly used method for parallel connecting of IGBTs. This method is supplemented by symmetric output wires and selecting IGBTs with characteristics as similar to each other as possible. Symmetric output wires of IGBTs mean a special mechanical arrangement, which ensures uniform current distribution in parallel conductors (conductors of the same length and shape). A positive temperature coefficient of IGBTs also contributes to correct current distribution. A more detailed description of the parallel connection is described in [2]. Examples of IGBT behaviours during turn ON and OFF are described in [3].

Connecting IGBTs serially is more difficult than connecting them parallelly. A fast turn ON of the first transistor leads to the second one suffering an overvoltage stress. This could cause a rapid destruction of stressed transistors. To ensure correct switching, there are several methods that compensate for the different dynamic behaviour of IGBTs. The presented principle is based on the active compensation of different turn ON and turn OFF times of serially connected IGBTs.

A combination of different methods is usually used in serially connected IGBTs. The presented method is complementary to other IGBT voltage balancing methods: RC or RCD (Resistor, Capacitor, Diode) snubber [4]–[6], active clamping [7], [8] and is analogous to the presented one in [9]. These methods allow the function of the serially connected IGBTs but with an increase in commutation losses. The presented method compensates for different delays of serially connected IGBTs and thus enables a reduction of losses in other balance circuits. The power converter efficiency can also be additionally increased by using the soft-switching methods described in [10].

II. PRINCIPLE OF OVERVOLTAGE DETECTION AND IGBT DELAY COMPENSATION

The principle of the presented balancing method involves measuring the overvoltage caused by different turn ON and turn OFF times of serially connected IGBTs. A block diagram of the prototype is shown in Fig. 2. The overvoltage can't be measured directly by an ADC because the duration of the overvoltage is very short ($10 \times \text{ns}$). Therefore a peak detector is used to capture these short pulses. It holds the captured peak voltage value until it is read by the ADC.

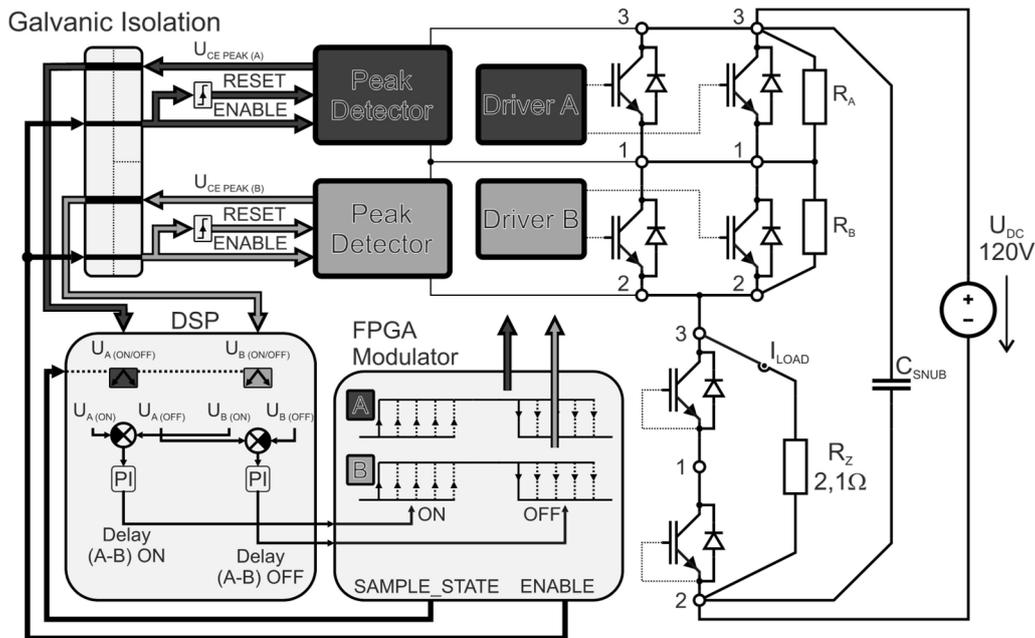


Fig. 2. Functional block diagram of Serial-Parallel IGBT unit of power 1 kW.

A peak detector is used to capture overvoltages during both turn ON and turn OFF. The implemented software in Digital Signal Processor (DSP) then decides which overvoltage was measured (turn ON or turn OFF). Furthermore, the DSP calculates the control deviation from overvoltages on both transistors (as at turn ON $U_B(ON) - U_A(ON)$ as at turn OFF $U_A(OFF) - U_B(OFF)$). The resulted error signal is the input of PI (Proportional-Integral) controllers, whose outputs are the relative delay between transistor A and transistor B (one for turn ON and one for turn OFF). These delays are entered to the modulator implemented in Field-Programmable Gate Array (FPGA). The FPGA modulator allows delaying the turn ON and turn OFF edges of the control signal with step 5 ns. The minimal step is determined by the maximal allowable frequency due to the longest critical signal path of the FPGA. Delayed control signals control IGBT transistors via IGBT drivers. Parallel transistors are controlled by the same output signal of the driver; each transistor has only its own Gate resistor $R_G = 10 \Omega$. The value of the gate resistor was chosen as relatively high in order to obtain more visible differences between transistors. The other outputs of the FPGA are control signals for the peak detector: ENABLE and SAMPLE_STATE, because the FPGA modulator generates the PWM signal.

ENABLE and SAMPLE_STATE signal generation is explained in Fig. 3. The ENABLE signal activates a peak

detector for detecting peaks (Collector Emitter overvoltage $U_{CE PEAK}$). A rising edge of this signal also resets the peak detector (erasing previously captured overvoltage).

A falling edge of the ENABLE signal starts the ADC's conversion (SOC Start Of Conversion). The ADC has enough time to convert until the next rising edge appears for the signal ENABLE. The ADC therefore reads the overvoltage during turn ON and the subsequent pulse of the ENABLE signal triggers another detection but with the result of the turn OFF. The detection of both overvoltages is therefore carried out during two periods.

This procedure was chosen because of the relatively long conversion time of the ADC compared with a minimum Pulse Width Modulation (PWM). In the PWM's case, close to 0 %, or 100 %, the time between overvoltage during turn ON and turn OFF is very short.

From the described principle it is evident that this is not a method that would balance transistor voltages in the current switching period. As was mentioned in Section I, this method is complementary to loss-making methods of balancing (active clamping, RCD snubber). Therefore, it is imperative to effectively balance the voltage of the transistors immediately for the first switch. The transistors are protected by the supplementary methods. After several periods the delay differences in IGBTs are already compensated for, and thereby the losses caused by the complementary balancing methods are reduced.

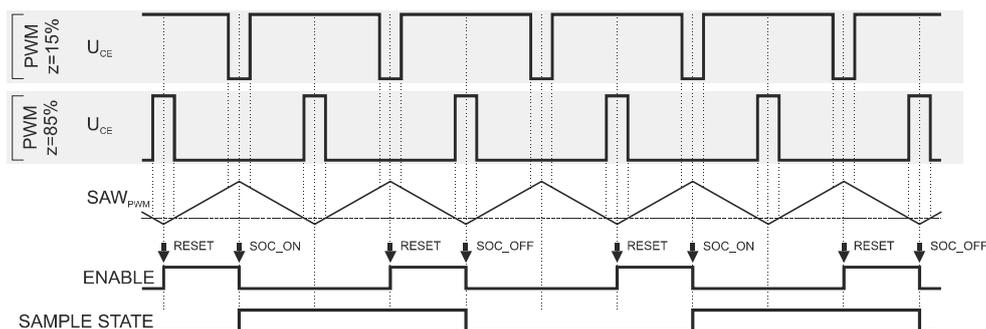


Fig. 3. Diagram showing the timing of peak detector overvoltage measurement and AD conversion.

III. TESTING CIRCUIT DESIGN

The testing prototype of output power 1 kW (at switching frequency 10 kHz and PWM 40 %) was constructed to verify the method. A half bridge module package was used as a serial arrangement of transistors. Transistors are already connected in series in the package. Their common connection was used only for parallel connection with another module and voltage measurement U_{CE} . The IGBT Module of serial-connected transistors is Semikron SKM50GB12T4 (two modules were used for parallel connecting).

A freewheeling diode module was formed by Semikron SKM75GB12V, whose control gates were short-circuited ($U_{GE} = 0$). Balancing during the steady state in off transistors was ensured by resistors R_A and R_B of the value 27 k . The switching power supply Chroma 61504 ensures the DC voltage of the value 120 V. The control algorithm was implemented in DSP TMS320F28335. A master control unit is shown in Fig. 4. Fig. 5 is a photo of the assembled serial-parallel IGBT unit.

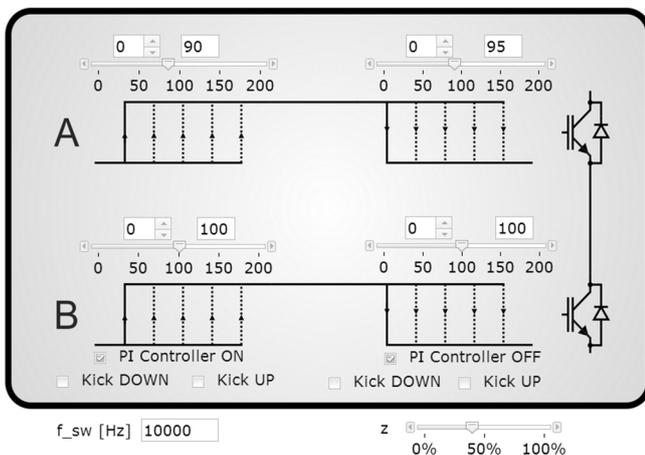


Fig. 4. Master control unit implemented in Code Composer Studio 5.5.

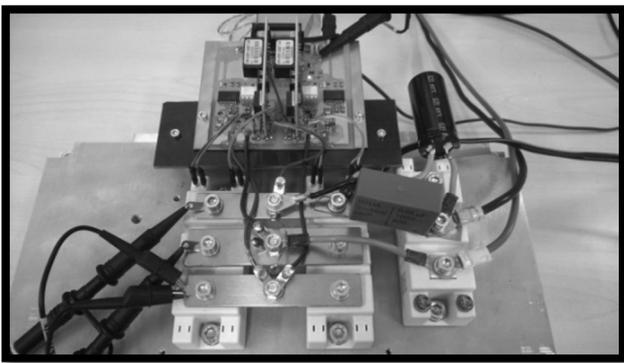


Fig. 5. Testing prototype of Serial-Parallel IGBT unit of power 1 kW.

The testing prototype isn't equipped by the balancing complementary circuits (active clamping, RCD snubber); this makes for a more noticeable effect of the presented method, including a demonstration of the voltage distribution in uncompensated delays of IGBT transistors. For this reason a lower voltage (120 V) than the blocking voltage of the transistors (1200 V) was chosen. The overvoltage detection circuit consists of two peak detectors (for transistor A and B), the galvanic isolation of the control signals ENABLE and SAMPLE_STATE and galvanic isolation between the analog values of detected peaks (again

for both channels A and B).

IV. MEASUREMENT

After the first functionality test of the serial-parallel unit, several measurements were executed. These measurements showed the expected function of delay compensation. The waveforms listed first during incorrect compensation of delays are listed in the following subsections IV.A and IV.B. As was mentioned above, the supply voltage for the test did not reach the maximum capability of the IGBTs. Therefore the consequences of an unbalanced transistor's voltage could be demonstrated without its destruction.

The subsection IV.C already demonstrates the presented method of the IGBT delay compensation. The following settings were applied for all measurements:

- CH1 voltage of the transistor A (T_A) U_{CEA} 20 V/div;
- CH2 voltage of the transistor B (T_B) U_{CEB} 20 V/div;
- CH4 current of the load I_{LOAD} 20 A/div;
- Time base 400 ns/div (IV.A, IV.C) 10 μ s/div (IV.B).

Conclusions of measurements are valid for all expectable switching frequencies (approximately up to 20 kHz) and for the full range of the PWM. The duty cycle of PWM, close to 0 % or 100 %, causes difficulties due to insufficient time for capturing the overvoltage (see Fig. 3). If these conditions persist only in a few PWM periods, PI controllers will not change the output delays significantly. In case of long duration of duty cycle close to 0 % or 100 % other balancing method (RCD snubber, active clamp) will balance the voltage with losses. Using this method for voltage higher than 120 V requires changing the sense voltage divider of peak detectors and balancing resistors (R_A , R_B). It will also be necessary to ensure greater resistance to interference whose levels will increase with increasing voltage (power).

A. Forced Imbalance during Turn ON

This subsection demonstrates the impact of incorrect voltage distribution on different delays during turn ON. One of the transistors was delayed intentionally by 100 ns. Figure 6(a) shows transistor A's delay. Figure 6(b) shows transistor B's delay. The DC voltage is equally divided into both transistors' voltages before turn ON. After 100 ns both transistors were opened and their voltages were equal to the saturation voltage. The overvoltage of the transistors during imbalanced voltages reaches 116 % of the DC voltage. This can lead to the transistors' destruction.

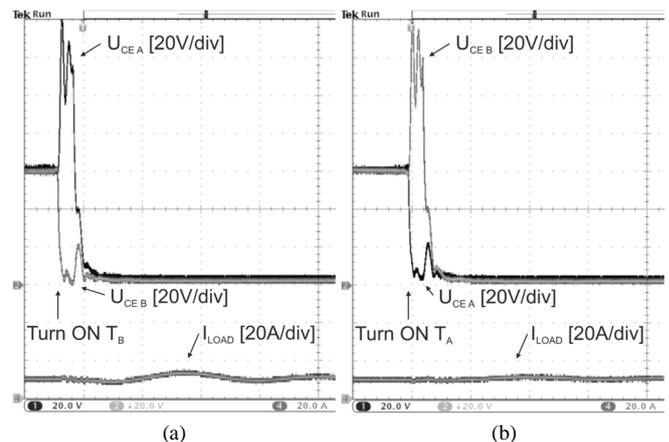


Fig. 6. Turn ON overvoltage (Timebase 400 ns/div): a) transistor A delayed 100 ns; b) transistor B delayed 100 ns.

B. Forced Imbalance during Turn OFF

This subsection demonstrates the impact of incorrect voltage distribution on different delays during the turn OFF. Again, one of the transistors was intentionally delayed by 100 ns during turn OFF. Figure 7 shows the delay of both transistor A and B. Both transistors were opened before turn OFF, therefore their voltages U_{CE} was equal to saturation voltage. The transistors' voltages were going to be equally divided due to balancing resistor R_A and R_B after turn OFF. The overvoltage on transistors during imbalanced voltages reaches 133 % of the DC voltage. This too can destroy the transistors.

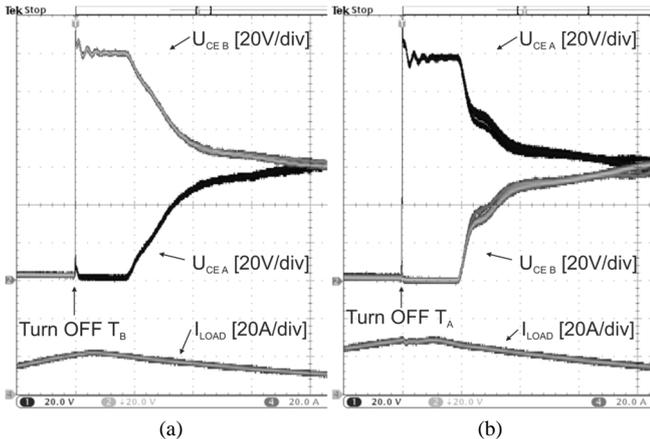


Fig. 7. Turn ON overvoltage (Timebase 10 μ s/div): a) transistor A delayed 100 ns; b) transistor B delayed 100 ns.

C. Balancing due to IGBT Delay Compensation

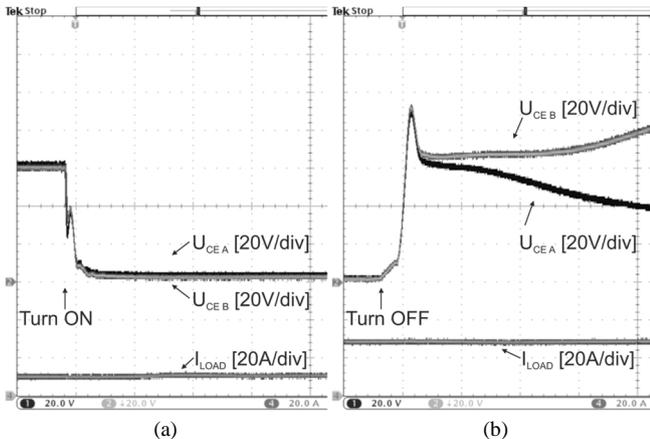


Fig. 8. Voltage division with delay compensation (Timebase 400 ns/div): a) during turn ON; b) during turn OFF.

This subsection demonstrates how the presented method compensates for the delay of IGBT. The oscillograms in Fig. 8(a) and Fig. 8(b) show the voltage distribution in transistors during turn ON and turn OFF. The voltage division is balanced during turn ON. During turn OFF the voltage is also divided equally, but unbalance occurs after the dynamic behaviour disappears. This unbalanced voltage is then balanced by resistors R_A , R_B . Overvoltages of these occurrences are comparable. The overvoltage during delay compensation is only 80 % of the DC voltage.

V. CONCLUSIONS

This paper presents a novel method for the serial connection of IGBTs. The different dynamic characteristics of serially connected IGBTs during turn ON and OFF cause short-term overvoltage stress of transistors. The presented method uses a peak detector to capture overvoltages for enough time to enable conversion by a common ADC.

The DSP measures overvoltages and defines required delays using PI controller computation. Output delays are generated by FPGA with a minimal delay step of 5 ns. In order to apply this method at nominal power (for a voltage supply higher than the blocking voltage of one transistor), it is necessary to supplement the serial-parallel unit with auxiliary balancing methods that protect semiconductor devices until the PI controllers finish balancing the voltage in the transistors.

Another improvement of the balancing control process is the reduction of step delay (less than 5 ns). It can be expected that a high current will unbalance the voltage in transistors more significantly during the same delays.

The proper function of the presented method was demonstrated on a 1 kW testing prototype. The final application of the presented method will be the 11 MW mining machine.

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