ELECTRONICS AND ELECTRICAL ENGINEERING
ISSN 1392 – 1215 2007. No. 6(78)
ELEKTRONIKA IR ELEKTROTECHNIKA

AUTOMATION, ROBOTICS
T125
AUTOMATIZAVIMAS, ROBOTECHNIKA

Transistor Control with Additional Charge Pumping Circuit

V. Augutis, D. Gailius, D. Styra
Department of Electronics and Measurements Systems, Kaunas University of Technology,
Studentų st. 50-445, LT-51368 Kaunas, Lithuania, phone: +370 37 45 16 17, e–mail: darius.styra@ktu.lt
A. Dumčius
Department of Electronics Engineering, Kaunas University of Technology,
Studentų st. 50-142, LT-51368 Kaunas, Lithuania, phone: +370 37 300520, e–mail: antanas.dumcius@ktu.lt

Introduction

At the output stages of modern horizontal deflection generators (HDG) bipolar transistors (BT) are used most often, which have typical high nominal collector voltages (1500-1700 V). Switching characteristics of such BT are related to the base excitation conditions. It is possible to reduce losses in the transistor during switching process by optimizing these conditions [1]. In HDG the MOSFET (Metal Oxide Semiconductor Field Effect Transistor) and IGBT (Insulated Gate Bipolar Transistor) type transistors are used, but the allowable maximal operating voltage of modern MOSFET type transistors is not sufficient.

The newest IGBT type transistors would be suitable for HDG according to allowable operating voltage and power, but the sufficient reduction of switching connection process losses is problematic, since they are strongly related to the magnitude of the switched current during optimization the gate control due to peculiarities of its characteristics.

Since BT switch-off characteristics are influenced by the basis excitation conditions, therefore switching losses can be reduced by optimizing the base excitation conditions.

When comparing the operation of BT, MOSFET and IGBT in HDG, it was found that it is most beneficial to use BT [2].

It was found that these specific operating conditions are characteristic to the transistor of each output stage model [2], [3]:

- Total base excitation current, especially at the end of I_b line;
- The shape of the base excitation current signal (rise, peak, decline (drop);
- The rate of base excitation current decline during switch-off.

Most of efforts were made in order to optimize the shape and amplitude of the base excitation current. The problem consists in the dispersion of amplification coefficient values of high-power BT. It is also influenced by the dispersions of the values of other parameters, but they are more easily eliminated.

The structure of horizontal deflection module is shown in Fig. 1.

The problem becomes even more intricate if it is needed to implement the possibility for a rapid change of the maximal value and frequency of horizontal deflection current.

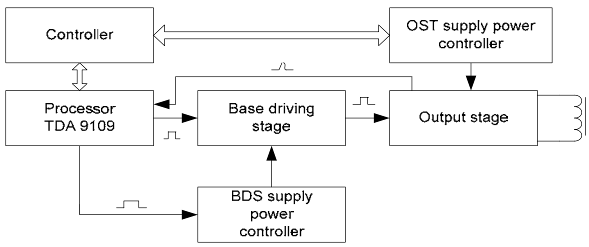

Fig. 1. The structure of horizontal deflection module with scanning processor

Transitional processes in the output stage

In order to form the excitation current of the output stage transistor in most cases the transformer is used between output and base driving stage.

At first, it separates conditionally low voltage circuits from high voltage circuits. Secondly, it is possible to receive positive and negative base current of needed shape by using only one positive voltage power supply in the base driving stage.

Output stage transistors (OST) mostly fails due to incorrect base circuit excitation or incorrect selection of the excitation mode. If the base excitation is too weak (or OST amplification coefficient is too small), then the saturation voltage is formed which is too high and it determines the increased (compared to nominal) conductance losses. If excitation is too strong (or OST amplification coefficient is too high) ST is switched off too slowly, and the losses during switch-off process are increased. The optimization of base excitation process allows minimizing these losses.

The secondary breakdown can be the other reason of OST failure, which is formed when unfavorable base and collector current and voltage combination is formed, even during the period of one line.

Specific resistance distribution in the transistor construction is characteristic to the BT used in output stages. The collector region is usually relatively thick, with high resistance, in order to receive high allowable collector-emitter junction voltage V_{ce}, and the base-emitter junction region is thin and with small resistance (the smaller the saturation voltage). The reverse voltage can be formed in the base-emitter junction during switch-off process due to such resistance distribution, if the excitation stage is inappropriately selected, and the base-emitter junction can be closed tightly. Thus the switching process is stopped. In this case the collector current starts to flow to the base, i.e. a process similar to diode switching is taking place. In other words, conditions are formed in the collector-base region, similar to diode, to which the reverse voltage is applied. The recuperation process grows slower due to the big amount of charge carriers contained in the collector; the transistor dissipated power is increased, especially in case of inductive load. Furthermore, local overheat points can emerge in the crystal and the thermal PT breakdown as a result, after which, for example for transistor BU2527DX, the resistance of base-transistor junction is decreased by 29-30 Ohms.

When the shape of the excitation signal applied to the base is incorrectly selected and when the negative switching voltage amplitude is too high, charge carriers are quickly sucked out of the areas close to base junction, therefore emitter is completely separated from the rest part of the transistor. The high-resistance collector area is relatively small.

The two stage structure, as shown in Fig. 1, is used in horizontal deflection channel most often. This scheme is simplified, the correction circuits are discarded.

If base current decreases more slowly during switch-off process, the reverse voltage is not formed in the base-emitter junction and the switch-off process continues. Emitter remains conductive, all injected charge carriers are pumped out and all transistor regions become non-conducting at the same moment of time. Because of this the collector current switch-off time is significantly shortened, dissipated power is decreased and the thermal breakdown possibility is eliminated. Certainly, the transitional processes will be longer in this case, but they are acceptable in the deflection generators.

Opposite course of action must be present during transistor switch-on: it is needed to achieve that the possibly larger part of high-resistance collector area would become conductive as quickly as possible. In order to achieve that, the base current must grow high sufficiently rapidly, till it reaches the needed amplitude – charge carriers have to be injected into high-resistance collector area as quickly as possible. Thus the base current in the beginning of switching has to be significantly bigger than it is required in order to saturate the transistor in the main part of switch-on process.

The low-voltage stage has to satisfy these conditions [2]:

- Rapid direct base current growth di_d/dt is required for the fast switch-on of the power stage transistor;
- Base current has to be sufficiently large, so that opened transistor would be fully saturated in order to minimize conductance losses;
- Controlled reverse base current di_d/dt for the removal of charge carriers contained in the transistor base, accelerating its switch-off in this way.

When using the matching transformer between low-voltage and power stages, the voltage acting on the base of power stage transistor can be described as

$$u_b(t) = \frac{n_s}{n_p}\left(\frac{D}{D-1}\right)u_{c1}(t), \qquad (1)$$

here D – the duty ratio of low-voltage stage transistor current; n_p and n_s are the number of primary and secondary winding turns, respectively; u_{c1} – low-voltage stage transistor collector voltage.

Under apriority assumption, that the square-shaped pulse with ½ duty ratio and sufficiently short rise time is applied to the base of base driving stage transistor, it follows from the (1) that low-voltage stage can control the shape and amplitude of OST base signal.

OST switching peculiarities: when OST is open, the positive base current has downward slope, and the collector current has upward slope; collector current varies from zero to the maximum; the base current of opening transistor is not large; base current of closing OST is large, and highest switching losses arise during switch-off – the largest collector current flows during the switch-off.

So, the OST switching losses are related to the magnitude of base current and the shape of its slope. They should be optimized in order to minimize GLT losses.

Various techniques are used to optimize base current, which are associated with particular stage implementation [4].

In order to reduce OST power losses it is purposeful to speed-up the removal of charge carriers out of transistor base using additional means, as it is shown in Fig. 2.

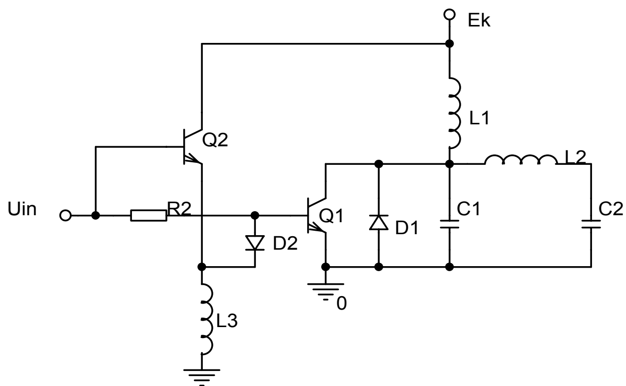

Fig. 2. Experimental circuit

On the basis of transitional analysis it was decided to use inductive element for additional removal of charge carriers and their injection into base of transistor Q_1. Currents vary only slightly in the inductive element during the transistor switching process – that is suitable for additional removal and injection of charge carriers. But it is not simple to connect the inductive element to the base of transistor Q_1.

The inductive element, connected to the base of transistor Q_1, should be saturated before closing transistor, and at the closing moment it should suck the positive charge carriers out of the base. In order to saturate the inductive element it should be connected to the power supply, but disconnected from the base of transistor Q_1, and contrarily in the transitional moment – it should be disconnected from the supply and connected to the transistor base.

When transistor Q_1 is open, very small current flows through the diode D_2, compare to base current of transistor Q_1, thus it is needed to select the diode D_2 with respective current-voltage characteristic, and also transistor Q_2 is open at the same time – the current flows through it and the coil, which saturates the coil L_3. With the drop of voltage U_{in} transistors Q_2 and Q_1 are closed, and current flowing through the coil L_3 doesn't stop flowing and it sucks out the positive charge carriers from transistor Q_1 over the diode D_2.

In order to make that the current does not flow through the diode D_2 when transistor Q_1 is open and in order to make that when the coil L_3 sucks out the positive charge carriers they would be forced to flow from the base of transistor Q_1 over the diode D_2, and not from the emitter of transistor Q_2, it is required that current-voltage characteristics of all three elements satisfy the conditions, illustrated in Fig. 3.

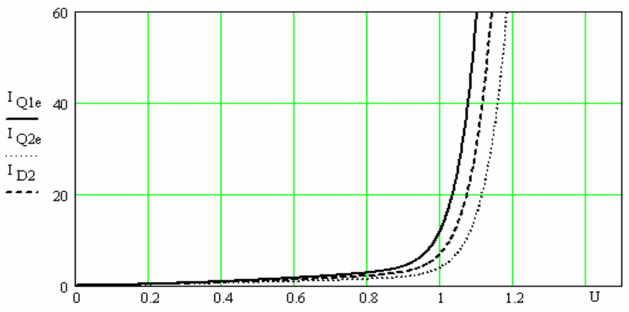

Fig. 3. Current-voltage characteristics of transistors Q_1, Q_2 and the diode

Thus transistor Q_1 should be opened when the smallest voltage is present, and transistor Q_2 – when the highest voltage is present. Diode opening voltage value has to be between opening voltage values of both transistors. Then when transistor Q_1 is open, current will not flow through the diode D_2 or its magnitude will be very small, in this case the opening of the transistor Q_2 is assured by resistor R_2 (Fig. 2). In the moment of transition – during the closing of the transistor Q_1, transistor Q_2 will be also closed, and the current will not stop flowing through the saturated coil and it will suck out all the charge carriers from the base of transistor Q_2 over the diode D_2 only in case if the diode opening voltage will be higher than the opening voltage of the transistor Q_2.

Experimental results

Simulation (OrCAD 9.1) results are presented in Fig. 3 and Fig. 4. Here the momentary power is normalized according to the maximal momentary power of the circuit without additional stored charge removal.

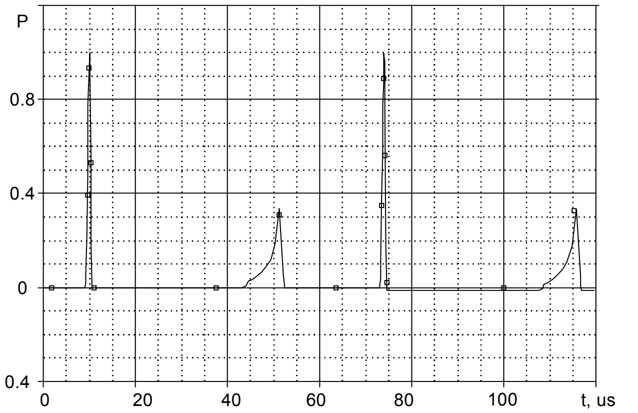

Fig. 4. Time diagram of the normalized momentary power without additional charge removal

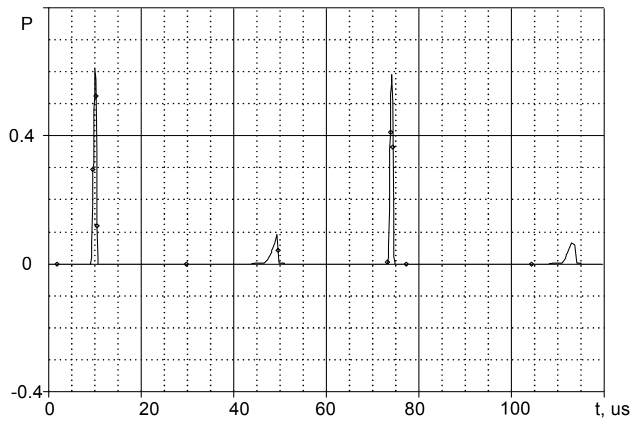

Fig. 5. Time diagram of the normalized momentary power in the circuit with additional charge removal

Initial modeling data: Q_1 – BU508; D_1 – BY249; L_1=7.36mH; R_{L1}=2Ω C_1=7.8nF; L_2=1.8mH; R_{L2}=1.8Ω; C_2=1μF; L_3=15μH; R_{L3}=1Ω.

Modeling results have shown that when selecting the inductance of the element L_3 it is possible to optimize the duration of transitional processes – the transistor closing time decreased almost three times. The momentary transistor dissipated power varies when varying the resistance value of R_2, but the shape of the current flowing through the deflection coil L_2 also varies. So it is possible to decrease the transistor Q_1 current only until the shape of the current flowing through the coil L_2 corresponds to the scanning linearity requirements.

The OST base current and simultaneously the losses in the OST may be controlled varying base driving stage supply voltage without affecting the shape of the current flowing through the coil L2. OST temperature was measured during the experiment. The results of the experiment are shown in Fig. 6.

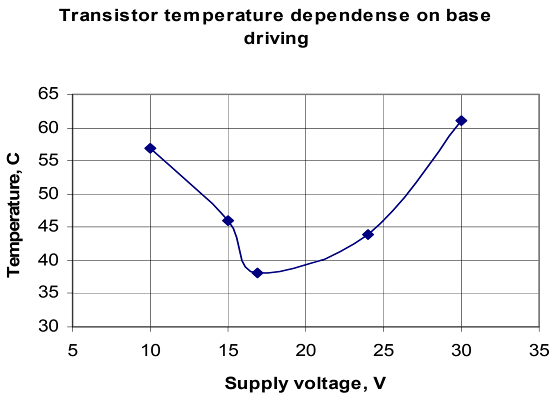

Fig. 6. Output stage transistor temperature dependence on the supply voltage of the low-voltage stage

Discussion

Bipolar transistors are used most often in the output stages to generate CPT horizontal deflection currents. Their operation mode is strongly related to the shape and magnitude of base current. Classic circuits are usually unsuitable for large diagonal CPT ant monitors. Various techniques and measures are offered for optimization of the power stage, but they are useful only in particular cases.

The offered technique of charge carrier injection into the base region permits the partial solution of power stage optimization. Experiments have shown, that the shape of the power stage transistor base current can be effectively varied when selecting the parameters of elements of primary winding „snubber“ (shunt) circuit of matching transformer.

Conclusions

1. When designing controlled output stages for horizontal deflection current generators for large diagonal CPT it is more beneficial to use bipolar transistors in these stages.
2. It is possible to reduce significantly the duration of transistor switching processes by using additional injection of charge carriers into the base of power stage transistor.
3. Charge carrier injection into the base significantly reduces the power loss in the power stage transistor during the switching processes.

References

1. **In-Hwan Oh.** Base Driving Method for the Horizontal Deflection Circuit. BJT Application Note II. – Fairchild Korea Semiconductor, Korea. – 1998. – 8 p.
2. **Sharples D.** CRT deflection. Designing 1 // Electronics World & Wireless World. – June, 1996. – No 6. – P. 472–479.
3. **Sharples D.** CRT deflection. Designing 2 // Electronics World & Wireless World. – July, 1996. – No 7. – P. 472–480.
4. **Billings K.H.** Switch mode Power Supply Handbook, Mc Graw-Hill, Inc. – 1989. – 343 p.
5. **Dumčius A.** Simulation of Sound Field in a Classroom // Electronics and Electrical Engineering. – Kaunas: Technologija, 2007. – No. 5(77). – P. 73–76.

Submitted for publication 2007 03 10

V. Augutis, D. Gailius, D. Styra, A. Dumčius. Transistor Control with Additional Charge Pumping Circuit // Electronics and Electrical Engineering. – Kaunas: Technologija, 2007. – Nr. 6(78). P. 79–82.

The main aim of this work was to determine the most efficient way for minimization of power loss in the horizontal deflection output stage transistor. In the monitors and TV receivers with the kinescopes of colored image in the final stage of horizontal deflection the high-voltage bipolar transistors of large power commonly are used. Because of their small factor of amplification base current must be comparatively large and they will change according to the complex law. For the formation of base current the transformer, suitable only for the specific set of elements, commonly is used. It is shown that the losses of switching can be decreased and even when the value of the voltage of supply of penultimate cascade. The simulation and experiment results are given. Ill. 6, bibl. 5 (in English; summaries in English, Russian and Lithuanian).

В. Аугутис, Д. Гайлюс, Д. Стира, А. Думчюс. Упрвалениe транзистора дополнительной инжекцией носителей заряда // Электроника и электротехника. – Каунас: Технология, 2007. – № 6(78). – С. 79–82.

Цель данной работы – выявить наиболее эффективный способ минимизации потерь в транзисторе оконечного каскада системы горизонтального отклонения. В мониторах и ТВ приемниках с кинескопами цветного изображения в оконечном каскаде горизонтального отклонения обычно применяются высоковольтные биполярные транзисторы большой мощности. Из-за их небольшого коэффициента усиления базовый ток должен быть сравнительно большой и изменяться по сложному закону. Для формирования базового тока обычно применяется трансформатор, пригодный только для определенного набора элементов. Представлены результаты моделирования и эксперимента. Ил. 6, библ. 5 (на английском языке; рефераты на английском, русском и литовском яз.).

V. Augutis, D. Gailius, D. Styra, A. Dumčius. Tranzistoriaus valdymas papildoma krūvininkų injekcija // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2007. – Nr. 6(78). – P. 79–82.

Monitoriuose ir TV imtuvuose su spalviniais kineskopais horizontaliojo kreipimo generatorių galinėse pakopose dažniausiai naudojami galingi dvipoliai aukštosios įtampos tranzistoriai. Dėl nedidelio stiprinimo koeficiento bazės srovės turi būti gana didelės ir kintančios laike pagal sudėtingą dėsnį. Valdymo srovei suformuoti paprastai naudojamas transformatorius, tinkantis tik tam tikram schemos elementų parametrų rinkiniui. Pasiūlyta ir išanalizuota galimybė papildomai valdyti horizontaliojo kreipimo galinės pakopos tranzistorių į jo bazę injektuojant krūvininkų. Parodyta, kad perjungimo nuostolius galima sumažinti parenkant priešgalinės pakopos maitinimo įtampą. Pateikti modeliavimo ir eksperimento rezultatai. Il. 6, bibl. 5 (anglų kalba, santraukos anglų, rusų ir lietuvių k.).