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Functional Delay Test Construction Approaches

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Introduction

Rapid advances of semiconductor technology lead to higher circuit integration as well as higher operating frequencies. Conventional fault models like the standard single stuck-at model were developed for gate-level logic circuits. Regardless of stuck-at fault model's efficiency for several decades, alternative models need to account for deep sub-micron manufacturing process variations [1]. Increasing performance requirements of circuits make it difficult to design them with large timing margins. Thus imprecise delay modeling, statistical variations of the parameters during the manufacturing process as well as physical defects in integrated circuits can sometimes degrade circuit performance without altering its logic functionality. These faults are called delay faults. Ensuring that the designs meet the performance specifications requires application of delay tests. However, delay fault testing of deep submicron designs is a complex task [2-6]. It requires application of two-vector patterns at the circuit's intended operating speed.

Two general types of delay fault models, the gate delay fault model [2] and the path delay fault model [3], have been used for modeling delay defects. Although the path delay fault model is generally considered to be more realistic and effective in modeling physical delay faults, it is often difficult to use in practice due to a huge number of paths in the circuit. Therefore, the gate delay fault model is more feasible for large circuits. The most commonly used gate delay fault model is the transition fault model [2]. However, an efficient fault model that will result in a high fault coverage and low computational complexity still remains to be elusive for gate-level circuit description.

In the case when a gate-level description of the Circuit-Under-Test (CUT) is not available or does not accurately describe the circuit, as is often the case in embedded core designs with Intellectual Property considerations, functional-level test generation must be performed. A test set generated at the functional level is independent of and effective for any implementation and, therefore, can be generated at early stages of the design process [7, 8]. Functional Automatic Test Pattern Generation (ATPG) can also be used to identify testability problems before an implementation is selected. Another advantage of functional ATPG for path delay faults over structural ATPG is related to the number of targeted faults. For structural ATPG, the number of faults is proportional to the number of paths in the circuit, which very often is exponential in circuit size. In the case of functional ATPG, the number of targeted faults is only proportional to the product of the number of inputs and the number of outputs in the circuit [8].

In this paper we analyse how the functional delay fault tests constructed using various test generation modes detect transition faults at gate-level. The paper is organized as follows. We review the related work in Section 2. We explore the properties of functional delay tests and present the experimental results in Section 3. We finish with conclusions in Section 4.

Related work

Functional fault models are proposed in [9-11]. Under these models, a fault is a tuple (I, O, tI, tO), where I is a CUT input, O is a CUT output, tI is a rising or falling transition at I , and tO is a rising or falling transition at O. Thus, four functional delay faults are associated with every input/output (I/O) pair and the total number of faults is 4*n*m, where n is the number of inputs of the CUT and m is the number of outputs of the CUT. A test for the functional delay fault is a pair of input patterns <u, v> that propagates a transition from a primary input to a primary output of a circuit [8]. Under the model introduced in Underwood et al. [9], only one pair of test patterns must be generated per fault. This model was expanded in Pomeranz and Reddy [11] by considering Δ different test patterns per fault. Δ is a positive integer, usually in the low hundreds, and is given as an input parameter for each CUT. Pomeranz and Reddy [10] proposed that all possible patterns are generated for each fault. This model guarantees detection of all robustly testable path delay faults in any gate-level implementation. However, the resulting test set sizes, as well as the test generation times, are very large and make this model impractical, especially for large circuits [10, 11]. However, the studies in [11] showed that it is not necessary to generate all possible test patterns for each fault in order to guarantee that actual path delays are covered in some gate-level implementation of the function. The validity of the model in Pomeranz and Reddy [11] is verified by applying the generated test sets to various gate-level implementations [8, 11].

Another model for functional ATPG based on input-output stuck-at faults testing and called pin pair (PP) fault model is suggested by Bareiša et al. in [12] and generalized in [13]. In [14] there are defined the rules how to get a functional delay fault test from the PP fault test. It is shown in the paper [14] that the functional delay tests obtained from PP tests correspond to tests generated using models proposed in [9-11]. In our work we use functional delay tests derived from the PP fault tests.

The possibilities of supplementing or expanding a particular test having a purpose to enhance test quality for detecting of delay faults are analysed in [4-6, 15-18]. Test sets for path delay faults in circuits with large numbers of paths are typically generated for path delay faults associated with the longest circuit path. This may lead to undetected failures since a shorter path may fail without any of the longest paths failing. The paper [4] proposes a test enrichment procedure that significantly increases the number of faults associated with the next-to longest paths that are detected by a compact test set. The alternative approach to this problem is a selection of the longest testable path [5, 6]. The papers [5, 6] combine the merits of both the transition fault model and the critical path delay model. Both papers agree that more automatic test pattern generation efforts are required to produce tests for all faults in this model than that given by the single transition fault model. Therefore the paper [5] suggests that to obtain a high quality transition fault test set using reasonable run times, initially a conventional transition fault test set can be generated and then augmented by a test based on the longest testable path passing through the fault site.

The other possibility to enhance test quality is the n-detection test set [15-17]. The n-detection test set is one where each fault f is detected by n different input patterns or by the maximum number of input patterns if f has fewer than n different input patterns that detect it. The paper [15] has proposed a reordering procedure to obtain n-detection test sets and variable n-detection test sets for transition faults. Though t_i and t_{i+1} are selected from the given test set as a test-pair for transition faults, authors do not consider the number of input changes between t_i and t_{i+1}. However, the multiple input change test-pairs have the following disadvantages: 1) hazards may occur by multiple input change test-pairs, and 2) multiple input change test-pairs have high power consumption. Further, the authors in [18] proved that single input change test sequences are more effective than multiple input change sequences to obtain high robust delay fault coverage. The paper [16] applies n-detection test sets to check path delay faults where n is a function of the number of paths through the check points.

Application of functional delay tests for transition fault detection

An interesting issue is how the tests generated for one type of faults cover the faults of another type. In this section we are going to analyse the test quality of functional delay tests in regard to transition faults. Both types of faults are designed for dynamic testing, however the test generation methods for these faults are different. The non-redundant ISCAS'85 benchmark circuits have been selected for experiments. The functional delay tests have been got from PP fault tests according to the rules presented in [14]. The test sets for PP faults were generated for the black-box model of the circuits [13] using a random search procedure. The black-box model represents a system by defining the behaviour of its outputs according to the values applied to its inputs without the knowledge of its internal organization. The black box models written in the programming language C for ISCAS'85 benchmark circuits were used by the test generation for the PP faults. The Synopsys test pattern generator TetraMAX was used for test generation of transition faults.

The parameters of the non-redundant ISCAS'85 benchmark circuits are given in Table 1. The numbers of testable functional delay faults were obtained analytically in [8].

Table 1. Parameters of the non-redundant ISCAS'85 benchmark circuits

Circuit	Gates	Inputs n	Outputs m	4*n*m	Testable functional delay (PP) faults	Transition faults
C432	160	36	7	1008	540	1412
C499	202	41	32	5248	5184	3430
C880	383	60	26	6240	1326	2396
C1355	546	41	32	5248	5184	3350
C1908	880	33	25	3300	3004	4848
C2670	1193	157	64	40192	3320	5646
C3540	1669	50	22	4400	2588	8960
C5315	2307	178	123	87576	10540	13816
C6288	2406	32	32	4096	3068	14422
C7552	3512	206	107	88168	12188	19160
Total	13258			245476	46942	77440

Now we will analyse how the functional delay fault tests constructed using various test generation modes detect transition faults at gate-level. Main attention will be paid to investigation of the possibilities to improve the transition fault coverage using n-detection functional delay fault tests. First we will explore 1-detection functional delay tests. 1-detection tests were generated using 4 different modes.

Mode 1 (M1). Suppose we have an input pattern w that detects q PP faults. Thus, for detection of q corresponding functional delay faults it is built of this pattern maximum l pairs of input patterns (signal transition on one input can cause signal transitions on s outputs, consequently, only one pair of input patterns is needed for detection of s functional delay faults) [14]. The test pattern pairs constructed in Mode 1 possess the change of signal value only on one input. Therefore, they are single-input transition (SIT) tests and functional robust [8]. Note that the obtained test detects 100% of targeted faults, i.e. functional delay faults.

Mode 2 (M2). The functional delay tests are constructed in the same way as in Mode 1. There is only one difference, namely, that initial PP tests were generated using another test generation tool.

Mode 3 (M3). In this mode every input pattern that detects PP faults is transformed only into one input pattern pair in such way: the signal value transition occurs on every input that is associated with PP fault detection on the considered test pattern. Consequently, if the test for PP faults consists of *p* input patterns the constructed functional delay test has p input pattern pairs too. The test pattern pairs constructed in Mode 3 possess the change of signal value on more than one input. Therefore, the constructed pattern pairs are multi-input transition (MIT) tests [8] and some of functional delay faults that are functional robustly detectable on SIT test may be functional nonrobust [8] or even worse not detectable on considered test pattern pair, because some activation conditions needed for signal propagation from particular input to particular output may be corrupted. Thus, the obtained test may not detect 100% of targeted faults, i.e. functional delay faults.

Mode 4 (M4). The functional delay tests are constructed in the same way as in Mode 3. There is only one difference, namely, the patterns in the test pair are counter changed, i.e. if in Mode 3 for particular PP fault test pattern the test pattern pair <u, v> was constructed then in Mode 4 the corresponding test pattern pair is <v, u>. The initial PP tests used in Modes 3 and 4 are the same as in Mode 1.

The experimental results of transition fault detection by 1-detection functional delay tests are presented in Table 2. The obtained test quality for every functional test generation mode is characterized by transition fault coverage and test size expressed as the number of test pattern pairs. The best transition fault coverages for particular circuit are in bold. The last two columns of Table 2 represent the Synopsys test pattern generator for transition faults TetraMAX. Remind that the tests generated in Modes 1-4 use algorithmic circuit description whereas TetraMAX uses gate-level circuit description and that transition faults are gate–level faults.

Table 2. Transition fault detection by 1-detection functional delay tests

Circuit	M1		M2		M3		M4		TetraMax	
	Coverage (%)	Test size	Coverage (%)	Test size	Coverage (%)	Test size	Coverage (%)	Test size	Coverage (%)	Test size
C432	**95.56**	348	93.53	349	87.28	117	52.98	117	100	142
C499	**94.40**	5180	**94.40**	5171	91.23	1077	94.29	1077	100	223
C880	**98.91**	1001	98.71	984	90.90	381	83.56	381	100	137
C1355	**97.13**	5162	**97.13**	5140	92.36	1011	92.09	1011	100	287
C1908	**95.24**	2359	93.40	2297	81.58	620	69.08	620	100	316
C2670	**96.51**	1820	94.79	1896	90.44	448	67.50	448	100	259
C3540	83.08	1457	84.30	1505	**88.28**	515	80.47	515	100	403
C5315	**98.41**	4950	98.23	4955	97.94	1169	89.24	1169	100	301
C6288	**99.75**	1065	99.54	1154	98.72	268	98.70	268	100	122
C7552	**99.21**	5801	98.82	5943	94.21	2115	98.90	2115	100	461
Average	**95.82**	2914	95.29	2939	91.29	772	82.68	772	100	265

If we examine the results of experiments presented in Table 2, we can see that the 1- detection functional robust SIT tests obtained in Modes 1 and 2 cover more than 95% of transition faults. The test generation tool used in Mode 1 produced better results for all circuits except circuit C3540. The tools used for initial PP fault test generation are very similar, main difference is in function applied for random pattern generation. However the obtained test coverages and sizes are comparable. For seven circuits the difference of transition fault coverage doesn't exceed 1%, for two – 2% and only for circuit C432 this difference is 2.03%. Modes 3 and 4 used for MIT functional delay test generation produced much worse transition fault coverages, particularly Mode 4, using which the obtained transition fault coverages are on average roughly 13% worse than in Modes 1 and 2. The on average 3.8 shorter tests don't overweight the 13% (Mode 4) or 5% (Mode 3) loss of transition fault coverage, thus in case of 1-detection functional delay test generation for transition fault detection the SIT tests must be preferred.

Now we will analyse n-detection functional delay tests. The tests were obtained using 7 different modes.

Mode 5 (M5). Tests obtained in Modes 1 and 2 are merged into one 2-detection functional delay test. The test pattern pairs composed in Mode 5 are single-input transition tests and functional robust.

Mode 6 (M6). One PP fault corresponds to one appropriate functional delay fault. However if the test pair <u, v> is a SIT test and detects functional delay fault (I, O, tI, tO), where tI is rising (falling) transition on input I and tO is rising (falling) transition on output O, then the test pair <v, u> detects functional delay fault (I, O, tI', tO'), where tI' is falling (rising) transition on input I and tO is falling (rising) transition on output O. This property is used in Mode 6. Thus, if we have an input pattern *w* that detects *q* PP faults for detection of corresponding functional delay faults there is built maximum 2**q* pairs of input patterns.

The functional delay test constructed in Mode 6 is 2-detection test. The test pattern pairs composed in Mode 6 are single-input transition tests and functional robust.

Mode 7 (M7). The functional delay tests are constructed in the same way as in Mode 6. There is only one difference, namely, that initial PP tests were generated using another test generation tool.

Mode 8 (M8). The tests obtained in Modes 1 and 3 are merged into one 2-detection functional delay test. One part of the test pattern pairs composed in Mode 8 are functional robust single-input transition tests and another part of the test pattern pairs are multi-input transition tests.

Mode 9 (M9). The tests obtained in Modes 3 and 4 are merged into one 2-detection functional delay test. The test pattern pairs composed in Mode 9 are multi-input transition tests.

Mode 10 (M10). The tests obtained in Modes 1 and 9 are merged into one 3-detection functional delay test. One part of the test pattern pairs composed in Mode 10 are functional robust single-input transition tests and another part of the test pattern pairs are multi-input transition tests.

Mode 11 (M11). The 2-detection tests obtained in Modes 6 and 7 are merged into one 4-detection functional delay test. The test pattern pairs composed in Mode 11 are single-input transition tests and functional robust.

The experimental results of transition fault detection by n-detection functional delay tests are presented in Table 3. The obtained test quality for every functional test generation mode is characterized by transition fault coverage and test size expressed as the number of test pattern pairs. The best transition fault coverages for particular circuit are in bold.

Table 3. Transition fault detection by n-detection functional delay tests

Circuit	M5		M6		M7		M8		M9		M10		M11	
	Coverage (%)	Test size	Coverage (%)	Test size	Coverage (%)	Test size	Coverage (%)	Test size	Coverage (%)	Test size	Coverage (%)	Test size	Coverage (%)	Test size
C432	98.11	697	97.67	696	97.89	698	97.38	465	93.02	234	98.48	582	**99.42**	1394
C499	94.40	10351	94.40	10360	94.40	10342	94.40	6257	**99.83**	2154	**99.83**	7334	94.40	20702
C880	99.17	1985	99.21	2002	98.91	1968	**100.00**	1382	91.78	762	**100.00**	1763	99.29	3970
C1355	97.13	10302	97.13	10324	97.13	10280	97.13	6173	98.69	2022	**98.99**	7184	97.13	20604
C1908	95.61	4656	97.48	4718	96.10	4594	96.04	2979	83.48	1240	96.74	3599	**97.85**	9312
C2670	98.35	3716	98.65	3640	95.71	3792	99.22	2268	91.73	896	**99.56**	2716	99.11	7432
C3540	89.03	2962	88.71	2914	90.07	3010	95.49	1972	90.77	1030	**96.85**	2487	93.79	5924
C5315	99.55	9905	99.58	9900	99.56	9910	**99.95**	6119	98.09	2338	**99.95**	7288	99.86	19810
C6288	99.88	2219	99.95	2130	99.94	2308	99.94	1333	98.72	536	99.94	1601	**99.99**	4438
C7552	99.52	11744	99.66	11602	99.24	11886	99.30	7916	99.11	4230	99.62	10031	**99.74**	23488
Average	97.08	5854	97.24	5829	96.90	5879	97.89	3686	94.52	1544	**99.00**	4459	98.06	11707

First we examine 2-detection tests. The best average transition fault coverage (95.82%) using 1-detection functional delay tests was achieved in Mode 1. Further we will use this coverage for comparison. Four (M5-M8) of five 2-detection modes allowed to improve the average transition fault coverage in range from 1.08% (Mode 7) to 2.07% (Mode 8). Only Mode 9 produced worse results: the average transition fault coverage was 94.52%, i.e. 1.3% worse than in Mode 1. Remind that that the tests generated in Mode 9 are pure MIT tests.

Let's more thoroughly analyse Modes 5-8. Modes 5-7 produce pure SIT tests; the improvement of transition fault coverage in comparison with Mode 1 is similar and ranges from 1.08% (Mode 7) to 1.42% (Mode 6). More interesting is the fact that for the tests constructed in Mode 5 two independent test generations of initial 1-detection PP fault tests were used, whereas Modes 6 and 7 require only one initial 1-detection PP fault test. Therefore, the construction of 2-detection functional delay tests takes twice less computing time than in Mode 5, because the computing time needed for functional delay test construction can be neglected in comparison with computing time needed for initial PP fault test generation. The best average transition fault coverage (97.89%) using 2-detection functional delay tests is achieved in Mode 8 and is almost equal to coverage (98.06%) achieved in Mode 11 which used 4-detection SIT functional delay tests. Remind that one part of the test pattern pairs composed in Mode 8 are SIT tests and another part of the test pattern pairs are MIT tests and that like Modes 6 and 7 Mode 8 requires only one initial 1-detection PP fault test. Another advantage of Mode 8 is that the test sizes are on average ~1.6 times lesser than in Modes 5-7 and ~3.2 times lesser than in Mode 11. We can generalize that in case of 2-detection functional test generation for transition fault detection the mixed (SIT and MIT) tests must be constructed.

The experimental results with 3 and 4-detection functional delay test are presented in the last 4 columns of Table 3. The 4-detection functional delay tests constructed in Mode 11 are SIT tests and allow to achieve 98.06% average transition fault coverage that is only marginally better (0.17%) than in Mode 8, but the obtained tests are much longer than in Mode 8. Apparently the best average transition fault coverage (99%), which is acceptable even for manufacturing test, is achieved with 3-detection functional delay tests produced in Mode 10. The sizes of tests built in Mode 10 are comparable with sizes of 2-detection tests and ~2.6 times lesser than sizes of 4-detection tests. One part of the test pattern pairs composed in Mode 10 are 1-detection SIT tests and another part of the test pattern pairs are 2-detection MIT tests and that like Modes 6-8 Mode 10 requires only one initial 1-detection PP fault test. At the end of analysis of all 11 functional delay fault test generation modes we can conclude that definitely the best is Mode 10.

In general, the test generation task at algorithmic level is more complicated than at gate-level because all possible realizations of design must be taken into account. Therefore, the tests are larger compared to tests for particular realization of the circuit. For comparison the sizes of tests produced using Synopsys test pattern generator for transition faults TetraMAX are presented in the last column of Table 2. As we see, the average test size by 100% transition fault coverage is only 265 test pattern pairs. And this test size is ~17 times less than average test size of tests produced in Mode 10. However, the test generation at algorithmic level can be done in parallel with the circuit synthesis process and the suitable test patterns for the synthesized gate-level implementation have to be selected on the base of the fault simulation. It is a pity that we don't have such automated test pattern selection tool. Thus we manually did the selection of the suitable test patterns for circuit C6288. We got the average test size of 562 test pairs, whereas TetraMAX produced 122 test pairs.

At the end of this section we present some considerations about SIT and MIT tests. The authors in [18] state that SIT test sequences are more effective than MIT sequences to obtain high robust delay fault coverage. That is probably true for path delay faults however misfit for transition fault detection using functional delay tests. Let‘s analyse the transition fault coverages of circuits C499 and C1355. We see that the transition fault coverages of SIT tests coincide and are 94.4% and 97.13% respectively, i.e. even the appliance of 4-detection SIT tests doesn‘t improve the fault coverage. We made for these two circuits additional experiments. Namely, we generated for each circuit 10-detection SIT tests, which test sizes were above 70000 test pattern pairs, but and employment of 10-detection SIT tests didn‘t improve the transition fault coverages. However, the pure MIT tests constructed in Mode 9 let us to achieve better transition fault coverages 99.83% and 98.69% for circuits C499 and C1355 respectively. There is only one explanation of this fact, namely, that some circuits contain transition faults, which are hard-to-detect or not detectable with SIT tests constructed at algorithmic level. Another argument for application of MIT test is that definitely the best functional test generation Mode 10 produces the test set where one part of the test pattern pairs are 1-detection SIT tests and another part of the test pattern pairs are 2- detection MIT tests. Thus the MIT tests complement SIT tests or vice versa.

Conclusions

In this paper we have explored the properties of n-detection functional delay fault tests. The functional delay fault tests were built using 11 different test generation modes and we have analysed how tests generated at algorithmic level are suitable for detection of gate-level transition faults.

Our experimental results show that the test sets, which are generated according to the functional delay fault model, obtain high fault coverages of transition faults. The 1-detection SIT tests cover up to 95.8% of transition faults, whereas 1-detection MIT test exposed up to 13% worse coverage. Therefore, in case of 1-detection functional delay test generation for transition fault detection the SIT tests must be preferred. On other hand mixed SIT and MIT tests exposed the best results in case of 2- detection functional delay test generation. The employment of such sets allowed improving the transition fault coverage up to 97.8%. The experiments with 3 and 4-detection functional delay test generation modes demonstrated that definitely the best of all 11 considered modes is 3-detection functional delay test generation mode, using which the composed test is comprised of 1-detection SIT test and of 2-detection MIT test. The achieved in this mode transition fault coverage of 99% is acceptable even for manufacturing test.

Some authors state that SIT test sequences are more effective than MIT sequences to obtain high robust delay fault coverage. That is probably true for path delay faults, however our experiment show that this statement misfits for transition fault detection using functional delay tests. There is only one explanation of this fact, namely, that some circuits contain transition faults, which are hard-to-detect or not detectable with SIT tests constructed at algorithmic level. Another argument for application of MIT test is that definitely the best considered functional test generation mode produces the test set where one part of the test pattern pairs are MIT tests. Therefore, it is necessarily to complement SIT tests with the MIT tests or vice versa.

In general, the test generation task at algorithmic level is more complicated than at gate-level because all possible realizations of design must be taken into account. Therefore, the tests are much larger compared to tests for particular realization of the circuit. However, the test generation at algorithmic level can be done in parallel with the circuit synthesis process and the suitable test patterns for the synthesized gate-level implementation have to be selected on the base of the fault simulation.

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It is explored how functional delay tests constructed at algorithmic level detect transition faults at gate-level. Main attention was paid to investigation of the possibilities to improve the transition fault coverage using n-detection functional delay fault tests. The proposed functional delay test construction approaches allowed achieving 99 % transition fault coverage which is acceptable even for manufacturing test. Bibl. 18 (in English; summaries in English, Russian and Lithuanian).

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Анализируется пригодность функциональных тестов задержки, сгенерированных на алгоритмическом уровне, для проверки вентильного уровня неисправностей переключения. Основное внимание уделено увеличению качества теста путем многократного обнаружения неисправности. Предложенные авторами способы конструирования функциональных тестов позволили достичь 99 % полности покрытия неисправностей переключения, приемлемую даже для производственного теста. Библ. 18 (на английском языке; рефераты на английском, русском и литовском яз.)

E. Bareiša, V. Jusas, K. Motiejūnas, R. Šeinauskas. Funkcinių vėlinimo gedimų testų konstravimo būdai // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2007. – Nr. 2(74). – P. 49–54.

Tiriamas funkcinių vėlinimo gedimų testų, sugeneruotų pagal schemos algoritminius aprašus, tinkamumas ventilinio lygmens perėjimo gedimams tikrinti. Daugiausia dėmesio skirta testo kokybės gerinimui, naudojant daugkartinio gedimo aptikimo testus. Pasiūlyti funkcinių testų kostravimo būdai leido pasiekti 99 % perėjimo gedimų patikrinimo išsamumą, priimtiną ir gamybiniam testui. Bibl. 18 (anglų kalba; santraukos anglų, rusų ir lietuvių k.).