Fractional-Order Phase Shifters with Constant Magnitude Frequency Responses

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Abstract—This contribution presents and experimentally analyzes the idea how to reach the constant magnitude as well as the phase response in the fractional-order (FO) phase when shifting two-ports. The straightforward method employing the automatic gain control circuit (AGC) in a cascade after socalled constant phase block approximating FO integrator or differentiator is studied. The variable gain amplifier utilized in AGC and simple RC-based FO constant phase elements (approximating capacitors with order alpha = 1/4 and alpha = 1/2 as an example) connected in the feedback of operational amplifier-based integrator are established in the experimental setup. The operation indicated in three decades (between 100 Hz and 100 kHz) is evaluated. The known solutions of the standard FO phase shifting circuits are discussed and generally compared with the features obtained in this paper, together with the supposed effects of AGC on their performances.

Index Terms—Automatic gain control circuit; Constant magnitude response; Constant phase block; Constant phase element; Differentiator; Fractional-order; Integrator; Phase Shifter; Variable gain amplifier.

I. INTRODUCTION

The standard two-ports, allowing the wideband flat phase shift (e.g., lossless differentiators or integrators, i.e., $\pm 90^{\circ}$) for the first-order circuits [1]–[4]), have a direct relation between the magnitude and the phase frequency response. When the phase is constant and the frequency is changing, then the magnitude must have a monotone character (± 20 dB/dec for the first-order systems, e.g., [1], [2]). Special circuits allowing different phase shifts from the standard integer-order concept (i.e., $\pm \alpha \times 90^{\circ}$, where α represents the non-integer order achieving values between 0 < $|\alpha|$ < 1) already exist [3]. However, their magnitude has only less steep slope of the magnitude increase or decrease

Manuscript received 8 December, 2018; accepted 29 May, 2019.

This article is based upon a work supported by COST (European Cooperation in Science and Technology), COST Action CA15225. This research was funded by a grant (No. LO1401) from the National Sustainability Program and a grant (No. LTC18022) from the Ministry of Education, Youth and Sports, Inter-Cost program. For the research, infrastructure of the SIX Center was used.

 $(\pm \alpha \times 20 \text{ dB/dec})$ than in case of the integer-order circuits. Nevertheless, the feature of the constant phase and, also, the magnitude response in a specified bandwidth (impossible in standard linear circuits due to fundamental principles) could be very beneficial and useful for many applications, especially phase shifters (PSs).

If the constant magnitude frequency response of PS is required, a decreasing/increasing nature of the impedance (utilized in active two-ports) with the frequency need to be somehow compensated. These impedances may have a standard integer-order character or may be represented by the fractional-order (FO) inductor or capacitor also. These FO inductors/capacitors are also known as so-called constant phase elements (CPEs) created intentionally from the passive RC elements [4], [5]. Moreover, the CPE character can be observed in nature [6], [7].

There are three possible solutions for obtaining the constant magnitude response. The first approach is based on the utilization of the inverse transfer function, i.e., the second CPE of the same order needs to be employed. However, it can cause the accumulation of the magnitude errors, since both CPEs are different due to the tolerances of the passive components. The concept of two CPEs can lead to the magnitude frequency response, which becomes significantly rippled. The second approach comprises the frequency dependent amplification control, i.e., amplifier with external gain control is utilized. Control voltage or current should be derived from CPE already engaged in PS. The last one comprises automatic gain control circuit (AGC) that effectively maintains the constant output level for different input levels by automatic variation of gain. Our paper presents the example of the last method because of the simplicity.

II. FO CONSTANT PHASE ELEMENT

The fractional-order elements (FOEs) can be obtained in various forms (liquid chemicals [8], polymers [9], ferroelectric materials [10], carbon [11], composites of various materials and resistive-capacitive elements with

distributed parameters [12], etc.). However, the easiest and cheapest form of FOE can be obtained by serial-parallel ladder structures of precise resistors and capacitors. The two-terminal passive RC device creating FO frequency-dependent impedance response (symbolically, in ideal case, $Z_{\text{CPE_C}}(s) = 1/(s^{\alpha}C_{\alpha})$ for FO capacitor; $Z_{\text{CPE_L}}(s) = (s^{\alpha}L_{\alpha})$ for the FO inductor) can be designed by various methods [13], [14]. We use a method presented by Valsa *et al.* [4], [5] that is applied on the circuitry shown in Fig. 1.

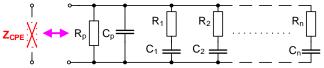


Fig. 1. One of the typical RC representations of constant phase element.

The values of particular elements (FO capacitors) designed by the method proposed in [4], [5] for the ideal bandwidth 10 Hz–100 MHz (practically, valid up to units of MHz) and the ideal phase ripple $\Delta \varphi_{\alpha} = 0.5$, and the order $\alpha_1 = 1/4$, and the $\alpha_2 = 1/2$ are summarized in Table I. Note that it results into n = 14 (14 branches for serial RC segments).

TABLE I. PARAMETERS OF DESIGNED CPEs (FO CAPACITORS).

	$\alpha_1 = 1/4$	$p_{\alpha 1} = 22.5^{\circ}$	$\alpha_2 = 1/2 \ (\varphi_{\alpha 2} = 45)$		
i	$C_{\rm i}$	$R_{\rm i}$	$C_{\rm i}$	$R_{\rm i}$	
1	33 μF	$30.2 \text{ k}\Omega$	4.35 μF	230 kΩ	
2	9.9 μF	$20.2 \text{ k}\Omega$	1.95 μF	103 kΩ	
3	3 μF	13.5 kΩ	870 nF	46 kΩ	
4	886 nF	9 kΩ	389 nF	20.6 kΩ	
5	265 nF	6 kΩ	174 nF	9.2 kΩ	
6	79 nF	$4~\mathrm{k}\Omega$	78 nF	4.1 kΩ	
7	24 nF	2.7 kΩ	35 nF	1.8 kΩ	
8	7.1 nF	$1.8~\mathrm{k}\Omega$	16 nF	822 Ω	
9	2.1 nF	1.2 kΩ	7 nF	368 Ω	
10	635 pF	807 Ω	3.1 nF	164 Ω	
11	190 pF	540 Ω	1.4 nF	74 Ω	
12	57 pF	361 Ω	623 pF	33 Ω	
13	17 pF	242 Ω	280 pF	15 Ω	
14	5 pF	162 Ω	125 pF	7 Ω	
	$C_p = 2 pF$,	$R_{\rm p} = 15 \ {\rm k}\Omega$	$C_{\rm p} = 100 \; {\rm pF}, R_{\rm p} = 280 \; {\rm k}\Omega$		

III. FO PHASE SHIFTER

It is well-known that phase frequency response is related with magnitude response via Hilbert transformation [15] and the phase shift between the output and the input network quantity can be expected from any circuit, which contains frequency dependent elements. Remember that, if utilized as voltage-mode PS, high input and low output impedance needs to be achieved. A cascade of FO integrator/differentiator and variable gain amplifier [16], [17] with a function of automatically controllable gain, represent the simplest way how to create the constant (flat) magnitude and phase traces of the frequency response. The frequency dependent two-port visible in Fig. 2 ($Z_{CPE}(s)$ indicates the position of CPE) with the operational amplifier (OA) [16], [17] have the character of FO integrator. Some literature (see [18] and references cited therein) refer these two-ports to as constant phase blocks (CPBs) also. The LT1364 IC [19] is selected for the presented example as OA in CPB. The second member of the cascade represents the automatic gain control circuit (discussed further in the text). The transfer response of the system can be expressed as

$$K_{C}(s) = \frac{V_{OUT}}{V_{INP}} = \frac{Z_{CPE}(s)}{R_{g}} \times K_{AGC}(V_{OUT}). \tag{1}$$

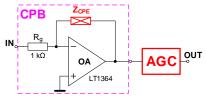


Fig. 2. The simplest solution of FO phase shifter with constant magnitude and phase response.

The magnitude of impedance $Z_{\text{CPE_C}}(s)$ has a monotone decrease (given by character of CPE: $-\alpha \times 20 \text{ dB/dec}$) of its value with the frequency. This decrease can be automatically compensated by AGC block in order to obtain the output with a constant magnitude response in a specified bandwidth.

IV. AUTOMATIC GAIN CONTROL CIRCUIT

The AGC maintains the constant output voltage level that is independent of the input signal level and frequency in the ideal case. The complete topology of AGC is given in Fig. 3, including the values of passive components.

The feedback of AGC is derived from the output of VGA as it is shown in the case of solution in [20]. The single VGA ensures gain compensation for the input signal within 60 dB dynamical range [20] in the operational frequency bandwidth. The $C_{\rm C}$ and $R_{\rm C}$ components serve for AC coupling. These values determine the lowest -3 dB frequency as possible,

$$f_d = \frac{1}{2\pi R_C C_C},\tag{2}$$

approximately reaching units only of Hz. The variable gain amplifier (VGA) creates the core of AGC block. In our case, VCA810 [20] is selected. The diode (BAT42) doubler ($C_{a1,2}$, $R_{a,b}$, $D_{1,2}$) generates DC error voltage derived from the output level. The inverted and integrated sum of the error voltage and constant DC level from R_P (setting actual gain for static case - without time variable input signal) is then inverted again (driving voltage of VGA must be in negative polarity [20]) and stored by C_{a5} . The response of the AGC is given by the time constant of the diode detector, C_{a3} and R_{f} , and C_{a5} . The low-cost operational amplifiers TL072 [21] can be used in the relatively slow feedback loop. The design of AGC cannot be described in more detail due to the page limit of this paper [22]. An analytical (mathematic) solution is not often available, even it is unsuitable for transient simulations. The gain of the AGC [20] in the operational bandwidth can be estimated as follows

$$|K_{AGC}|[dB] \cong 20 \times \log \left[10^{2(|V_{control}|-1)}\right],$$
 (3)

where $V_{\text{control}} \sim V_{\text{error}} (v_{\text{AGC OUT}}(t)) + V_{\text{initial_set}}$. The designed AGC has some real practical limitations. The AGC itself is tested (with DC coupling). The magnitude frequency

response of the AGC itself is flat (gain about +8.5 dB with the acceptable deviation ± 1 dB) approximately from 30 Hz up to 450 kHz and the phase response can be considered as

acceptable because of the deviation of $\pm 3^{\circ}$ kHz up to 100 kHz. Therefore, AGC itself limits further applications to the bandwidth 30 Hz \rightarrow 100 kHz (Fig. 4).

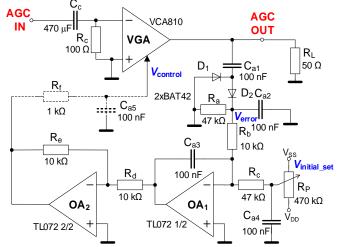


Fig. 3. The complete structure of AGC used in Fig. 2.

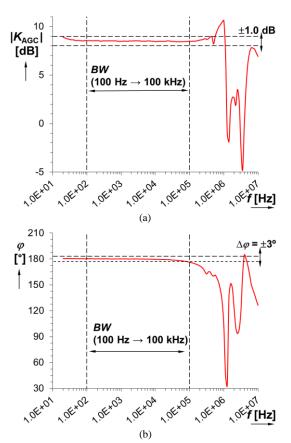


Fig. 4. The frequency response plots of standalone AGC (measured results): (a) Magnitudes; (b) Phases.

The expected operational bandwidth for the application shown in Fig. 2 (including the impact of AC coupling capacity on phase response) should fit the range from 100 Hz up to 100 kHz (indicated in Figures). The highest contribution of the gain dependent group delay (τ_d) of VGA on phase deviation in operational range reaches $\varphi(f_{\rm IN}=100~{\rm kHz})\cong\tau_d\times\omega\cong5\times10^{-9}\times2\pi\times100\times10^3=3.14\times10^{-3}~{\rm rad}~(0.18^\circ)$ [20]. The transient (step) response of AGC on the fast edge of square wave signal (Fig. 5) indicates the time delay between the input and output signal equal to

104 ns and settling time equal to $5.1 \mu s$.

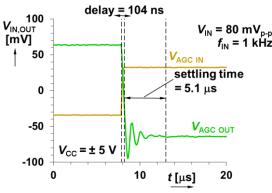


Fig. 5. The transient (step) response of AGC on edge of square wave (measured results).

We can see that AGC itself has minimal impact in this bandwidth (the acceptable delay and settling time for the supposed application). Note that the wider operation and faster response of the AGC systems than used in our design are possible [23], [24], but this requires more difficult/complex design and precise high-speed active elements, also, in the feedback loop of the AGC. Nevertheless, the presented design is sufficient for the application shown in this contribution.

V. EXPERIMENTAL VERIFICATION OF PHASE SHIFTER

Two CPEs ($\alpha_1 = 1/4$ and $\alpha_2 = 1/2$) defined in Section II are tested in the system shown in Fig. 2. Oscilloscope DSO-X-3022T/FRA is used for the following experiments with circuitries from Fig. 1–Fig. 3. We consider the acceptable magnitude and the phase shift inaccuracy as ± 1 dB and $\pm 3^{\circ}$ (from ideal flat traces) in the operational bandwidth 100 Hz–100 kHz. The PS (Fig. 2) with $Z_{CPE}(s)$ fulfilling $\alpha_1 = 1/4$ and $\alpha_2 = 1/2$ creates the response shown in Fig. 6. Note that the inverting character of AGC as well as transfer of the operational amplifier-based two-port yield negative polarity of the phase shift (-22.5° and -45° in ideal case) as expected from the non-inverting integrator. The gain in observed

operational bandwidth is set by $V_{\rm initial_set}$ approximately to 4.5 dB because the integrator has very high gain at low frequencies. This setting avoids saturation of the VGA by very large input signals at the lowest frequency of the operational bandwidth. The difference of measured results (as error of magnitude and phase) from ideal magnitude and phase responses is shown in Fig. 7. The maximal error from ideal values (flat traces of +4.5 dB in the magnitude and -22.5° and -45° in phase responses) reaches -8 % with variation of ± 2 % in the magnitude and 15 % for the phase response of $\alpha_1 = 1/4$. Note that these results are expected these deviations from flat responses are obtained within the allowed tolerance of magnitude and the phase fluctuations ± 1 dB (experiments yield even better results ± 0.5 dB) and $\pm 3^\circ$.

The measured dependence of the pass band gain (and control voltage $V_{\rm control}$) of the AGC, compensating the decreasing magnitude (in operational bandwidth) of integrator with CPE, is shown in Fig. 8. The $Z_{\rm CPE}(s)$ having $\alpha_1 = 1/4$ (low steepness -5 dB/dec of the slope) requires the magnitude change within 15 dB. The AGC compensates magnitude change 30 dB, when $Z_{\rm CPE}(s)$ has $\alpha_2 = 1/2$ (high steepness -10 dB/dec of the slope) as it is clear from Fig. 8.

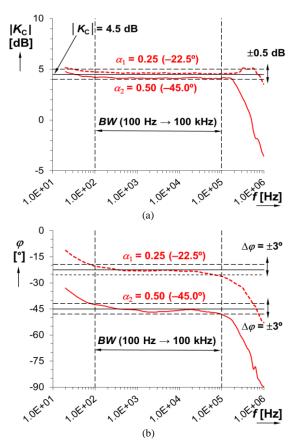


Fig. 6. The frequency response plots for PS including $Z_{CPE}(s)$ of $\alpha_1 = 1/4$ and $\alpha_2 = 1/2$ (measurement results): (a) Magnitudes; (b) Phases.

The example of time domain responses of the system on different excitation signals (frequency: $f_{\rm IN} = 1 \, \rm kHz$, input level: $V_{\rm IN} = 100 \, \rm mV_{p-p}$) with $\alpha_1 = 1/2$ is shown in Fig. 9. The example of spectral analysis of the sine wave input signal is shown in Fig. 10. The observed total harmonic distortion (THD) stays below 1 % and this is valid for the whole studied operational bandwidth. Power consumption reaches

250 mW at $\pm 5 \text{ V}$ (2·25 mA). This is given mostly by the active elements used and it is a fact that this is not intended to be a low-power design.

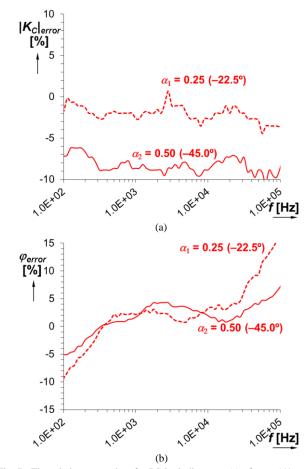


Fig. 7. The relative error plots for PS including $Z_{CPE}(s)$ of $\alpha_1 = 1/4$ and $\alpha_2 = 1/2$ in observed band (100 Hz–100 kHz): (a) Magnitudes; (b) Phases.

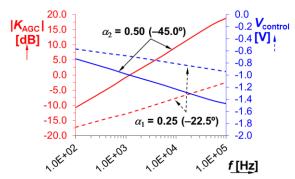
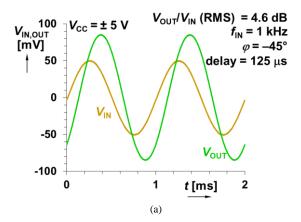


Fig. 8. The frequency response plots of AGC for $Z_{CPE}(s)$ with $\alpha_1 = 1/4$ and $\alpha_2 = 1/2$ gain in operational bandwidth (pass band).



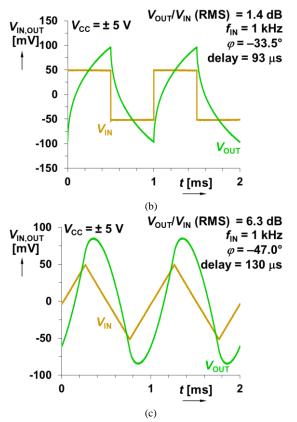


Fig. 9. The time domain responses for PS including $Z_{CPE}(s)$ of $\alpha_2 = 1/2$ (measurement results) and excitation: (a) Sine wave; (b) Square wave; (c) Triangular ramp.

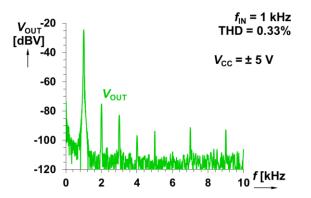


Fig. 10. The measured frequency spectrum for PS including $Z_{CPE}(s)$ of $\alpha_2 = 1/2$.

VI. COMPARISON OF PROPOSED PS WITH KNOWN TYPES OF FO PHASE SHIFTING SOLUTIONS

The Table II is prepared for a brief comparison of the selected typical FO systems [25]–[30] serving for phase shifting and supposed effect of the AGC on behavior.

TABLE II. BRIEF COMPARISON OF TYPICAL FO SYSTEMS SERVING FOR PHASE SHIFTING.

Reference	Number of active components	Constant magnitude response	Constant phase response	Validity of constant magnitude and phase	May AGC help with flat/constant magnitude and phase response?	Is AGC already included in design?		
FO Phase Shifters								
[25]	1-2	Yes	No	single tone	-	-		
[26]	2-3	Yes	No	single tone	-	-		

Reference	Number of active components	Constant magnitude response	Constant phase response	Validity of constant magnitude and phase	May AGC help with flat/constant magnitude and phase response?	Is AGC already included in design?		
	FO All-pass Filters							
[28]	2	No	No	single tone	No	-		
[29]	2	No	No	single tone	No	-		
FO Constant Phase Blocks (integrators/differentiators)								
[18]	15	No	Yes	single tone	Yes	No		
[27]	1	No	Yes	single tone	Yes	No		
[30]	1	No	Yes	single tone	Yes	No		
Proposed								
Fig. 2	4	Yes	Yes	operational bandwidth	Yes	Yes		

Note that standard all-pass filtering solution, including FO CPE (instead of integer-order capacitor), does not have typical response of the phase shifting circuits [28], [29] and cannot be used in this design. From Table II, it is clear that AGC may be very helpful for the constant phase and the magnitude response in concepts of constant phase blocks (integrators/differentiators).

VII. CONCLUSIONS

The proposed solution confirms possibility to obtain constant phase and, also, magnitude response in limited bandwidth given by the features of the selected and designed AGC system. The measured results indicate usability in three decades (100 Hz–100 kHz), when overall $\pm 3^{\circ}$ phase and ± 0.5 dB magnitude ripple are obtained while THD < 1%.

Theoretically, each CPB can be easily extended by AGC block in order to be applied in a phase shifter (see Table II). The slight extension of the circuitry (additional active elements) is the cost for such a modification. The future work in this field should concentrate on analysis of the discussed approaches, indicated in the introductory part, as well as on improvements and optimization of AGC systems for the presented purposes (FO phase shifters) in the wider operational bandwidths.

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