Novel Reconnection-Less Reconfigurable Filter Design Based on Unknown Nodal Voltages Method and Its Fractional-Order Counterpart

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Abstract—A novel solution of reconnection-less electronically reconfigurable filter is introduced in the paper. The filter is designed based on unknown nodal voltages method (MUNV) using operational transconductance amplifiers (OTAs) and variable gain amplifier (VGA). The structure can provide all-pass, band-stop, high-pass 2nd order functions, highpass function of the 1st order and direct transfer from the same topology without requirement of manual reconnection. The proposed structure also offers the electronic control of the pole frequency. Moreover, fractional-order design of the proposed filter is also provided. The behaviour is verified by simulations using Cadence IC6 (spectre) software.

Index Terms—Electronic control; Electronic reconfiguration; Operational transconductance amplifier; Reconfigurable filter; Universal filter.

I. INTRODUCTION

The possibility of modification and fine adjusting of the transfer function of the frequency filters has been found quite useful feature in case of the signal processing [1]. Therefore, the ability to change the type of the resulting frequency response of the circuit is being a favourable property sought by many researchers. Many scientific works [2]-[6] deal with this issue by the design of filtering structures referred to multifunction/universal when these filters provide several, if not all, standard transfer functions (low pass (LP), band pass (BP), high pass (HP), band stop (BS) and all pass (AP)). These functions, however, are obtainable between different nodes of the network resulting in a filter requiring multiple inputs or outputs, when the switching between these inputs/outputs is necessary in order to obtain a desired function. The above-mentioned multifunction/universal filters can be divided, depending on the number of inputs/outputs, into single input - multiple output (SIMO) filters [2], [3] and multiple input - single

This article is based upon work from COST Action CA15225, a network supported by COST (European Cooperation in Science and Technology). Research described in this paper was financed by the National Sustainability Program under grant LO1401 and by the Ministry of education, Youth and Sports under grant LTC18022 of Inter-Cost program. For the research, infrastructure of the SIX Center was used.

output (MISO) filters [4], [5]. It is also possible to come across the so called single-input single-output filters [6], but manual modification of the internal topology is necessary in this case. However, switching between inputs/outputs and manual modification of the internal topology is not suitable or possible in cases such as full on-chip implementation, etc.

Thus, the idea of the change of type of the frequency response of two-port (filter) without the necessity to modify the internal topology or a position of the input or the output port(s) by setting of the electronically controllable active elements (many novel controllable active elements are summarized in [7]) is an advantageous approach to the filter These filtering structures referred design. are to as reconnection-less reconfigurable filters [8]-[13]. The resulting output response of these filters depends on the setting of electronically controllable parameters of used active elements. Table I provides a comparison of the previously reported reconnection-less reconfigurable filters.

The domain of fractional-order filters [14]–[18] also caught the interest of many research teams. The fractional-order filters can be designed in two conventional ways. The first approach is an approximation of the fractional-order Laplacian operator s^{α} using a function of a higher order [14], [15]. The other way is based on the so-called Fractional-Order Elements (FOE). The FOEs are usually substituted by effectively designed RC ladder networks [16]–[18] due to the absence of commercially available FOEs.

The proposed filter offers the 2nd order functions (HP, BS, AP) and it also offers HP transfer function of the 1st order and direct transfer between the input and output of the filter. All these functions are available by suitable setting of electronically controllable active elements without the necessity of manual modification of the internal topology or switching between inputs/outputs of the filter. The passband/stop-band region at lower frequencies can be easily adjusted. It offers also a special high-pass function with transfer zero (HPZ). Furthermore, the filter offers the electronic control of its pole frequency. Moreover, the proposed structure is later complemented with the FOE in order to confirm the suitability of the structure for the fractional-order filter design.

Manuscript received 14 December, 2018; accepted 2 March, 2019.

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Ref No.	[8]	[9]	[10]	[11]	[12]	[13]	Fig. 2
Year	2011	2015	2015	2016	2018	2018	-
No. of active elements	2	4	4	2	4	6	4
No. of passive elements	4	2	2/3	3	4	4	2
Type of active element(s)	CCII-	ΟΤΑ	ΟΤΑ	DO-CA, DVCC	CG-CCDDCC	VDTA, ACA, MO-CF	OTA, VGA
Type of control	В	$g_{ m m}$	$g_{ m m}$	<i>B</i> , <i>g</i> _m	$B, R_{\rm X}$	<i>B</i> , <i>g</i> _m	A, g_{m}
Operation mode	VM	VM	VM	СМ	VM	СМ	VM
Available transfer functions (2nd order if not indicated)	AP, BS	AP, BP, BS, HP, LP, HPZ, LPZ	AP, BP, BS, HP, LP, HPZ, LPZ	BS, HP, LP, HPZ, LPZ	AP, BP, BS, HP, LP, HPZ, LPZ	AP, BP, BS, HP, LP, HPZ, LPZ	AP, BS, HP, HPZ, HP 1 st order, DT

TABLE I. COMPARISON OF RECENTLY REPORTED RECONNECTION-LESS RECONFIGURABLE FILTERS.

Note: A list of previously unspecified abbreviations: CCII – second generation current conveyor, OTA – operational transconductance amplifier, DO-CA – dual-output current amplifier, DVCC – differential-voltage current conveyor, CG-CCDDCC – controlled-gain current-controlled differential difference current conveyor, VDTA – voltage-differencing transconductance amplifier, ACA – adjustable current amplifier, MO-CF – multiple-input current follower, B – current gain, g_m – transconductance, R_X – input resistance, A – voltage gain, VM – voltage mode, CM – current mode, LPZ – low-pass with zero, DT – direct transfer.

II. DESIGN PROPOSAL

The proposed filter has been designed based on the matrix method of the unknown nodal voltages (MUNV) [1], using two types of active elements. MUNV is a suitable way for the symbolic analysis and synthesis of linear circuits such as linearized amplifiers, filters, etc. It is based on wellknown relation $\mathbf{Y} \cdot \mathbf{V} = \mathbf{I}$, where **Y** is a square admittance matrix, V stands for a column vector of unknown nodal voltages and I is designated for a column vector of excitation current sources. The first active element used in the proposal is an Operational Transconductance Amplifier (OTA) [7]. The schematic symbol of the OTA is depicted in Fig. 1(a). It has two voltage input and one current output terminals and the relation between the terminals follows the expression $I_{\text{out}} = g_{\text{m}} \cdot (V_{\text{in+}} - V_{\text{in-}})$, where g_{m} denotes the transconductance. The OTA has been implemented by a multiplier with a current output introduced in [19] which is designed in ON Semiconductor 0.35 µm I3T CMOS process. Its transistor-level model can be found in [19]. The transconductance of this implementation is controlled via DC voltage V_{SET_gm}. The second used active element, (shown in Fig. 1(b)), is a Variable Gain Amplifier (VGA) [7]. The behaviour of the VGA is described as $V_{\text{out}} = A \cdot (V_{\text{in+}} - V_{\text{in-}})$, where A is the voltage gain of this element. The VGA has been also implemented by a multiplier from [19] while the multiplier provides the transfer from input voltage to output current, depending on its gm and a resistor $(R = 1/g_m)$ connected to the output of the VGA is used to transfer the output current back to voltage. The voltage gain A is controlled by a DC voltage $V_{\text{SET A}}$ when $A = k \cdot V_{\text{SET A}} \cdot R$ (|k| =2 mA/V²) [19].

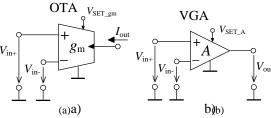


Fig. 1. Schematic symbol of a) OTA, b) VGA.

We start the design by the expectation of the resulting transfer function which is then used for circuit synthesis. The desired transfer function is described as:

$$K(s) = \frac{s^2 C_1 C_2 - s C_2 g_{m3} + g_{m1} g_{m2} A}{s^2 C_1 C_2 + s C_2 g_{m1} + g_{m1} g_{m2}}.$$
 (1)

In this case we consider that the designed circuit has three independent nodes and one excitation source, in order to obtain a SISO type filter. The MUNV matrix of such circuit has the following form:

$$\begin{pmatrix} Y_{11} & Y_{12} & Y_{13} \\ Y_{21} & Y_{22} & Y_{23} \\ Y_{31} & Y_{32} & Y_{33} \end{pmatrix} \cdot \begin{pmatrix} V_1 \\ V_2 \\ V_3 \end{pmatrix} = \begin{pmatrix} I_1 \\ 0 \\ 0 \end{pmatrix}.$$
 (2)

For the simplicity of the proposal and an easier calculation, we will omit voltage gain A in (1) for now (the circuit would have four independent nodes). Considering the proposed structure with capacitor C_1 between nodes 1 and 3 and capacitor C_2 connected to node 2, the relation (2) turns into:

$$\begin{pmatrix} sC_1 & 0 & -sC_1 \\ 0 & sC_2 & 0 \\ -sC_1 & 0 & sC_1 \end{pmatrix} \cdot \begin{pmatrix} V_1 \\ V_2 \\ V_3 \end{pmatrix} = \begin{pmatrix} I_1 \\ 0 \\ 0 \end{pmatrix}.$$
(3)

In order to obtain the same transfer functions as in (1) and supposing $K(\mathbf{s}) = V_{\text{OUT}}/V_{\text{IN}} = V_3/V_1 = \Delta_{1,3}/\Delta_{1,1}$, the determinants $\Delta_{1,1}$ and $\Delta_{1,3}$ have to as follows:

$$\Delta_{1,1} = Y_{22}Y_{33} - Y_{32}Y_{23} = b_2s^2 + b_1s + b_0 = s^2C_1C_2 + sC_2g_{m1} + g_{m1}g_{m2} = sC_2(sC_1 + g_{m1}) - [(-g_{m1}g_{m2})], \quad (4)$$

$$\Delta_{1,3} = Y_{21}Y_{32} - Y_{31}Y_{22} = a_2s^2 + a_1s + a_0 = s^2C_1C_2 - sC_2g_{m3} + g_{m1}g_{m2} = (-g_{m2})(-g_{m1}) - [(-sC_1 + g_{m3})sC_2]. \quad (5)$$

Supplementing (4) and (5) into (3), the final matrix takes form of:

$$\begin{pmatrix} sC_1 & 0 & -sC_1 \\ -g_{m2}A & sC_2 & g_{m2} \\ -sC_1 + g_{m3} & -g_{m1} & sC_1 + g_{m1} \end{pmatrix} \cdot \begin{pmatrix} V_1 \\ V_2 \\ V_3 \end{pmatrix} = \begin{pmatrix} I_1 \\ 0 \\ 0 \end{pmatrix}.$$
(6)

To be able to obtain some transfer functions, the low-pass function has to be controllable. Thus, either g_{m1} or g_{m2} has to be multiplied by voltage gain A in (6). In order to influence the coefficient of the s^0 term in the numerator of the transfer function, voltage gain A has to multiply Y_{21} (already included in (6)). This will cause the designed circuit to have four independent nodes (there is no other component connected to node 4, it only provides direct connection between the output of the VGA and input of the OTA₂).

The matrix (6) can be then directly transferred into a circuit scheme shown in Fig. 2.

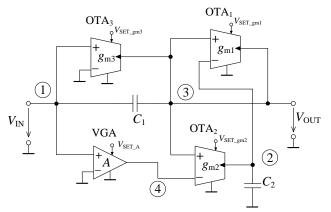


Fig. 2. Proposed reconnection-less reconfigurable filter using three OTAs and one VGA.

The proposed filter consists of three OTAs, one VGA and two capacitors and its transfer function is identical to (1). The transfer function of the HP of the 1st order is equal to $K(s) = sC_1/(sC_1 + g_{m1})$. A special function HPZ can be obtained for the same setting as in case of BS, except that voltage gain A is less than 1. It would be also possible the inverting BP to obtain LPZ and function by supplementing the structure with one voltage amplifier at the output of the filter. The specific setting of control voltages of the controllable parameters of the used active elements, depending on desired output response, is summarized in Table II.

TABLE II. SETTING OF CONTROL VOLTAGES FOR SPECIFIC

OUTPUT RESPONSE.						
	V _{SET gm1}	V _{SET gm2}	V _{SET gm3}	V _{SET A}		
AP	0.5 V	0.5 V	0.5 V	0.5 V		
BP	0.5 V	0.5 V	0 V	0.5 V		
HP	0.5 V	0.5 V	0 V	0 V		
1st-order HP	0.5 V	0 V	0 V	0.5 V		
DT	0 V	0.5 V	0 V	0 V		
HPZ	0.5 V	0.5 V	0 V	< 0.5 V		

The relations for the pole frequency and quality factor of the proposed filter are as follows:

$$\begin{cases} f_0 = \frac{1}{2\pi} \sqrt{\frac{g_{m1}g_{m2}}{C_1 C_2}}, \\ Q = \sqrt{\frac{C_1 g_{m2}}{C_2 g_{m1}}}. \end{cases}$$
(7)

From (7) is evident that f_0 can be electronically controlled, independently from Q, by changing g_{m1} and g_{m2} transconductances while following the condition $g_{m1} = g_{m2}$.

III. DESIGN VERIFICATION

Simulations using Cadence IC6 (spectre) software have been carried out to verify the design correctness. The circuit has been simulated using the active element described in the previous section while the supply voltage is equal to ± 1.65 V. As the initial state, the values of all parameters were set accordingly: the values of transconductances are $g_{m1} = g_{m2} = g_{m3} = 1$ mS, capacitors $C_1 = 1$ nF and $C_2 = 2$ nF, voltage gain A is equal to 1. This specific setting results in theoretical f_0 equal to 112.5 kHz and Q equal to 0.707 (Butterworth approximation). The particular setting of the filter parameters depending on desired output response is summarized in Table II.

The transfer functions of BS, HP, HP of the 1st order and DT are shown in Fig. 3. The simulation results are presented by coloured lines and the theoretical expectations by black dashed lines. As it can be seen, the obtained results are in good agreement with the theoretical expectations. Minor differences between the simulation and theoretical results (which occur in case of all presented results) are caused by the parasitic features of the used active elements. The specific setting of independent filter parameters, according to the desired transfer function, can be found in Table II.

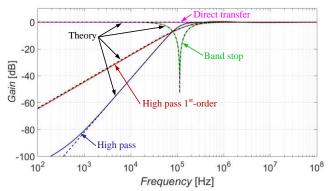


Fig. 3. Output responses of BS, HP, HP of the 1st-order and DT – simulations (coloured lines), theoretical expectations (black dashed lines).

Figure 4 depicts the characteristics of the all pass filter (group delay (blue line), phase (red line) and gain (green line)).

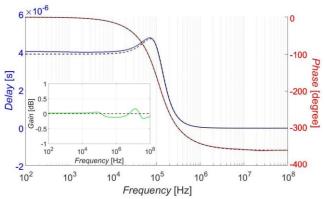


Fig. 4. AP filter – group delay (blue line), phase (red line) and gain (green line), theory (black dashed lines).

The illustration of the electronic control of f_0 of the proposed filter in case of the BS function is shown in Fig. 5. As mentioned before, the frequency f_0 is controlled by the values of transconductances g_{m1} and g_{m2} which are set by the

DC voltages $V_{\text{SET}_{gm1}}$ and $V_{\text{SET}_{gm2}}$. For illustrative purposes, the values of these voltages have been set to 0.25 V, 0.5 V and 1 V which correspond with the values of the transconductances equal to 0.5 mS, 1 mS and 2 mS resulting in the theoretical pole frequencies of 56.3 kHz, 112.5 kHz and 225.1 kHz. The actual values of f_0 obtained from simulations are stated in Fig. 5. It can be seen that the obtained values are close to the theory.

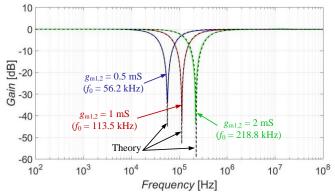


Fig. 5. Example of the electronic control of f_0 for $g_{m1} = g_{m2} = 0.5$ mS, 1 mS and 2 mS.

The special function HPZ (high-pass with transfer zero) and its comparison to the theory is presented in Fig. 6.

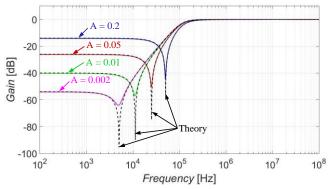


Fig. 6. Demonstration of behaviour of HPZ – simulations (coloured lines) vs. theory (black dashed lines).

The HPZ has the same setting as the BS function except that voltage gain A is less than 1, which provides the adjustment of the pass-band/stop-band region at lower frequencies. The value of the voltage gain A has been set to 0.2, 0.05, 0.01 and 0.002 (corresponding with the values of control voltage V_{SET_A} equal to 0.1 V, 0.025 V, 0.005 V and 0.001 V).

IV. FRACTIONAL-ORDER FILTER

The proposed filtering structure has been supplemented by the FOE to provide fractional-order behaviour. A fractional-order capacitor $C_{\alpha} = C\omega_0^{1-\alpha}$ [20] implemented by the 5th-order RC topology of the Cauer I type [20] (depicted in Fig. 7) has been applied to the proposed structure replacing capacitor C_2 .

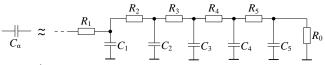


Fig. 7. 5th-order RC structure of the Cauer I type used to approximate C2.

The denominator of the fractional-order function, calculated based on the general fractional-order transfer functions with Butterworth characteristics [21], is described as:

$$D(s) = s^{1+\alpha} + s^{\alpha} \frac{g_{m1}}{C_1} + \frac{g_{m1}g_{m2}}{C_1 C_{2\alpha}}.$$
 (8)

The Oustaloup approximation [22] has been used in order to calculate the values of the individual components of the RC structure for the tested values of parameter α . The calculations were carried out using a Matlab script. All the values are summarized in Table III (for the HP function). The value of capacitor C_1 is equal to 10 nF and the pole frequency was chosen $f_0 = 10$ kHz. The values of transconductances g_{m1} and g_{m2} have to be recalculated depending on the actual value of capacitor C_2 which depends on the selected value of parameter α . The values of g_{m1} and g_{m2} are calculated comparing the particular term of (8) and general fractional order transfer functions [21]. The resulting values of g_{m1} and g_{m2} are also included in the table.

TABLE III. VALUES OF COMPONENTS OF THE RC STRUCTURE FOR HP FUNCTION IN DEPENDENCE ON VALUE OF ALPHA.

α/part	0.3	0.5	0.7
$C_{2\alpha}$ [µF/sec ^{1-α}]	22.8	2.51	0.28
$R_0 \left[\Omega \right]$	1831.0	6439.5	178867.6
$R_1[\Omega]$	399.8	159.2	63.4
$R_2[\Omega]$	471.4	462.9	454.4
$R_3[\Omega]$	687.3	1025.2	1525.9
$R_4 [\Omega]$	1143.6	2464.5	5239.1
$R_5[\Omega]$	1802.9	5364.3	14827.6
C_1 [nF]	1.5	2.2	3.85
$C_2 [nF]$	5.2	4.2	3.52
C ₃ [nF]	18.4	10.2	5.7
<i>C</i> ₄ [nF]	69.4	27.0	10.7
C5 [nF]	336.0	97.8	32.2
g_{m1} [µS]	259.7	397.1	585.1
g_{m2} [µS]	1302.0	894.8	636.5

Figure 8 illustrates the behaviour of the fractional-order HP function for three chosen values of parameter α ($\alpha = 0.3$, 0.5 and 0.7). The values of the resulting orders (*n*) obtained from simulations are stated in Fig. 8. The simulation results are in good agreement with the expected results. From the graph, it can be seen that the used approximation does not follow the correct slope of the transition between pass-band and stop-band region under frequency of 100 Hz because the approximation ceases to be valid anymore.

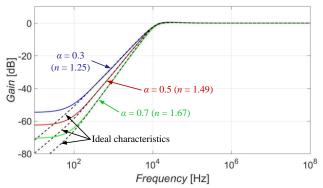


Fig. 8. Demonstration of fractional-order HP function for $\alpha = 0.3, 0.5$ and 0.7 – simulations (coloured lines), ideal characteristics (black dashed lines).

V. CONCLUSIONS

The features of proposed filter have been verified by simulations in Cadence IC6 (spectre) software. The filter provides all presumed transfer functions, depending on the setting transconductances and the voltage gain (all controlled electronically by DC voltages) without the necessity of any kind of reconnection of input or output node. All obtained results are close to the theoretical expectations. In case of the electronic control of the pole frequency of the filter for the theoretical chosen $f_0 = 56.3$ kHz, 112.5 kHz and 225.1 kHz, the obtained values of f_0 are 56.2 kHz, 113.5 kHz and 218.8 kHz. The proper function of the fractionalorder filter has been also proved, providing orders 1.25, 1.49 and 1.67 for theoretical orders 1.3, 1.5 and 1.7.

REFERENCES

- [1] W. K. Chen, *The Circuits and Filters Handbook, Third Edition.* CRC Press: New York, 2009.
- [2] V. Chamnanphrai, W. Sangiamvibool, "Electronically tunable SIMO mixed-mode universal filter using VDTAs", *Przegląd Elektrotechniczny*, vol 93, no. 3, pp. 207–211, 2017. DOI: 10.15199/48.2017.03.48.
- [3] S. Lin, X. Zuo, X. Deng, "Current and voltage mode resistorless universal biquad filter using a single CCCDTA", *Chinese Journal of Electronics*, vol. 27 no. 6, 2018, pp. 1250–1257. DOI: 10.1049/cje.2018.08.007.
- [4] A. Yesil, D. Ozenli, E. Arslan, F. Kacar, "Electronically tunable MOSFET-only current-mode biquad filter", *Int. J. Electron. Commun.* (AEÜ), vol. 81, 2017, pp. 227–235. DOI: 10.1016/j.aeue.2017.07.019.
- [5] J. Pimpol, O. Channumsin, W. Tangsrirat, "MISO universal filter employing single VDTA", in *Proc. Int. Conf. Engineering, Applied Sciences, and Technology (ICEAST 2018)*, Phuket, Thailand, 2018, pp. 1–4. DOI: 10.1109/ICEAST.2018.8434454.
- [6] H. D. Tran, H. Y. Wang, Q. M. Nguyen, N. H. Chiang, W. C. Lin, T. F. Lee, "High-Q biquadratic notch filter synthesis using nodal admittance matrix expansion", *Int. J. Electron. Commun. (AEÜ)*, vol. 69, pp. 981–987, 2015. DOI: 10.1016/j.aeue.2015.03.001.
- [7] D. Biolek, R. Senani, V. Biolkova, Z. Kolka, "Active elements for analog signal processing: Classification, review, and new proposals", *Radioengineering*, vol. 17, no. 4, pp. 15–32, 2008.
- [8] R. Sotner, J. Jerabek, B. Sevcik, T. Dostal, K. Vrba, "Novel solution of notch/all-pass filter with special electronic adjusting of attenuation in the stop band", *Elektronika ir Elektrotechnika*, vol. 17, no. 7, pp. 37–42, 2011. DOI: 10.5755/j01.eee.113.7.609.
- [9] R. Sotner, J. Petrzela, J. Jerabek, T. Dostal, "Reconnection-less OTA based biquad filter with electronically reconfigurable transfers", *Elektronika ir Elektrotechnika*, vol. 21, no. 3, pp. 33–37, 2015. DOI: 10.5755/j01.eee.21.3.10205.
- [10] R. Sotner, J. Petrzela, J. Jerabek, K. Vrba, T. Dostal, "Solutions of

reconnection-less OTA-based biquads with electronical transfer response reconfiguration", in *Proc. 25th Int. Conf. Radioelektronika*, Pardubice, Czech Republic, 2015. pp. 40–45. DOI: 10.1109/RADIOELEK.2015.7128991.

- [11] J. Jerabek, R. Sotner, J. Polak, K. Vrba, T. Dostal, "Reconnectionless electronically reconfigurable filter with adjustable gain using voltage differencing current conveyor", *Elektronika ir Elektrotechnika*, vol. 22, no. 6, pp. 39–45, 2016. DOI: 10.5755/j01.eie.22.6.17221.
- [12] R. Sotner, L. Langhammer, O. Domansky, J. Petrzela, J. Jerabek, T. Dostal, "New reconfigurable universal SISO biquad filter implemented by advanced CMOS active elements", in *Proc. 15th IEEE Int. Conf. Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD 2018)*, Prague, Czech Republic, 2018, pp. 257–260. DOI: 10.1109/SMACD.2018.8434560.
- [13] L. Langhammer, R. Sotner, O. Domansky, T. Hricko, "Electronically reconfigurable universal filter based on VDTAs", in *Proc. 28th IEEE Int. Conf. Radioelektronika*, Prague, Czech Republic, 2018, pp. 1–4. DOI: 10.1109/RADIOELEK.2018.8376353.
- [14] T. J. Freeborn, "Comparison of (1 + α) fractional-order transfer functions to approximate lowpass Butterworth magnitude responses", *Circuits, Systems, and Signal Processing*, vol. 35, no. 6, 2015, pp. 1983–2002. DOI: 10.1007/s00034-015-0226-y.
- [15] G. Tsirimokou, C. Psychalinos, A. S. Elwakil, "Fractional-order electronically controlled generalized filters", *International Journal of Circuit Theory and Applications*, vol. 45, no. 5, 2017, pp. 595–612. DOI: 10.1002/cta.2250.
- [16] T. J. Freeborn, B. Maundy, A. S. Elwakil, "Approximated fractional order Chebyshev lowpass filters", *Mathematical Problems in Engineering*, vol. 2015, pp. 1–7, 2015. DOI: 10.1155/2015/832468.
- [17] L. A. Said, S. M. Ismail, A. G. Radwan, A. H. Madian, M. F. Abu El-Yazeed, A. M. Soliman, "On the optimization of fractional order lowpass filters", *Circuits, Systems, and Signal Processing*, vol. 35, no. 6, pp. 2017–2039, 2016. DOI: 10.1007/s00034-016-0258-y.
- [18] I. Dimeas, G. Tsirimokou, C. Psychalinos, "Experimental verification of filters using fractional-order capacitor and inductor emulators", in *Proc. Int. Conf. Telecommunications and Signal Processing*, Vienna, Austria, 2016, pp. 559–562. DOI: 10.1109/TSP.2016.7760943.
- [19] R. Sotner, J. Jerabek, R. Prokop, V. Kledrowetz, J. Polak, "A CMOS multiplied input differential difference amplifier: a new active device and its applications", *Applied Sciences*, vol. 7, no. 1, pp. 1–13, 2017. DOI: 10.3390/app701010.
- [20] G. Tsirimokou, "A systematic procedure for deriving RC networks of fractional-order elements emulators using MATLAB", *Int. J. Electron. Commun. (AEÜ)*, vol. 78, pp. 7–14, 2017. DOI: 10.1016/j.aeue.2017.05.003.
- [21] D. Kubanek, T. Freeborn, "(1+alpha) Fractional-order transfer functions to approximate low-pass magnitude responses with arbitrary quality factor", *Int. J. Electron. Commun. (AEÜ)*, vol. 83, pp. 570–578, 2018. DOI: 10.1016/j.aeue.2017.04.031.
- [22] M. Sugi, Y. Hirano, Y. F. Miura, K. Saito, "Simulation of fractal immitance by analog circuits: an approach to the optimized circuits", *IEICE Trans. Fundam. Electron. Commun. Comput. Sci.*, vol. E82, no. 8, pp. 1627–1634, 1999.