

# Implementation of a Memcapacitor Emulator with Off-the-Shelf Devices

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**Abstract**—We implemented a memcapacitor emulator with off-the-shelf electronic devices. The memcapacitor is an element whose capacitance can be altered with external current or voltage. The implementation of the emulator is very important since commercial versions are not yet available. The proposed memcapacitor emulator has a simple dedicated memcapacitor architecture that does not require a mutator. It is the first memcapacitor emulator implemented with commercially available devices. The operation as a memcapacitor has been proven via both breadboard experiments and PSPICE simulations.

**Index Terms**—Memory element, memristor emulator, memcapacitor emulator, off-the-shelf devices.

## I. INTRODUCTION

The discovery of the physical model of a memristor by the HP group [1] has attracted considerable interest from researchers in the areas of memory, neural synapses and logic circuit applications [2]–[6]. The model was originally postulated by Leon O. Chua as the fourth basic circuit element [7]. Related two other circuit elements, memcapacitors and meminductors [8], which are the higher-order elements in Chua's  $\alpha$  and  $\beta$  periodic table [9], also show memory features. Though it is widely known that memristors, memcapacitors and meminductors are promising elements for the implementation of memory smaller than any other existing memories, they are not expected to be commercially available in the near future due to cost and technical difficulties. Emulators can be useful alternatives for the development of application circuits.

In contrast to memristor emulator [10], memcapacitor emulator has not been studied actively so far. The only contribution for memcapacitor emulator is a mutator-based approach, in which memcapacitance is obtained via transforming memristance using mutators [11]–[13]. Since

the memcapacitor is built in an indirect way of employing mutators, the circuit is rather complicated, which leads to difficulty in building complicated circuits. Recently, Biolek et al., presented a SPICE model of the memcapacitor emulator without a mutator [14]. However, it is only a SPICE model, and its feasibility has not yet been proven. In this study, we designed a simple dedicated memcapacitor circuit without mutators and implemented it with off-the-shelf electronic devices. It is the first memcapacitor emulator implemented with commercially available devices. The operation of the proposed memcapacitor emulator as a memcapacitor has been shown via both breadboard experiments and PSPICE circuit simulations.

## II. MEMCAPACITOR AND MEMCAPACITIVE SYSTEM

Memcapacitance is based on the nonlinear relationship between integral of charge and integral of flux. Memcapacitor with a relation  $f_{MC}(\sigma, \varphi)$  is defined as

$$\sigma = \int_{t_0}^t q(t)dt, \quad \varphi = \int_{t_0}^t v(t)dt. \quad (1)$$

Assume that  $\varphi$  is a function of  $\sigma$ , then, it leads to

$$\frac{d\varphi}{dt} = \frac{d\varphi}{d\sigma} \frac{d\sigma}{dt}. \quad (2)$$

Since  $\frac{d\varphi}{dt} = v(t)$  and  $\frac{d\sigma}{dt} = q(t)$ , it follows from (1) and (2) that

$$v(t) = \frac{d\varphi}{d\sigma} q(t), \quad \text{or} \quad q(t) = \frac{d\sigma}{d\varphi} v(t). \quad (3)$$

Therefore, the term  $\frac{d\sigma}{d\varphi}$  in (3) denotes a kind of capacitance with nonlinear features called memcapacitance and is denoted as

$$C_M = \frac{d\sigma}{d\varphi}. \quad (4)$$

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By applying a voltage or current to the memcapacitor, its capacitance can be altered. A common fingerprint of the memcapacitor and the memcapacitive system is their pinched hysteresis loops in the charge versus voltage plane, under any bipolar sine wave-like excitations, which is the unique qualitative phenomena that are absent from that of other passive elements resistor, inductor, and capacitor. Due to these phenomena, the capacitance depends upon the past history of input signal, which enables this device to function as a memory.

The voltage controlled memcapacitor is defined as

$$q(t) = C_M(x_1, x_2, \dots, x_n)v(t), \quad (5)$$

where  $C_M$  is the memcapacitance and  $x_i$ 's are the state variables and  $q$  and  $v$  are charge and voltage respectively. The state variables  $x_1, x_2, \dots, x_n$  are defined by "n" differential equations where  $n \geq 1$ , called the associated state equations, as follows

$$\frac{dx}{dt} = f[x, x, \dots, x, v], \quad k = 1, 2 \dots n. \quad (6)$$

If the device possesses only a single variable  $x$  ( $n=1$ ) and it is a function of only the voltage  $v$ , the device is called ideal voltage controlled memcapacitor.

Similarly the  $n^{\text{th}}$  order charge controlled memcapacitive system is defined as:

$$v(t) = D_M(x_1, x_2, \dots, x_n)q(t), \quad (7)$$

$$\frac{dx_k}{dt} = f_k[x_1, x_2, \dots, x_n, q], \quad k = 1, 2 \dots n, \quad (8)$$

where  $D_M$  is the inverse of memcapacitance  $C_M^{-1}$ .

The basic relation between  $v(t)$ ,  $q(t)$ , and internal state  $x(t)$  for  $n=1$  in a charge-controlled memcapacitor is defined as:

$$v(t) = D_M(x, q, t)q(t), \quad (9)$$

$$\frac{dx(t)}{dt} = f(x, q, t), \quad (10)$$

where  $D_M(\cdot)$  and  $f(\cdot)$  are the nonlinear functions that depend on the physical implementation of the memcapacitive systems.

Figure 1 shows the concept of a memcapacitor in which the capacitance is adjusted by the width ( $L$ ) of the dielectric [14].  $L$  is varied from  $L_{min}$  to  $L_{max}$  according to the limits of capacitances ( $C_{M, max}, C_{M, min}$ ) and inverse capacitance ( $D_{M, min}, D_{M, max}$ ).

The inverse of the memcapacitance that depends on the state variable is given by

$$D_M(t) = D_{M, Min} + \Delta D x(t), \quad (11)$$

where  $\Delta D = (D_{M, Max} - D_{M, Min})$ .

The state equation for a charge-controlled memcapacitor in a linear model is described as

$$\frac{dx(t)}{dt} = K_1 q(t), \quad (12)$$

where  $K_1$  is the mobility factor.

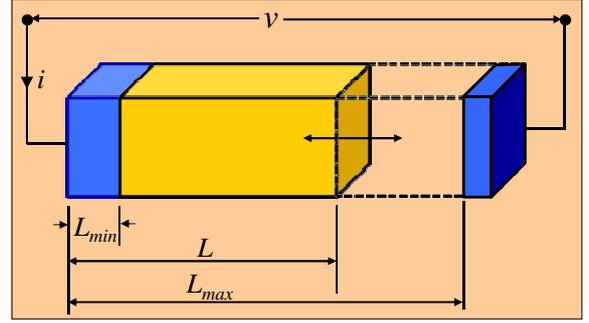


Fig. 1. Memcapacitor with charge-dependent dielectric.

Integrating (12) with respect to time  $t$

$$x(t) = K_1 \int q(t) dt, \quad (13)$$

where the initial state is assumed to be zero.

From (9), (11) and (13), the relation between the voltage and charge in a memcapacitor is given by

$$v(t) = (D_{M, Min} + K \int q(t) dt) q(t), \quad (14)$$

where  $K = \Delta D K_1$  is a constant.

From (3), (4) and (14), the inverse of memcapacitance

$$D_M = C_M^{-1} = \frac{d\varphi}{d\sigma} = D_{M, Min} + K \int q(t) dt. \quad (15)$$

### III. BASIC ARCHITECTURE OF MEMCAPACITOR EMULATOR

The proposed memcapacitor emulator is designed in the way of composing the input capacitance as a function of applied voltage. Figure 2(a) is the basic idea to implement memcapacitor using buffer and Fig. 2(b) is the equivalent circuit to design the memcapacitor emulator.

The input voltage  $v_{in}$  in Fig. 2(a) is given by

$$v_{in} = v_A - v_B = \frac{1}{C_S} \int i_{in} dt - v_B = \frac{q}{C_S} - v_B. \quad (16)$$

where  $v_A$  is the voltage across the capacitor  $C_S$  and  $v_B$  is the voltage to the input terminal and  $i_{in}$  is the input current across the capacitor.

If  $v_B$  is the proportional to the charge, then

$$v_{in} = \frac{q}{C_S} - mq = \left( \frac{1}{C_S} - m \right) q, \quad (17)$$

where  $v_B = mq$ . Equation (17) implies that the inverse of memcapacitor is  $D_M = C_M^{-1} = \left( \frac{1}{C_S} - m \right)$ . If the value of

$m$  is controlled to the time integral of the charge, then, the circuit in Fig. 2 acts as a memcapacitor. To emulate  $v_B$  in (17), integrator and analog multiplier are implemented, in which the voltage from the buffer and that from the integrator are multiplied using an analog voltage multiplier.

The memcapacitor emulator conducting the operation in

Fig. 2 has been designed with commercially available devices as shown Fig. 3. The devices employed for the circuit are OPAMPs (TL082CP), a resistor, capacitors, a diode (D1N4148), and a voltage multiplier (MLT04GP).

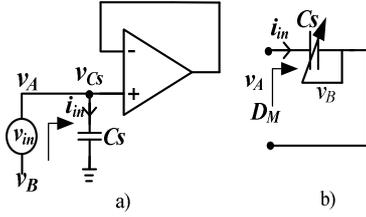


Fig. 2. Basic concept of memcapacitor emulator. (a) Inverse of memcapacitance as function of voltage  $v_B$ . (b) Equivalent circuit.

In the circuit, the capacitor  $C_S$  produces a voltage  $v_{CS}$  with the integration of the current  $i$ .

$$v_A = v_{CS} = \frac{1}{C_S} \int i(t) dt = \frac{q(t)}{C_S}. \quad (18)$$

Also, the same voltage is obtained at the output terminal of  $v_{U1}$ .

The current through  $R_I$  is

$$i_{R1} = \frac{q(t)}{R_1 C_S}. \quad (19)$$

The output voltage  $v_{U2}$  across the integral circuit is

$$v_{U2} = -\frac{1}{C_1} \int i_{R1} dt = -\frac{\int q(t) dt}{R_1 C_1 C_S}, \quad (20)$$

where the negative voltage comes with the diode implemented across  $C_1$ . The Diode DIN4148 is for keeping the output of the integrator to have negative values. For the proper operation of the proposed memcapacitor, the output of the integrator should be varied only in negative region. However, leakage current in the circuit could have the output of integrator get into positive region undesirably. Whenever the output of integrator gets into positive region, the diode is in forward biased and the output of the integrator becomes zero volts. Thus, the output of the integrator always stays in negative region.

An analog voltage multiplication is performed between the voltages  $v_{U1}$  and  $v_{U2}$  as

$$v_B = \frac{v_{U1} \times v_{U2}}{2.5} = -Kq(t) \int q(t) dt, \quad (21)$$

$$\text{where } K = \frac{1}{2.5 R_1 C_1 C_S^2}.$$

From (18) and (21), the expression of input voltage  $v_{in}$  is

$$v_{in} = v_{AB} = v_A - v_B = \left( \frac{1}{C_S} + K \int q(t) dt \right) q(t). \quad (22)$$

Observe that equation (22) describes the operation of the memcapacitor in (14) and (17). Thus, the circuit in Fig. 3 is

confirmed to be a memcapacitor circuit, in which the inverse of memcapacitance is

$$D_M = C_M^{-1} = \left( \frac{1}{C_S} + K \int q(t) dt \right). \quad (23)$$

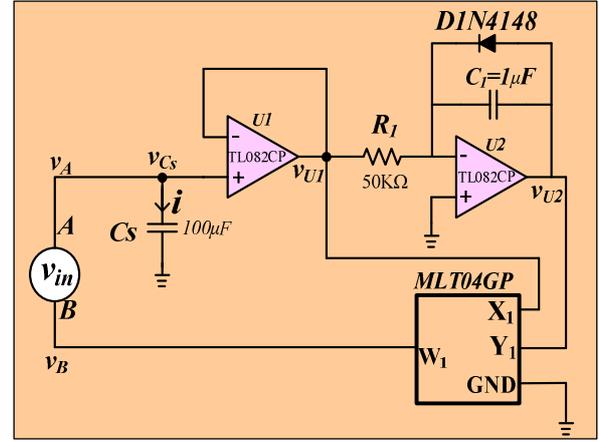


Fig. 3. Schematic of the proposed architecture of the memcapacitor emulator with off-the-shelf devices.

Note that the circuit of Fig. 3 is a simple dedicated architecture without a mutator.

#### IV. EXPERIMENTAL RESULTS

The proposed architecture of the memcapacitor emulator has been implemented on a breadboard with off-the-shelf electronic devices, and proper operation has been verified via comparisons with the results of PSPICE simulations. The parameters used for this circuit are  $\pm 5$  V power,  $C_S = 100 \mu\text{F}$ ,  $R_1 = 50 \text{ K}\Omega$ , and  $C_1 = 1 \mu\text{F}$ .

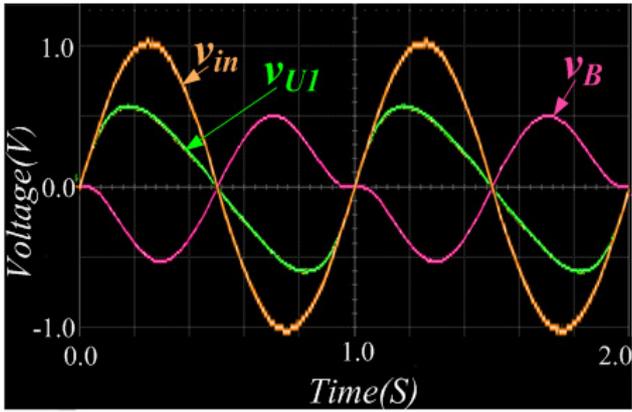
Figure 4(a) shows experimental results measured on the breadboard circuit at the input terminal  $v_{in}$ , buffer output  $v_{U1}$ , and multiplier output voltage  $v_B$  at 1 V sinusoidal signal with 1 Hz frequency. Figure 4(b) is the oscilloscope display of a pinched hysteresis loop measured from the memcapacitor emulator.

The PSPICE simulation is performed to measure the voltage across different nodes of the memcapacitor emulator. The input is sinusoidal source with 1 V amplitude and 1 Hz frequency. The waveforms of the input voltage ( $v_{in}$ ), the buffer output voltage ( $v_{U1}$ ), integrator output voltage ( $v_{U2}$ ) and the corresponding multiplier output ( $v_B$ ) are shown in Fig. 5.

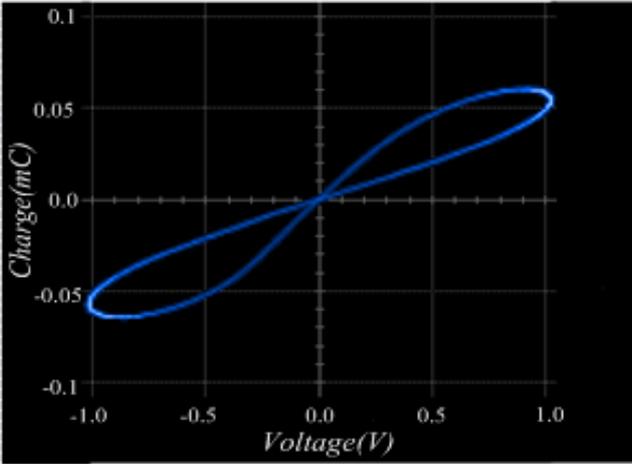
Figure 6 shows PSPICE simulations results, when the memcapacitor emulator is driven by sinusoidal source with 1 V and 1 Hz frequency. The flux curve is obtained by integrating the input source which has a similar integrator as  $U2$ . Similarly, the charge curve is obtained at node  $v_{U2}$ .

Since the voltage across  $v_{U2}$  is  $-\frac{\int q(t) dt}{R_1 C_1 C_S}$ , the actual charge

in *Coulomb* is obtained by multiplying the voltage of  $v_{U2}$  by  $-R_1 C_1 C_S$ . The input voltage, flux and charge measured across the proposed memcapacitor emulator are shown in Fig. 6(a) with respect to time axis. The corresponding variation of the flux with respect to charge is shown in Fig. 6(b).



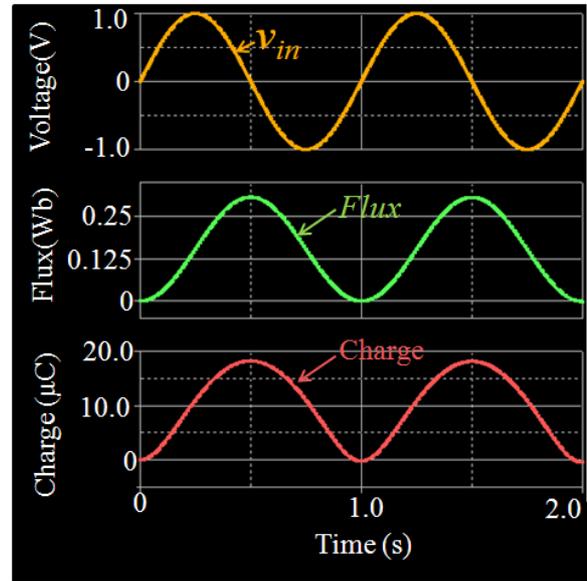
a)



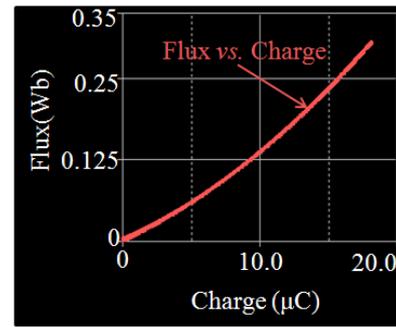
b)

Fig. 4. Experimental results from the hardware memcapacitor emulator. (a) Voltage waveforms measured at several nodes of the hardware circuit. (b) Oscilloscope trace of the pinched hysteresis loop of hardware memcapacitor emulator at 1 Hz.

when input signals of 1 Hz, 2 Hz, 5 Hz, 10 Hz, and 25 Hz with 1 V sinusoidal signals are applied to the hardware circuit.



a)



b)

Fig. 6. (a) Waveforms of the input voltage, flux and charge of the memcapacitor emulator for input voltage  $v_{in} = A \sin(2\pi ft)$  with amplitude  $A=1$  V and frequency  $f=1$  Hz. (b) The corresponding variation of the flux with respect to the charge.

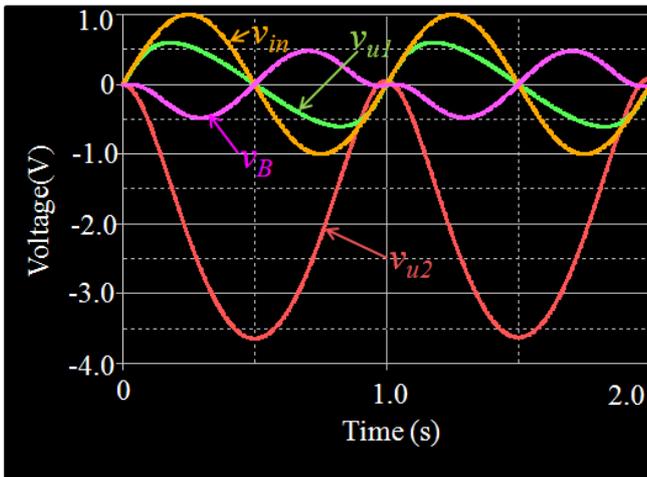
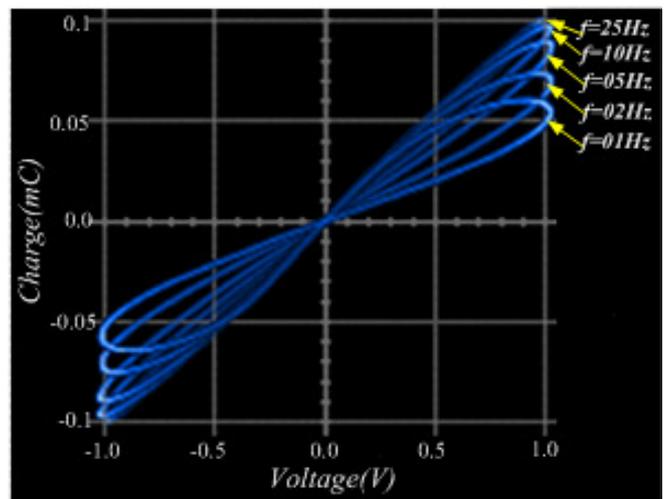


Fig. 5. Waveforms of the input voltage ( $v_{in}$ ), the buffer output voltage ( $v_{U1}$ ), integrator output voltage ( $v_{U2}$ ) and the corresponding multiplier output ( $v_B$ ) of the proposed memcapacitor emulator.

Experiments for the frequency dependency of the pinched hysteresis loops, which is the fingerprints of memcapacitors, have also been performed. Figure 7(a) shows the results



a)

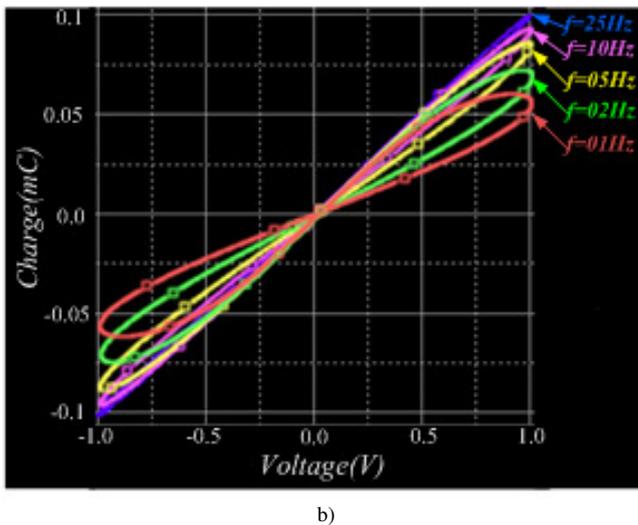


Fig. 7. Pinched hysteresis loops obtained with the proposed memcapacitor emulator circuit for various frequencies. (a) Hardware experimental results. (b) PSPICE simulation results.

Observe that the widths of the pinched hysteresis loops are shrunken as the frequency becomes higher. Figure 7(b) also shows the results of PSPICE simulations, which are similar to the hardware experimental results.

## V. CONCLUSIONS

We proposed a new memcapacitor emulator architecture which is useful for circuit applications. The proposed circuit has a dedicated architecture for the memcapacitor emulator, in which mutators are not employed. The circuit has been implemented with off-the-shelf devices, and the operation has been verified to be very close to PSPICE simulation result. Since the proposed architecture has no mutators, the architecture is simple, and can be applied for design applications of complicated memcapacitor circuits.

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