

# A Low Power 3-Stage Voltage-Controlled Ring Oscillator in 0.18 $\mu\text{m}$ CMOS Process for Active RFID Transponder

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**Abstract**—This paper presents a 3-stage ring voltage-controlled oscillator (RVCO), designed for active Radio Frequency Identification (RFID) transponders. High frequency local oscillators designed for battery-powered transponders are always crucial concerns for chip designers, as those oscillators consume considerable amount of power. Thus, the primary goal of this research work is to design a low power VCO at 2.45 GHz in the ISM band. In addition, in order to reduce overall oscillator size, ring based architecture has been adopted with easy integration technique. For varying the oscillating frequency from 2.2 GHz to 2.85 GHz, PMOS transistors with fixed value capacitors are utilized. Providing 1.8 V supply, the oscillator dissipates 6.99 mW of power and exhibits phase noise of -112 dBc/Hz at 10 MHz offset. The proposed RVCO is designed in CEDEC 0.18  $\mu\text{m}$  standard CMOS process using Mentor Graphics environment.

**Index Terms**—CMOS, differential, ring, VCO.

## I. INTRODUCTION

The Radio Frequency Identification (RFID) system is among several recent technological inventions, which is used widely in applications such as supply chain, public transportation and biomedical industry. This smart identification system usually comprises of one or several readers, which communicate with many transponders (tags) simultaneously. The operating frequency ranges of recent RFID systems established for international standards extend from 135 KHz to 2.45 GHz [1]. In the RFID system, tags can be categorized into two types: passive and active [2]. These types are devised based on power sources. Passive tags do not need power source on-board. These tags use the magnetic field of the readers as a source of energy and thus, communicate with the readers. On the other hand, active tags are battery-powered devices that have an active transmitter on-board. Unlike passive tags, active tags generate RF energy by themselves and this autonomy from the reader means that they can communicate at long distances

dissipating more power than their passive counterparts.

In an analog transceiver of active RFID tag, one of the key blocks is the frequency synthesizer or local oscillator, which is formed typically by using phase-locked loop (PLL) Every PLL is usually composed of a phase detector, a low pass filter, a VCO and a frequency divider as shown in Fig. 1. In this PLL-based local oscillator, voltage controlled-oscillator (VCO) is known as the most power hungry module. This module generates operating frequency for transponder and this operating frequency can be changed by varying control voltage to achieve desired tuning range.

In both wired and wireless communication systems, LC-type and ring-type of CMOS VCOs are widely used [3]. These VCOs performances are typically analyzed by low phase noise, low power dissipation, low voltage operation, high-speed oscillation, multi-phase application, supply sensitivity reduction, simplified integration method, small layout area and wide tuning range. So far, LC based VCO has the lowest level of phase noise among all CMOS VCOs [4]. Nevertheless, it has narrow tuning range, greater power dissipation and large die area [3]. In addition, it is difficult to integrate an inductor in CMOS process [5]. These shortcomings of can be overcome by ring VCO. Usually a number of delay cell or delay stage blocks are connected in a positive or regenerative feedback loop for building a ring oscillator (RO), which is the basis of ring VCO. Recently, this type of VCO has been established not only in wireless communication but also in optical communication and many more applications of the emerging ultra-wide band (UWB) and wireless sensor networks (WSNs), where wide tuning range and easy integration are required.

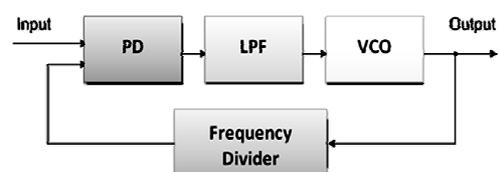


Fig. 1. Block diagram of high frequency PLL based local oscillator.

In this paper, a 3-stage ring VCO has been proposed in 0.18  $\mu\text{m}$  CMOS process designing in Design Architect-IC of

Mentor Graphics environment. The ring VCO of local oscillator will be used in the RF transceiver of active transponders. While designing the module for 2.45 GHz operating frequency, power dissipation is reduced to improve the performance of the transponder. Besides reduction of power, the tuning range and phase noise performance of the VCO are also important parameters to be improved in this research work.

## II. METHODOLOGY

The ring VCO can be implemented either by single-ended or by differential architecture of delay stages. A single-ended RVCO topology comprises of inverters and each inverter is made up of an NMOS and PMOS transistors. On the other hand, a differential topology is usually constructed by the load (active or passive) with a NMOS differential pair. In our design, we adopt differential topology, due to several reasons. Firstly, single-ended has no common-mode rejection of supply and substrate noise [6]. Secondly, it could only be formed by odd number of stages and finally, it is not possible to achieve both in-phase and quadrature outputs in single-ended ring VCO [7].

### A. Differential ring VCO architecture

For incorporation of the proposed ring VCO, only three of differential inverting amplifier stages are connected in a single delay path formation as shown in Fig. 2. Though several 2-stage ring VCO can be composed by different delay stage, extra power is certainly needed to provide an excess phase shift for oscillation fulfilling well-known Barkhausen criterion. Conversely, implementation of 4-stage ring VCO can be possible by differential topology, however, this oscillator consumes significant amount of power. Unlike 2-stage or 4-stage ring VCO, three-stage ring oscillator cannot produce quadrature outputs. Nevertheless, it is faster than its four-stage ring counterpart. Moreover, in three-stage VCO, fulfillments of proper start-up conditions can easily be attained than any even number ring VCOs, where latch-up frequently occurs. Thus, the use of 3-stage ring VCO is chosen to increase the oscillation and to reduce power consumption at the same time.

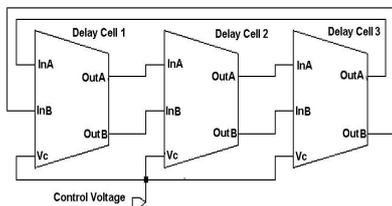


Fig. 2. Architecture of the three-stage ring VCO.

The principle operation of ring oscillator is if one of the nodes is excited, the pulse will propagate through all the stages and will reverse the polarity of the initially excited node. For start-up and oscillation criteria, the transfer function for this three-stage ring oscillator with the number of stages set to 3 can be represented as

$$H(S) = \frac{-A_0^3}{\left(1 + \frac{S}{\omega_0}\right)^3}, \quad (1)$$

where  $A_0$  denotes voltage gain of each delay stage and  $\omega_0$  denotes 3 dB bandwidth at each stage.

As one of the Barkhausen criteria for oscillation is a phase shift of  $180^\circ$ , i.e., each stage contributes with  $60^\circ$  of phase shift, the frequency at which it occurs given as

$$\omega_{osc} = \omega_0 \cdot \tan\left(\frac{180^\circ}{N}\right). \quad (2)$$

The other criterion for oscillation is a loop gain greater than 1 at  $\omega_{osc}$ . Thus, the minimum voltage gain per delay stage has been calculated by inserting the oscillation frequency expression of (2) into the gain equation found from (1). The result yields the minimum voltage gain of 2 (two) for each delay stage.

For every signal cycle, there is a downward as well as an upward transition. Since the high-to-low ( $t_{pHL}$ ) and low-to-high ( $t_{pLH}$ ) propagation delays associated with these transitions are not usually equal, the average propagation delay is given by

$$T = \frac{(t_{pHL} + t_{pLH})}{2}. \quad (3)$$

The oscillation frequency for an  $N$ -stage ring is derived from the average propagation delay ( $T$ ) of the inverter. A propagating signal will have to pass twice through the chain of delay stages, for a total delay of  $2NT$ , to complete one period. Thus, the frequency of the oscillation ( $f$ ) is expressed as

$$f = \frac{1}{2NT}. \quad (4)$$

### B. Proposed differential delay stage topology

In this research work, a new delay stage configuration for the ring VCO has been proposed as shown in Fig. 3. In CMOS integrated circuits (ICs), fully (true) differential and pseudo-differential (PD) are the two main configurations that are used extensively [8], [9]. The proposed delay stage topology is preferred as it alleviates necessity of tail current transistor, which causes flicker noise in the true-differential circuit [8]. Additionally, it improves output voltage stability without redundant bias circuit occupying a large area in the chip [9].

A pair of CMOS differential push-pull inverter is used as inputs in the new delay stage architecture. This push-pull inverter consists of two different sizing of PMOS and NMOS. Additionally, two cross-coupled PMOS transistors are connected in parallel with inverters PMOS transistors. These cross-coupled PMOS transistors are applied for fast switching speed. All four PMOS in the stage are of equal size to ensure smooth oscillation. In addition, a serially connected PMOS with a load capacitor of 0.1 pF is employed in parallel with each NMOS input for frequency tuning.

The operation of the delay cell can be described considering half-cell circuit. While the input node of  $InA$  goes high (near VDD), another input node of  $InB$  becomes low (equal to 0 V). This voltage transition turns on M1 of

the node *InA* and voltage of the output node, *OutA* becomes grounded.

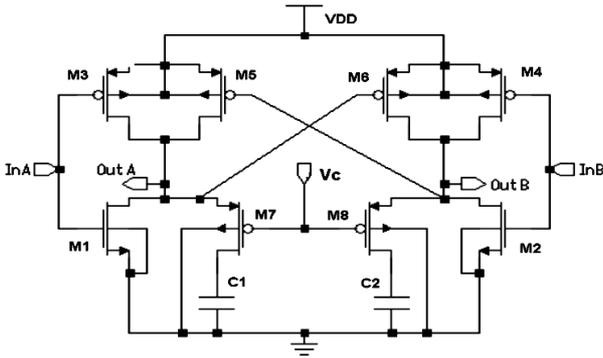


Fig. 3. Schematic of the proposed delay stage.

Due to this transition, the capacitor (C1) discharges initially stored charge of it, or in other words, a discharge path is formed sinking current from the node, *OutA*. Conversely, M3 of the node, *InA* and M5 connected with it remains off during this time. Again, if the node *InA* turns into 0 V, then another differential input node, *InB* becomes high. Then zero potential (0 V) at the node, *InA* turns on M3 and turn off M1 simultaneously. M5 connected in parallel with M3 of *InA* also remains switched on at this time. Thus, the discharged capacitor is recharged again through these PMOS transistors. In both operations of the whole circuit, a pair of PMOS tuning transistors (M7 and M8) controls the overall charging and discharging of fixed capacitors (C1 and C2) by varying voltage.

### III. RESULTS AND DISCUSSIONS

The proposed delay stage circuit has been verified by using the Eldo RF simulator of Mentor Graphics and the process parameters for the transistors used in this work correspond to Collaborative Micro-electronic Design Excellence Centre (CEDEC) 0.18  $\mu\text{m}$  standard CMOS process. To determine the center frequency of the proposed RVCO, the post-layout simulated output of the ring is shown in Fig. 4. If the control voltage is set to 0.12 V, frequency of 2.45 GHz is achieved at 27<sup>o</sup> C.

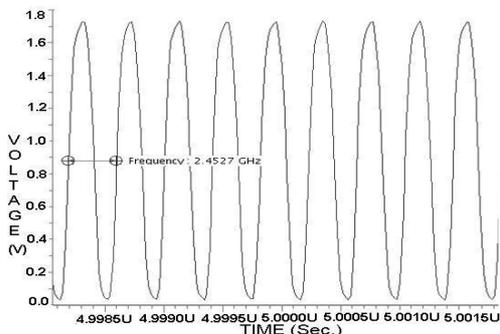


Fig. 4. Output frequency of the proposed ring VCO.

This RVCO tunes linearly from 2.36 GHz to 2.85 GHz with a tuning voltage range of 0 V to 1.1 V. In order to validate the proposed circuit in wide frequency range, a simulation is done at different control voltages as shown in Fig. 5. This figure shows that if the control voltage is set to 0 V, the proposed circuit is able to work in 2.36 GHz

frequency. When this VCO's control voltage is increased to 1.1 V, the circuit oscillates in 2.85 GHz frequency. Since IEEE 802.11b protocol requires operating frequency from 2.4 GHz to 2.48 GHz, the proposed ring VCO works reliably on this frequency range. The tuning range could also be varied in different temperature values of 10<sup>o</sup> C, 27<sup>o</sup> C, 70<sup>o</sup> C and 10<sup>o</sup> C as shown in Fig. 5.

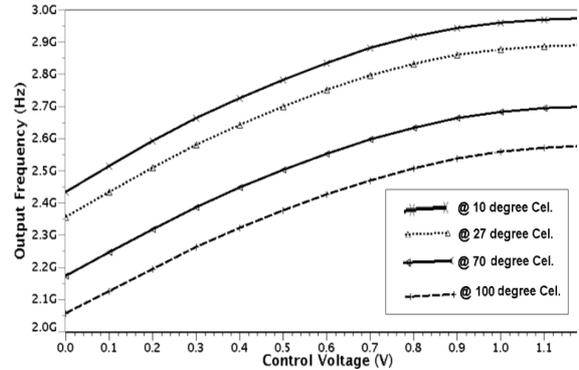


Fig. 5. Tuning range vs. control voltage at different temperature.

In this design, different sizing of transistors are calculated by taking into account the optimization of power consumption and phase noise. The designed RVCO typically draws 3.88 mA of current from 1.8 V supply at 27<sup>o</sup> C. The oscillator's power dissipation is 6.99 mW and is simulated single side-band (SSB) phase noise (PN) of -112 dBc/Hz at 10 MHz offset from 2.45 GHz as shown in Fig. 6.

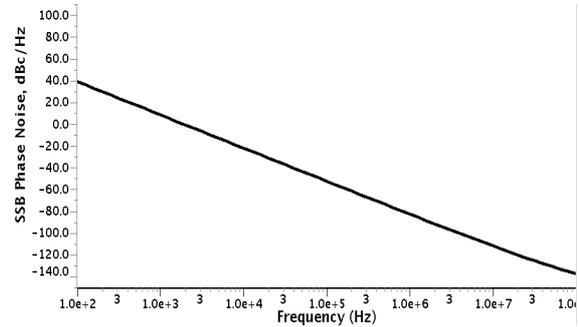


Fig. 6. Single side-band (SSB) phase noise (PN) of proposed RVCO.

Provided in [4], the figure of merit (FOM) of the proposed RVCO can be calculated from the power dissipation and the phase noise of the simulated oscillation frequency as

$$FOM_{dB} = L(\Delta\omega) + 10 \log\left(\frac{power_{DC}}{1mW}\right) - 20 \log\left(\frac{\omega_0}{\Delta\omega}\right), \quad (5)$$

where  $L(\Delta\omega)$  is phase noise in  $\Delta\omega$  offset frequency and  $\omega_0$  is the frequency of oscillation of the RVCO. The achievable figure of merit (FOM) is determined - 151.34 dBc/Hz. The area of the core layout (without pads) is 97.65  $\mu\text{m} \times 33.15 \mu\text{m}$  as shown in Fig. 7.

Finally, the performance comparisons of RVCOs of CMOS technologies are shown in Table I. Compared to other research works, it is observed that the proposed RVCO dissipates lowest power, which is around 6.99 mW, though it operates in very high frequencies than [8]–[10]. However,

the designed oscillator's phase noise performance degrades a little, as phase noise is inversely proportional to power consumption of the signal [6] (Note: relation between phase noise and signal power can be found in the Appendix at the end of this paper). Moreover, our design achieves higher value of figure of merit (FOM) in expense of optimum power than [9], [10], which is designed higher frequency to those of the RVCO presented in this paper. The proposed design's power consumption is significantly lower than [9] and wide tuning range is notable as well.

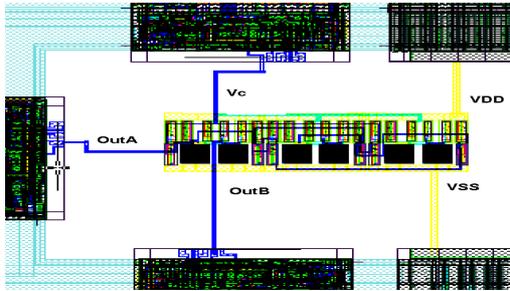


Fig. 7. Layout of differential RVCO.

TABLE I. THE PERFORMANCE COMPARISONS OF CMOS RVCO

Architecture	Center Freq. (GHz)	Tuning Range (GHz)	Phase noise (dBc/Hz)@ Offset (MHz)	Supply Voltage (V)	Power (mW) or current (mA)	FOM (dBc/Hz)	CMOS Process ( $\mu\text{m}$ )
2 stage, Single delay loop [10]	0.9	0.73-1.43	-106.1 @0.6	1.8	65.5 mW	-151.45	0.18
4-stage, Dual delay loop [11]	—	1.77-1.92	-123.4 @10	1.8	13 mW	—	0.18
3-stage, Single Delay loop [12]	0.866	0.381-1.15	-126 @10	3.3	7.48 mW	-156	0.35
4-Stage, Single-delay loop [9]	3.125	18%	-91 @1	1.8	12.6 mW	-149.1	0.18
3-stage, Single delay loop [This work]	2.45	2.36-2.85	-112 @10	1.8	6.99 mW	-151.34	0.18

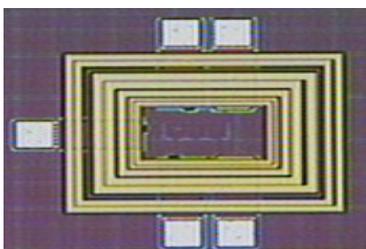


Fig. 8. Die microphotograph of the ring VCO's prototype.

Since the ring VCO was sent for fabrication, a microphotograph of the prototype, fabricated using standard  $0.18 \mu\text{m}$  CMOS process is shown in Fig. 8. The chip includes pads without the buffer circuits. In fact, the buffers were designed at the outputs of the VCO to magnify and regulate the output signal of the front circuit. Meanwhile, they provide a large enough current and voltage to drive the follow-up circuit. The future research work will be focused on realizing the measurement of the RVCO circuit performances and we will compare them with those obtained

from post-layout simulations. Thus, measurement results of the complete RF PLL's die will be published in a further work.

#### IV. CONCLUSIONS

In this paper, a 3-stage ring VCO has been proposed for active RFID transponder. The post-layout simulated results show that its operating frequency is 2.45 GHz and it is able to work with IEEE 802.11b protocol for low data rate RFID applications due to its tuning range coverage. Moreover, its convincing performances prove to be suitable for low power RF sensors and handy wireless devices.

#### APPENDIX A

Classical oscillator's phase noise equation given by Leeson is as follows

$$L\{\Delta\omega\} = 10 \log\left[\frac{2FKT}{P_{DC}}\left(1 + \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right)\left(1 + \frac{\omega_0}{\Delta\omega}\right)\right]. \quad (6)$$

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