Methods for Extension of Tunability Range in Synthetic Inductance Simulators

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Abstract—Presented work focuses on methods for the extended electronic control in the designs of inductance simulators based on single-loop feedback topology. Implementation is based on diamond transistors as voltage-to-current converters and two voltage-mode multipliers connected to different positions in topology (providing amplification or control of equivalent resistance). Presented solutions achieve significantly extended adjustability of equivalent inductance value in comparison to standard approaches based on CMOS differential pair-based operational transconductance amplifiers. Proposed designs of synthetic inductors are based on utilization of integer-order as well as fractional-order (constant phase element) capacitor. Their features are verified both via PSpice simulations and experimental measurements. Results confirmed intended purposes of designs implementing discussed methods.

Index Terms—Adjustability extension; Constant phase element; Diamond transistor; Electronic control; Fractional-order inductance simulator; Integer-order inductance simulator; Tunability extension; Voltage-mode multiplier.

I. INTRODUCTION

Inductance simulators are very useful active building blocks for many various analogue systems [1], [2]. Their utilization is welcomed because they can replace standard metallic coils (heavy, bulky, expensive, unsuitable for low-frequency applications) in signal processing circuits as well as due to their simple electronic controllability (that is practically impossible in metallic form). Various active elements [1], [3] are used in the design of inductance simulator. Operational transconductance amplifiers (OTAs) [1]–[6] are very beneficial in applications of immittance conversion [5], [7] and multiplication [7]. As we know, diamond transistor (DT) OPA860 [8] is frequently used as OTA, when base (B) serves as high-impedance input and collector (C) as high-impedance current output, and emitter (E) is connected to ground through so-called degradation resistor, which sets value of transconductance ($g_m = 1/R_{dc}$) [9]. This connection can be also explained by an alternative way as second-generation current conveyor (CCII) [1] having connected current input terminal X to ground through resistor $R_{dc}$, high-impedance voltage input Y serves as input and high-impedance terminal Z represents current output (typical inter-terminal relations are: $I_Y = 0$, $V_X = V_Y$, $I_Z = I_X$) [9]. However, lack of electronic adjustability of commercially available CCIIIs (AD844 for example) results in logical question: How circuits consisting these active elements should be electronically controlled? This is very important, because electronic controllability is one of the emerging issue expected from modern electronic circuits as subparts of communication systems. Several possible integrated OTAs, controllable by bias current, are available on the market (LM13700, LT1228). However, their dynamics and linearity as well as frequency features are not favorable for designs operating at hundreds of kHz and beyond in comparison to DT and high-speed multiplier (MLT), for example AD835 [10].

In this work, electronic control of immittance converter/inductance simulator based on two diamond transistors in single loop are analysed. Controllability of the parameters of the device is based on control of parameters of two voltage-mode multipliers included to the topology in several places. These two multipliers are employed in order to extend the tunability range. Extended range of control is observed in three cases. The following section explains the reasons and motivation for this work. Afterwards, all circuits are analysed in case of integer-order operational mode and also example of fractional-order operation is shown. The conclusion summarises gained findings and suggests further works on this topic.

II. MOTIVATION

Figure 1 shows standard topology serving for impedance transformation and inversion, i.e. for design of synthetic inductance simulator as discussed for example in [5], where OTAs were employed as active elements in the loop. However, effectivity of $g_m$ driving by bias current ($I_{bias}$) in controllable applications is quite limited because of the
nonlinear (square root) dependence of \( g_{m1} \) on \( I_{bias} \) [4]-[5] (valid for CMOS solution). Bipolar solution of OTA has linear dependence of \( g_{m1} \) on \( I_{bias} \) [11], which extends tunability range, theoretically. However, in both cases (bipolar or CMOS), input dynamics and linearity is very limited. Therefore, better active elements (linear and having wider dynamics) than differential pair based OTAs should be considered for these purposes. Moreover, more effective methods of controllability can be developed and introduced for purposes of tunability extension. In CMOS implementation of OTAs, considering solution shown in Fig. 1, equivalent inductance value \( L_{eq} \) is given by

\[
Z_{inp}(s) = \frac{sC}{sC} = \frac{sC}{kI_{bias}I_{bias2}} \approx \frac{sC}{kI_{bias}I_{bias2}} = \frac{1}{R_{deg1,2}},
\]

where \( L_{eq} \) depends on both bias currents.

\[ Z_{inp}(s) = \frac{sC}{sC} \approx \frac{sC}{kI_{bias}I_{bias2}} \approx \frac{1}{R_{deg1,2}}, \] (1)

Fig. 1. Standard topology of synthetic inductance simulator based on two OTAs [5] or diamond transistors (alternative realization).

III. METHODS FOR TUNABILITY RANGE EXTENSION

The following text deals with three investigated methods of tunability extension (targeted on special cases of dependence of \( L_{eq} \) value on driving force) in feedback topology of two diamond transistors. In comparison to differential pair-based OTAs, diamond transistors do not allow electronic control of transconductance value \( (g_{m}) \). Fortunately, other possibilities of electronic control in the topology (Fig. 1) can be added and bring certain advantages for designers as presented below.

A. Single Adjustable Voltage Gain in the Loop Driven by Square of Control Voltage

The first proposed solution shown in Fig. 2 includes two diamond transistors and two multipliers. The first multiplier serves as amplifier and the second as a squarer of DC driving voltage \( V_{set} \). The square of driving voltage \( V_{set} \) serves as part of multiplication constant directly creating the gain of the block between \( C \) of DT1 and \( B \) of DT2. Voltage gain created by MLTs has definition \( |A_1| = 4V_{y2} \) (explanation of MLT operation is provided later). Then the gain reaches dependence on \( V_{set} \) as: \( |A_1| = 4(4V_{set})^2 \) as clear from interconnection in Fig. 2. The relation for input impedance has a form (valid for integer-order capacitor)

\[
Z_{inp}(s) = \frac{sC R_2 R_2}{A_1} \approx \frac{sC R_2^2}{A_1} \approx \frac{sC R_2^2}{16(V_{set})^2}. \] (2)

Polarity of \( L_{eq} \) can be easily modified by interchange of terminals \( y_1, y_2 \) of MLT1. However, special attention must be given to possible risk of instability and output saturation when polarity of the closed loop is positive. Advantage of presented approach consists in minimized negative impact of increasing number of active elements on the circuitry (MLT2 is not influencing frequency features, it operates with DC signal).

B. Cascade of Two Adjustable Voltage Gains in the Loop

Another solution is to cascade two MLTs in operation of controllable amplifiers, see Fig. 3. It creates very similar effect when compared to solution from Fig. 2. However, both MLTs are members of feedback loop, therefore their frequency features influence overall behaviour of the circuit. Both voltage gains \( A_1 \) and \( A_2 \) depend on \( V_{set} \) as shown in previous text \((|A_1,2| = 4V_{set,1,2})\), therefore, also final equation for input impedance depending on \( V_{set} \) is

\[
Z_{inp}(s) = \frac{sC R_2 R_2}{A_1 A_2} = \frac{sC R_2^2}{A_2} \approx \frac{sC R_2^2}{16(V_{set})^2}. \] (3)

The polarity of \( L_{eq} \) can be turned by interchange of \( y_1 \) and \( y_2 \) connection in MLT1 or MLT2 (DC control by \( V_{set} \)) or by swap of input terminals \( x_1, x_2 \) of MLT2. Again, special attention must be given to stability issues when loop transfer turns to positive.

C. Inversely Proportional Adjustable Resistors

The last studied solution (Fig. 4) supposes two adjustable resistors, but dependence of equivalent resistances on DC control voltage \( V_{set} \) is now inversely proportional:
In addition, clear restriction \( A_{1.2} < 1 \) \((0 \leq V_{\text{set},2} < 0.25 \text{ V})\) arises from definition of this concept. Input impedance is defined as follows

\[
Z_{\text{imp}}(s) = \frac{sCR_{2}}{(1-A_{1})(1-A_{2})} = \frac{sCR^{2}}{(1-A)^{2}} \approx \frac{sCR^{2}}{(1-4V_{\text{set}})^{2}}.
\]

(4)

IV. VERIFICATION

We verified basic features of all previously presented concepts by PSpiCe simulations. Solution in Fig. 2 was also tested experimentally. Verification focuses on integer-order (implementation of standard capacitor) as well as fractional-order behaviour (implementation of constant phase element (CPE) as discussed later). The voltage-mode multiplier AD835 [10] arranged for intended purposes in developed topologies is shown in Fig. 5. Note that the value of multiplication constant \( m = (R_{1} + R_{2})/R_{2} \) has been set to \( 4 \) in order to achieve \( |A_{\text{max}}| = 4 \). All cases of inductance simulators having extended tunability of parameters were tested by PSpiCe simulations when the following parameters were set as constant: \( R_{1} = R_{2} = R = 91 \Omega \) (overall value \( R_{31.2} = R_{1.2} + R_{3.1.2} = 102 \Omega \), i.e. sum of external \( R_{1.2} \) and internal \( R_{31.2} \) resistance 11 \( \Omega \) of DT at E terminal [8]).

Fig. 5. Voltage-mode multiplier AD835 implemented in proposed designs: a) symbol, b) circuit solution and key relation.

A. Integer-Order Behaviour

All discussed topologies were tested with standard integer-order capacitor \( C = 1 \text{ nF} \). Ideal range of \( L_{\text{eq}} \) tunability 250 \( \mu \text{H} \rightarrow 2.5 \mu\text{H} \) was expected for \( V_{\text{set}} \) adjusted from 0.05 V to 0.50 V in case of the first and second solution (Fig. 2 and Fig. 3). Magnitude and phase responses of input impedance for first (Fig. 2) solution are shown in Fig. 6. Simulations yield \( L_{\text{eq}} \) tunability 247 \( \mu\text{H} \rightarrow 3.0 \mu\text{H} \). Certain and common lossy resistive part (low value – below 5 \( \Omega \)) of input impedance occurs in simulated results.

Fig. 6. AC analysis of input impedance for the first solution (Fig. 2): a) magnitude responses; b) phase responses.

Measurements were performed with vector network analyser (VNA) E5071C. Experimental results are presented by the red colour in figures and all measured traces start from 9 kHz due to frequency limitation of used VNA (9 kHz-4.5 GHz). However, it sufficiently confirms expected behaviour. AC analysis of the second solution (Fig. 3) yields very similar results (302 \( \mu\text{H} \rightarrow 3.0 \mu\text{H} \)).

The third (last) studied topology (Fig. 4) was tested in reduced range \((0.02 \rightarrow 0.2) V_{\text{set}}\) due to above mentioned restriction \((0 \leq V_{\text{set},2} < 0.25 \text{ V})\). It results in ideal \( L_{\text{eq}} \) adjustability 12 \( \mu\text{H} \rightarrow 250 \mu\text{H} \). Simulations provided range 14 \( \mu\text{H} \rightarrow 237 \mu\text{H} \). Figure 7 and Table I introduce comparison of tunability of all solutions in comparison with standard method (proportional to 1/A, where A is controlled by \( V_{\text{set}} \) linearly).

Table I. Comparison of Proposed Methods.

<table>
<thead>
<tr>
<th>Solution</th>
<th>Range of ( V_{\text{set}} ) [V]</th>
<th>Range of ( L_{\text{eq}} ) [( \mu \text{H} )]</th>
</tr>
</thead>
<tbody>
<tr>
<td>standard</td>
<td>0.05→0.50 (10:1)</td>
<td>ideal: 50→5 (10:1)</td>
</tr>
<tr>
<td>Fig. 2 (solution 1)</td>
<td>0.05→0.50 (10:1)</td>
<td>ideal: 250→2.5 (100:1)</td>
</tr>
<tr>
<td>Fig. 3 (solution 2)</td>
<td>0.05→0.50 (10:1)</td>
<td>ideal: 250→2.5 (100:1)</td>
</tr>
<tr>
<td>Fig. 4 (solution 3)</td>
<td>0.02→0.20 (10:1)</td>
<td>ideal: 12→250 (21:1)</td>
</tr>
</tbody>
</table>

Solutions in Fig. 2 and Fig. 3 offer the largest adjustability of \( L_{\text{eq}} \). The solution from Fig. 4 is not as beneficial as obvious from comparison. On the other hand, utilization of equivalent resistance in form as in case of Fig. 4 brings also
improvement in comparison to standard method. Sensitivity and uncertainty of setting given by real behaviour causes differences of simulated and measured $L_{eq}$, for $V_{set} < 0.1$ V especially.

![Image](https://example.com/image1.png)

Fig. 7. Dependence of $L_{eq}$ on $V_{set}$: a) comparison of solutions 1, 2 (Fig. 2, Fig. 3); b) solution 3 (Fig. 4).

B. Fractional-Order Behaviour

We tested presented circuit in Fig. 2 also with so-called CPE implemented instead of standard integer-order capacitor. We used ladder structure RC designed and presented in [12] for $\alpha = 1/3$ ($\phi = 30^\circ$). Impedance of CPE (capacitance) from [12] has character $Z_{CPE}(s) = 1/(s^\alpha C_0)$, where $Z_{CPE}(s) = 118 \Omega$ (@ 100 kHz). Then $C_0$ can be calculated as $C_0 = 1/[l/(2\pi f)^n|Z_{CPE}(f)|]$. Our value reaches $C_{103} = 1/[l/(2\pi 100\cdot10^3)^{1/3}118] = 99 \mu F/sec^{3/3}$. Equivalent inductance can be calculated as $L_{eq} = C_0 R^2/(16 V_{set}^2)$ [sec$^{-1/3}$/F]. Simulated results are shown in Fig. 8, Table II, and Table III (values $|Z_{eq,0}|$ were obtained at 100 kHz). The purple trace indicates magnitude for standard $C = 1 \mu F$ ($V_{set} = 0.25$ V) for comparison purposes.

### Table II. Calculated and Simulated Eq. Inductances.

| $V_{set}$ [V] | $|Z_{eq,0}|$ [Ω] | $L_{eq} = C_0 R^2/(16 V_{set}^2)$ [sec$^{-1/3}$/F] (calculated) | $L_{eq} = C_0 R^2/(2\pi f)^{3/3}$ [sec$^{-1/3}$/F] (simulated) |
|---------------|-----------------|-------------------------------------------------|--------------------------------------------------|
| 0.05          | 2240            | 25.7                                            | 26.2                                             |
| 0.10          | 624             | 6.4                                             | 7.3                                              |
| 0.25          | 103             | 1.0                                             | 1.2                                              |
| 0.50          | 26              | 0.26                                            | 0.3                                              |

### Table III. Comparison of Simulations and Experiments.

| $V_{set}$ [V] | $|Z_{eq,0}|$ [Ω] (simulated) | $|Z_{eq,0}|$ [Ω] (measured) | $L_{eq} = C_0 R^2/(16 V_{set}^2)$ [sec$^{-1/3}$/F] (simulated) | $L_{eq} = C_0 R^2/(2\pi f)^{3/3}$ [sec$^{-1/3}$/F] (measured) |
|---------------|-----------------|-----------------|-------------------------------------------------|--------------------------------------------------|
| 0.05          | 2240            | 1122            | 26.2                                            | 13.5                                             |
| 0.10          | 624             | 704             | 7.3                                             | 8.2                                              |
| 0.25          | 103             | 114             | 1.2                                             | 1.3                                              |
| 0.50          | 26              | 27              | 0.3                                             | 0.3                                              |

V. Comparison with State-of-the-Art

Standard inductance simulator based on two OTAs has been introduced in [5] ($L_{eq}$ controlled by two $g_m$ in Fig. 1). However, issues [16] with linearity and dynamics remain (implementation of standard OTAs). Topologies focused on complex immittance synthesis were presented in [16]. However, synthesis does not suppose electronic control. Works [14], [15] introduce solutions based on single active element. The controllability of $L_{eq}$ is possible only by single $g_m$. It highly reduces adjustability ($g_m$ driven by square root of $I_{bias}$), 0.25→1 mH (4:1) in [14] for example (our cases at least 17:1 in Table I). Therefore, presented methods offer solution extending limited tunability range, see Table IV.

### Table IV. Comparison with Existing Solutions.

<table>
<thead>
<tr>
<th>Reference</th>
<th>Type of electronic control</th>
<th>No. of passive/active elements</th>
<th>Adjustability</th>
<th>Type of $L_{eq}$</th>
<th>Controllability</th>
</tr>
</thead>
<tbody>
<tr>
<td>[5]</td>
<td>$g_m$</td>
<td>1/2</td>
<td>No</td>
<td>$-1/l_{bias}$</td>
<td>hyperbolic</td>
</tr>
<tr>
<td>[13]</td>
<td>N/A</td>
<td>N/A</td>
<td>No</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>[14]</td>
<td>$g_m$</td>
<td>2/1</td>
<td>No</td>
<td>$-1/l_{bias}$</td>
<td>1/square root</td>
</tr>
<tr>
<td>[15]</td>
<td>$g_m$</td>
<td>2/1</td>
<td>No</td>
<td>$-1/l_{bias}$</td>
<td>1/square root</td>
</tr>
<tr>
<td>Fig. 2</td>
<td>A</td>
<td>3/4</td>
<td>Yes</td>
<td>$-1/V_{eq}$</td>
<td>1/quadratic</td>
</tr>
<tr>
<td>Fig. 3</td>
<td>A</td>
<td>3/4</td>
<td>Yes</td>
<td>$-1/V_{eq}$</td>
<td>1/quadratic</td>
</tr>
<tr>
<td>Fig. 4</td>
<td>A</td>
<td>3/4</td>
<td>Yes</td>
<td>$-1/(1-4/V_{eq})$</td>
<td></td>
</tr>
</tbody>
</table>

N/A – not available, $g_m$ – transconductance, $A$ – voltage gain

VI. Conclusions

Three different circuitries serving for inductance simulation allowing advanced electronic control of $L_{eq}$ have been presented. Operational range of proposed circuits in this particular configuration belongs to hundreds of Hz up to
hundreds of kHz (max. units of MHz). The first and the second solution (Fig. 2, Fig. 3) seem to be the most beneficial, but also solution from Fig. 4 offers useful extension of tunability range in comparison to standard methods. In future works we suppose further engagement of available parameters of similar active elements suitable for significant extension of the range of \( I_{\text{on}} \) adjusting. Different dependency of electronic control of parameters will be the most challenging problem in such designs.

REFERENCES


