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PLL as the Frequency Synthesizer with Continuous Phase Divider

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PLL synthesizer

The PLL (Phase Locked Loops), as it is well known [1], could be used on two ways, depending on whether the output is an error voltage, which is used for regulation of the voltage controlled oscillator (VCO), or the output is the signal itself (voltage) generated by the VCO. In the first case, it has been used for FM signal detection [2], since the error voltage has the shape of the modulating signal. The second important usage of the PLL, in frequency synthesis, has been enabled by the fact that frequency of the signal generated by the VCO is equal to the frequency of the referential signal, and its phase shift is clearly defined in relation to the phase shift of the referential signal. This kind of synthesizers with usage of just one quartz crystal and programmable (frequency) divider enables (practical) realization of highly stable frequencies [3] within a given frequency range, with the given frequency raster or step. They have been used in realization of highly stable generators of carrying frequencies at transmitters, as well as in local oscillators in radio and TV receivers.

The mostly used PLL in frequency synthesis is given in Fig.1. It consists of the following fundamental components (pieces): phase detector (FD), loop filter (NF), voltage controlled oscillator (VCO), and frequency divider (N).Afterwards the circuit synchronization the following condition is fulfilled $f_r = f_{in}$, therefore the synthesizer output frequency is

$$f_{out} = Nf_{in}\,. \tag{1}$$

If variation of f_{out} is required within a given range, then the dividing factor in the *feedback branch* N of the PLL circuit has to be changed from $N_{\min}$ to $N_{\max}$.

Although the PLL synthesizer either with variable or constant dividing module is one of the mostly used synthesizers, it has a serious disadvantage. Namely, in order to create a period of the divider's output signal, which together with referential signal in FD creates the error voltage, it is necessary n VCO periods to elapse, which means that during all this time the VCO is out of control.

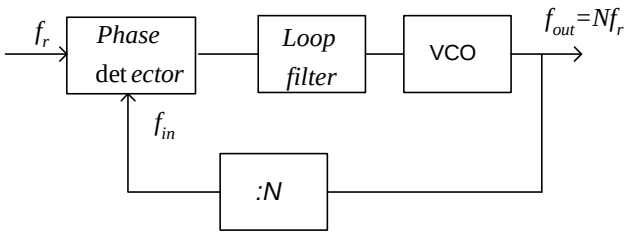

Fig. 1. Block diagram of PLL synthesizer

A solution that resolves this disadvantage is usage of look-up tables, Fig. 2.

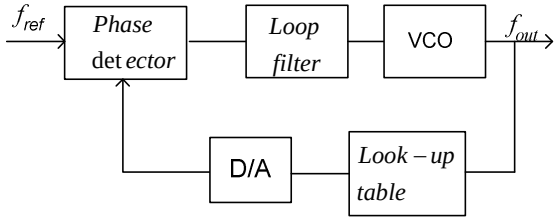

Fig. 2. PLL frequency synthesizer with look-up tables

As stated, the continuous phase divider considered here is based on look-up table. Suppose that the range of required frequencies is from $f_{\min}$ to $f_{\max}$, where

$$f_{\min} = N_{\min} f_{ref}\,, \quad f_{\max} = N_{\max} f_{ref}\,. \tag{2}$$

The look-up tables, Fig.2. store $N_{\max} - N_{\min}$ vectors of numbers, where each vector belongs to one of the required frequencies. The length of vector which belongs to the frequency $f = Nf_{ref}$ is

$$n = N/p \quad (p = 1,2,...,N/2) \tag{3}$$

and it contains m samples of one period of the reference signal. After m periods of the VCO, the process is

repeated, and thus the phase of the VCO is divided almost continuously by N. Obviously, for the case when $p=1$ $(n=N)$, the obtained approximation is the best one**.**

A typical solution for resolving this problem is usage of look-in tables [4], in which are memorized samples of the sinusoidal function with n discrete values, while the number of discrete values is equal to the wanted module of the divider. One discrete value is read from the memory in every VCO period, afterwards it is sent to the D/A converter and then to the phase detector where together with referential voltage gives the regulating (control) voltage influencing VCO [4]. Subsequently, loop reaches the stable state faster (for less period of time), and it remains under control of the phase detector all the time by the end of the stable state.

In this paper, a hardware solution for generating sinusoidal function in samples instead of the look-in tables and D/A converters is proposed [5], on this way all advantages of the synthesis given in [4] are kept (preserved). The proposed solution is suitable for integration, resulting in the new integrated PLL synthesizer.

Realization of the divider as a sinusoidal waveform generator

The operational amplifier gain as well as the descrete sinusoidal function, i.e. $\sin(2\pi f_0 \Delta t k)$, are regulated by resistors [2], where k is the serial number of the sample within a VCO period, and Δt is duration of a sample. Variable gain of the operational amplifier is attained by a set of resistors, whereby only one of the resistors is switched on in the circuit at a moment of time, and stays switched on for the period of time Δt. The resistors are switched on by a switch (chopper), and their operation is controlled by the control logic

$$u_2(t) = A\sin(2\pi f_0 t)U_1 \ . \qquad (4)$$

Discretization of this function is performed on the way that $k\Delta t$ is introduced instead of t, where k is the serial number of the sample, on that way the signal in the descrete number of points is obtained i.e.

$$u_2(t) = A\sin k\Delta\theta U_1, \qquad (5)$$

where

$$\Delta\theta = 2\pi f_0 \Delta t \ , \ \Delta t = \frac{1}{n f_0} \ .$$

Realization of (5) could be performed by the circuit given in Fig. 3. The output signal of this circuit is

$$U_2 = AU_1 = \frac{R}{R_k}U_1, k = 1,2...n \ . \qquad (6)$$

If we suppose that U_1 is a constant voltage equal to one $(U_1 = 1)$, then

$$U_2 = \frac{R}{R_k}, k = 1,2...n \ , \qquad (7)$$

where R_k is the serial number of the resistor which is switched on in the curcuit. The negative half-period of the sinusoudal function is achived by an AND circuit, i.e. by the input signal of the opposite polarity.

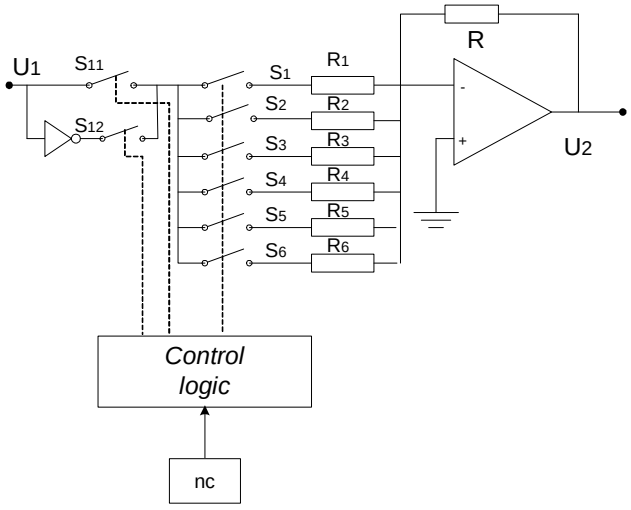

Fig. 3. The network of resistors for realization of a discrete signal

Table 1. Values of resistors

$\theta_k[^0]$	$\sin\theta_k$	$R_k[k\Omega]$	R_1	R_2	R_3	R_4	R_5	R_6
7.5	0.130	76.923	1	0	0	0	0	0
22.5	0.383	26.110	0	1	0	0	0	0
37.5	0.608	16.447	0	0	1	0	0	0
52.5	0.793	12.610	0	0	0	1	0	0
67.5	0.924	10.882	0	0	0	0	1	0
82.5	0.991	10.091	0	0	0	0	0	1
97.5	0.991	10.091	0	0	0	0	0	1
112.5	0.793	10.822	0	0	0	0	1	0
127.5	0.793	12.610	0	0	0	1	0	0
142.5	0.608	16.447	0	0	1	0	0	0
157.5	0.383	26.110	0	1	0	0	0	0
172.5	0.130	76.923	1	0	0	0	0	0

Values of the resistors R_k from the previous expressions are:

$$R_k = \frac{R}{\sin(k\Delta\theta)}, k = 1,2...n \ , \qquad (8)$$

where $\Delta\theta = \frac{360^\circ}{n}$ and n – the number of points in which discretization of the function is performed. In Table 1 value "1" means that the resistor is switched on, while "0" means that the resistor is switched off.

The new PLL synthesizer

The new PLL frequency synthesizer with the continuous phase divider is shown in Fig. 4. The output signal from the voltage controlled oscillator is used for

triggering of the sinusoidal waveform generator in which n samples of the sinusoidal waveform are actually generated, whereby n is the number of discrete points equal to the dividing module. By this realization, one sampled value of the sinusoidal function is generated within every VCO period and sent to the phase detector. This allows presence of the both signals in the phase detector starting from the first VCO oscillation period, which subsequently causes faster reaching of the stable state. Additionally, the system is permanently controlled by the voltage from the phase detector.

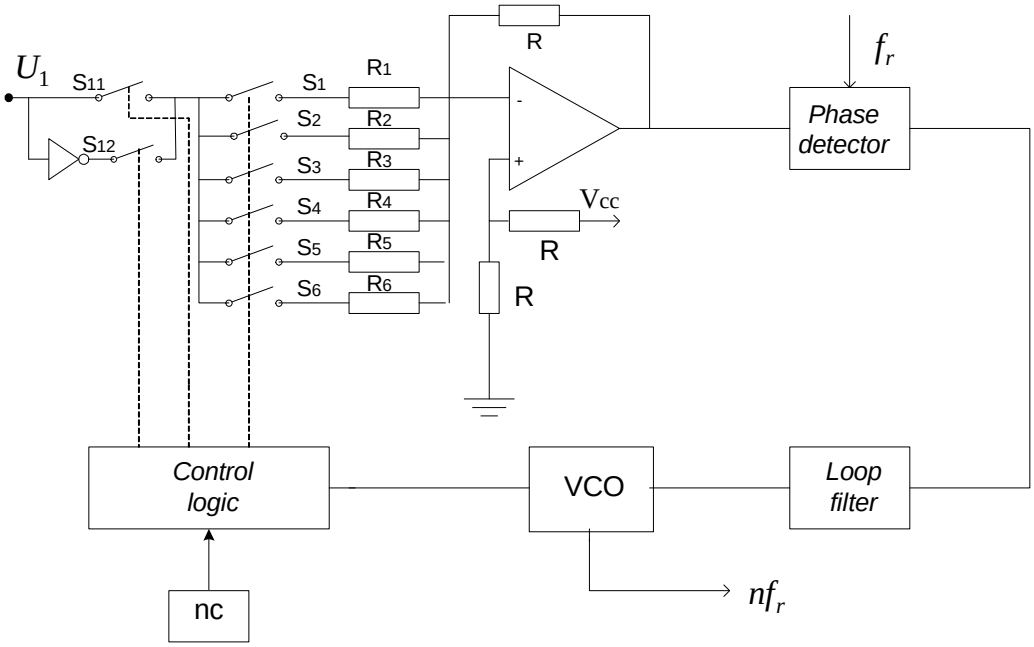

Fig. 4. The new PLL synthesizer

In the real implementation, variation of the operational amplifier gain has to be realized by progressive turning switches (choppers) on from the first one to the last one. In Table 2. are given values for θ_k, and $\sin\theta_k$, as well as values of the resistors needed for generating of the resistor network output signal, based on samples, in the case that discretization of the sinusoidal function is performed in 24 points, which subsequently means $n = 24$ and $\Delta\theta = 15^\circ$.

By (9), and for $R = 10k\Omega$, value of the resitor R_k is calculated. That resistor is turned on in the circuit within the period of time Δt and refers to the $k-th$ sample of the discretized sinusoidal function. On this way, discrete values of the sinusoidal function are realized for a quarter of the half-period $(0-\pi/2)$. For the second quarter of the half-period $(\pi/2-\pi)$ the switches has to be progressively turned off from the last one to the first one. The negative half-period is realized by repeating the previous procedure with turning the switch S_{12} on, whereby the input DC voltage U_1 is now inverted, i.e. negative. This procedure reduces glitch magnitudes in the waveform of the output signal comparing to the solution where a certain discrete value of the sinusoidal function is realized by one resistor only, and the next value by switching-off that one and switching-on some other resistor (Table 1).

For the proposed practical implementation, discretization of the sinusoidal function is performed in 24 points, and in the table we don't start with "0°", but with "$\theta/2$" in order to avoid generation of the value "$\sin 0^\circ$" for which R_e has an infinity value. In order to accomplish progressive turning switch on, $R_e(k)$ represents resistors arranged in a parallel connection assigning the appropriate discrete value of the voltage U_2 to $k-th$ sample, whereby that value is calculated by (9). If $R = 10k\Omega$, then from R_e it follows: $R_1 = 76{,}9k\Omega$, $R_2 = 39{,}5k\Omega$, $R_3 = 44{,}4k\Omega$, $R_4 = 54{,}05k\Omega$, $R_5 = 76{,}3k\Omega$ and $R_6 = 149{,}25k\Omega$.

Table 2. Values of resistors

$\theta_k[^0]$	$\sin\theta_k$	$R_k[k\Omega]$	R_1	R_2	R_3	R_4	R_5	R_6
7.5	0.130	76.923	1	0	0	0	0	0
22.5	0.383	26.110	1	1	0	0	0	0
37.5	0.608	16.447	1	1	1	0	0	0
52.5	0.793	12.610	1	1	1	1	0	0
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112.5	0.793	10.822	1	1	1	1	1	0
127.5	0.793	12.610	1	1	1	1	0	0
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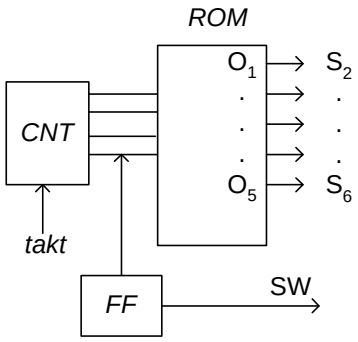

Fig. 5. Block diagram of the control logic

The control logic from the Fig. 5 consists of counter CNT, read only memory ROM, and flip-flop FF. State of the counter is defined by equidistant phase shift from the Table 2. The sinusoidal signal has been generated in two half-periods. Within the first half-period, $0\text{-}180^0$, the switch SW is in the position "1", while in the second one $180^0\text{-}360^0$, the switch SW is in the position "0". State of the switch SW is controled by flip-flop FF, which is induced by the signal from the line with highest weight of the counter CNT. The analog switch S_1 is continuously turned on while lines from O_1 to O_5 regulate switches from S_2 to S_6.

Conclusion

In this paper a new method for frequency synthesis based on the PLL with continuous phase divider has been presented. Look-in table and the D/A converter are replaced by the generator in which n samples of the sinusoidal wave form are generated. The number of the discrete points is eqaul to the modulus of the divider. On this way, a new realization of the dividing function with continuous phase has been enabled. This method of frequency synthesis is characterized by short period of time necessary for reaching the stable state and high purity of the output frequency.

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A. M. Raičević, B. M. Popović. PLL as the Frequency Synthesizer with Continuous Phase Divider // Electronics and Electrical Engineering. – Kaunas: Technologija, 2009. – No. 5(93). – P. 47–50.

A PLL frequency synthesizer which (frequency) divider is replaced by a sinusoidal waveform generator has been analyzed. In the generator, *n* samples of the sinusoidal waveform are generated (created), and (while) the number of discrete points is equal to the dividing module of the divider. By this realization, within every VCO period one sampled value of the sinusoidal function has been generated, it has been sent to the phase detector and together with reference frequency it gives the control voltage. Subsequently, this allows faster reaching of the stable state, which implies high spectral purity of the sinusoidal waveform signal at the synthesizer's output. This approach keeps all advantages of the PLL synthesizers with look-in tables in terms of stability, and in the same time their architecture is much simpler. Ill. 5, bibl. 5 (in English; summaries in English, Russian and Lithuanian).

А. М. Райчевич, Б. М. Попович. Фазовую петлю использующий синтезатор частоты с равномерным делением фазы // Электроника и электротехника. – Каунас: Технология, 2009. – № 5(93). – С. 47–50.

Анализируется PLL синтезатор частоты, в котором делитель частоты заменен генератором сигнала синусойдальной формы. В генераторе создается *n* отсчетов синусойдального сигнала, а число дискретных точек равно модулю деления делителя. Таким образом во время каждого периода напряжением контролируемого осцилятора генерируется одна ситуация синусойдальной функции, она направляется в детектор фазы и по величине опорного сигнала выдается соответсвующее напряжение управления. Это позволяет быстрее достигнуть стабильное состояние, в следствие чего на выходе синтезатора получается синусойдальный сигнал чистого спектра. Метод сохраняет все преимущества PLL синтезатора в части стабильности, а архитектура генератора упрощается. Ил. 5, библ. 5 (на английском языке; рефераты на английском, русском и литовском яз.).

A. M. Raičević, B. M. Popović. Fazinę kilpą naudojantis dažnio sintezatorius su tolygiuoju fazės dalikliu // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2009. – Nr. 5(93). – P. 47–50.

Analizuojamas PLL dažnio sintezatorius, kurio dažnio daliklis pakeistas sinuso formos signalo generatoriumi. Generatoriuje sukuriama *n* sinusinio signalo atskaitų, o diskretinių taškų skaičius yra lygus daliklio dalijimo moduliui. Taigi kiekvieno įtampa kontroliuojamo osciliatoriaus periodo metu sugeneruojama viena sinusinės funkcijos atskaita, nusiunčiama į fazės detektorių ir pagal atraminio dažnio signalą įjungiama atitinkama valdymo įtampa. Tai leidžia greičiau pasiekti stabilią būseną, todėl sintezatoriaus išėjime gaunamas švaraus spektro sinusinis signalas. Taikant šį metodą išlaikomi visi PLL sintezatoriaus stabilumo pranašumai, o generatoriaus architektūra tampa paprastesnė. Il. 5, bibl. 5 (anglų kalba; santraukos anglų, rusų ir lietuvių k.).